INSTRUCTION MANUAL

RFL 9700
Digital Protection Channel

NOTICE

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RFL Electronics Inc.

WARRANTY

Except where noted, all RFL Electronics Inc. products come with a one-year warranty from date of delivery for replacement of any part which fails during normal operation. RFL will repair or, at its option, replace components that prove to be defective at no cost to the Customer. All equipment returned to RFL Electronics Inc. must have an RMA (Return Material Authorization) number, obtained by calling the RFL Customer Service Department. A defective part should be returned to the factory, shipping charges prepaid, for repair or replacement FOB Boonton, N.J.

RFL Electronics Inc. is not responsible for warranty of peripherals, such as printers and external computers. The warranty for such devices is as stated by the original equipment manufacturer. If you have purchased peripheral equipment not manufactured by RFL, follow the written instructions supplied with that equipment for warranty information and how to obtain service.

WARRANTY STATEMENT

RFL Electronics Inc. products are warranted against defects in material and workmanship for one year from the date of shipment. During the warranty period, RFL will repair or, at its option, replace components that prove to be defective at no cost to the customer, except the one-way shipping cost of the failed assembly to the RFL Customer Service facility in Boonton, New Jersey.

This warranty does not apply if the equipment has been damaged by accident, neglect, misuse, or causes other than performed or authorized by RFL Electronics Inc. This warranty specifically excludes damage incurred in shipment to or from RFL. In the event an item is received in damaged condition, the carrier should be notified immediately. All claims for such damage should be filed with the carrier.

NOTE

If you do not intend to use the product immediately, it is recommended that it be opened immediately after receiving and inspected for proper operation and signs of impact damage.

This warranty is in lieu of all other warranties, whether expressed, implied or statutory, including but not limited to implied warranties of merchantability and fitness for a particular purpose. In no event shall RFL be liable, whether in contract, in tort, or on any other basis, for any damages sustained by the customer or any other person arising from or related to loss of use, failure or interruption in the operation of any products, or delay in maintenance or for incidental, consequential, indirect, or special damages or liabilities, or for loss of revenue, loss of business, or other financial loss arising out of or in connection with the sale, lease, maintenance, use, performance, failure, or interruption of the products.

RFL Electronics Inc.
Boonton, New Jersey USA

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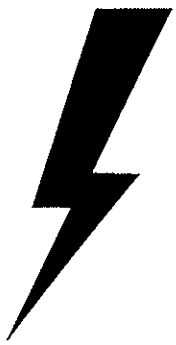
"Z-80" is a registered trademark of Zilog, Inc.

The trademark information listed above is, to the best of our knowledge, accurate and complete.

CAUTION

FOR YOUR SAFETY

THE INSTALLATION, OPERATION, AND MAINTENANCE OF THIS EQUIPMENT SHOULD ONLY BE PERFORMED BY QUALIFIED PERSONS.



WARNING:

The equipment described in this manual contains high voltage. Exercise due care during operation and servicing. Read the safety summary on the reverse of this page.

SAFETY SUMMARY

The following safety precautions must be observed at all times during operation, service, and repair of this equipment. Failure to comply with these precautions, or with specific warnings elsewhere in this manual, violates safety standards of design, manufacture, and intended use of this product. RFL Electronics Inc. assumes no liability for failure to comply with these requirements.

GROUND THE CHASSIS

The chassis must be grounded to reduce shock hazard and allow the equipment to perform properly. Equipment supplied with three-wire ac power cables must be plugged into an approved three-contact electrical outlet. All other equipment is provided with a rear-panel ground terminal, which must be connected to a proper electrical ground by suitable cabling. Refer to the wiring diagram for the chassis or cabinet for the location of the ground terminal.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE OR IN WET OR DAMP AREAS

Do not operate the product in the presence of flammable gases or fumes, or in any area that is wet or damp. Operating any electrical equipment under these conditions can result in a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel should never remove covers. Component replacement and internal adjustments must be done by qualified service personnel. Before attempting any work inside the product, disconnect it from the power source and discharge the circuit by temporarily grounding it. This will remove any dangerous voltages that may still be present after power is removed.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT

Because of the danger of introducing additional hazards, do not install substitute parts or make unauthorized modifications to the equipment. The product may be returned to RFL for service and repair, to ensure that all safety features are maintained.

READ THE MANUAL

Operators should read this manual before attempting to use the equipment, to learn how to use it properly and safely. Service personnel must be properly trained and have the proper tools and equipment before attempting to make adjustments or repairs.

Service personnel must recognize that whenever work is being done on the product, there is a potential electrical shock hazard and appropriate protective measures must be taken. Electrical shock can result in serious injury, because it can cause unconsciousness, cardiac arrest, and brain damage.

Throughout this manual, warnings appear before procedures that are potentially dangerous, and cautions appear before procedures that may result in equipment damage if not performed properly. The instructions contained in these warnings and cautions must be followed exactly.

RFL Electronics Inc.

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Section 1. GENERAL INFORMATION

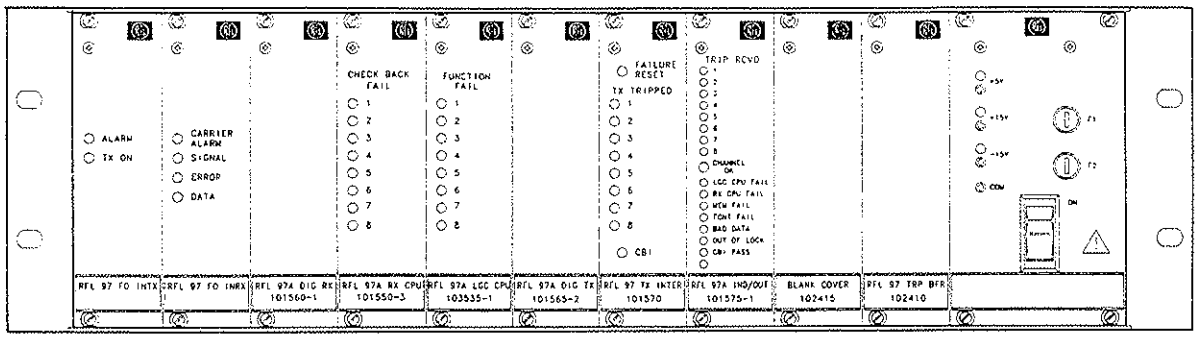


Figure 1-1. RFL 9700 Digital Protection Channel

NOTE

Throughout this manual, data transmission rates are specified in bits per second, or "bps". One Kbps equals 1,000 bits per second, and one Mbps equals 1,000,000 bits per second. One bps is sometimes referred to as one "baud."

Signal names appear in CAPITAL letters. Inverted or active-low signals appear in CAPITAL letters followed by an asterisk (Q1*, RD*, etc).

Specific terminals on terminal blocks, DIP switch sections, and IC and connector pin numbers are noted by the circuit symbol number followed by a dash and the terminal, section, or pin number (TB1-1, SW1-1, IC1-1, P1-1, etc).

1.1. PURPOSE OF THIS MANUAL

This manual provides operation and maintenance information for the RFL 9700 Digital Protection Channel, shown in Figure 1-1. Included are an overall functional description of its purpose, a physical description and specifications, installation instructions, operating procedures, maintenance procedures, theory of operation, and replaceable parts information for all circuit card modules.

1.2. PURPOSE OF EQUIPMENT

The RFL 9700 is a digital system designed for protective relaying; it is particularly suited to transfer trip applications. Unlike traditional tone or carrier transfer trip systems, the RFL 9700 simultaneously sends and receives up to eight transfer trip commands. The primary communications mediums for the RFL 9700 are RS-449 interfaces (at 56 Kbps), and CCITT X.21 interfaces (at 64 Kbps). 56-Kbps terminals also can be connected by fiber optic cable pairs, using an assortment of fiber optic interface modules.

The RFL 9700's performance can be altered by using jumpers and DIP switch settings. This allows you to achieve the security, dependability, and reliability required for each function in your application.

1.3. FEATURES

a. Adaptability. Each of the RFL 9700's eight transfer trip inputs and outputs are independently programmable for a wide range of applications.

b. High Speed. The RFL 9700 is capable of operating within 1.5 to 2 ms, with selectable security and dependability performance.

c. Self Test. Internal diagnostics continuously monitor channel and hardware performance. Besides checking for corrupted communications, key internal components and firmware are monitored to enhance system security.

d. Modular Construction. All parts can be serviced or replaced without major effort. This reduces system down-time and produces shorter MTTR (mean time to repair) times.

e. Fiber Optics. The RFL 9700 is adaptable to all fiber optic requirements; 850 nm or 1300 nm, LED or laser source, singlemode or multimode. Plug-on heads make for simple, trouble-free, field configuration changes.

f. Integrated Optic Multiplexer. 56-Kbps RFL 9700 terminals can be supplied with an eight-port multiplexer. This allows additional functions (such as voice and data) to share the optic path used by the RFL 9700.

g. Dual Processors. All critical communications tasks are handled by one processor; all application and configuration tasks are performed by a separate processor. This allows for maximum system versatility without affecting communications operating criteria, for minimal speed with maximum performance.

h. Choice Of Four Or Eight Outputs. The RFL 9700 can be provided with either four or eight outputs to suit your application. This makes eight digitally-controlled functions available for about the cost of one analog function.

i. RS-449 And CCITT X.21 Interface Capabilities. 56-Kbps RFL 9700 terminals can be interfaced with RS-449 equipment, when equipped with an RS-449 interface module in place of the fiber optic emitter and detector heads. If desired, external RS-449 multiplexer assemblies can be connected to a dedicated connector on the RFL 9700's rear panel; this will allow seven other RS-449 devices to share the fiber optic link with the RFL 9700.

All 64-Kbps RFL 9700 terminals are equipped with a CCITT X.21 interface module. This allows direct connections between the RFL 9700 and CCITT X.21 equipment.

j. Voice And Data Options. Accessory voice and data modules are available. These modules allow voice and data to be sent along the fiber optic line along with the protection signals generated by the RFL 9700.

k. Addressing Feature. An addressing feature is available for enhanced security. A transmit address is appended to the communication packet before it is transmitted. At the receiving end, the received address is verified before the data is processed.

1.4. PHYSICAL DESCRIPTION

Each RFL 9700 terminal is a group of circuit card modules housed in a chassis three rack units high. The chassis accepts circuit cards in a bookshelf-style arrangement. Interconnections between modules are made by a motherboard at the rear of the chassis. External equipment is connected to the chassis through terminal blocks on the rear panel.

1.5. TYPICAL APPLICATIONS

Paragraphs 1.5.1 through 1.5.7 describe some typical applications for the RFL 9700. For more information on these or other possible applications, contact the factory or an RFL Sales Representative.

1.5.1. Relaying

The RFL 9700 can be applied over a 56-Kbps or 64-Kbps synchronous data channel of a T1 multiplexer such as an RFL 9000, as shown in Figure 1-2. This allows for optimum use of channels by providing up to eight functions over a single 56-Kbps or 64-Kbps data channel unit (DCU). Figure 1-2 shows two RFL 9700 terminals used in parallel for communications path redundancy.

1.5.2. Communication Interface

The RFL 9700 is suitable for a variety of communications mediums, such as digital microwave (Fig. 1-3a) or T1 carrier (Fig. 1-3b). 56-Kbps RFL 9700 terminals can be equipped with fiber optic modules that allow its signals to be fed to a remotely located microwave for integration into the existing communications network. (See Figure 1-3c.) Optional multiplex fiber optics modules allow the eight functions of the RFL 9700 to be applied directly to dedicated fibers. The optic modules fit into the card cage, allowing for maximum utilization of panel space and of fiber bandwidth by multiplexing eight RFL 9700 terminals (or other compatible products) onto a single fiber pair.

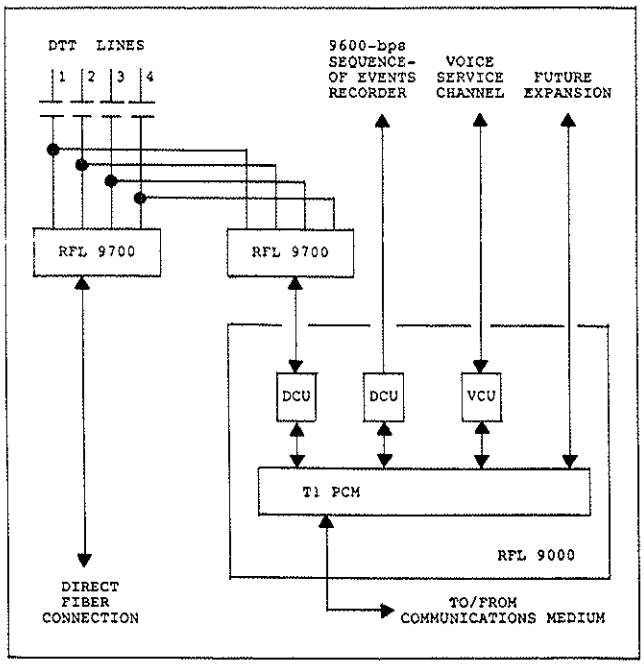


Figure 1-2. Typical relaying application

1.5.3. Fiber Optic Multiplexing

Figure 1-4 shows an application for protection at a power house requiring direct transfer trip (DTT) and line protection (current differential relaying). The 56-Kbps signals are multiplexed into the eight-port fiber optic multiplexer. In this example, an RFL 9720 Pilot Wire Interface is used to convert the current differential signals to 56-Kbps RS-449 data.

1.6. SYSTEM SPECIFICATIONS

As of the date this manual was published, the following specifications apply to all RFL 9700 terminals, except where indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Communications:

56-Kbps Systems:
- Signal Interface: EIA Standard RS-422A.
- Connector Type: EIA Standard RS-449.
- Data Rate: 56 Kbps, synchronous.

64-Kbps Systems:
- Signal Interface: CCITT V.11.
- Connector Type: CCITT X.21.
- Data Rate: 64 Kbps, synchronous.

TRIP Inputs: Optically isolated, solid-state, input current dependent on station battery voltage.

Outputs:

TRIP And GUARD: Solid-state, isolated, 1-amp capacity at station battery voltage.

Alarms: Two Form C (SPDT) relays; one for non-fatal alarms, and one for fatal alarms. Relay contacts are rated for 10 amperes @ 24 Vdc and 0.1 ampere @ 125 Vdc.

TRANSMITTER HAS TRIPPED: Solid-state relay, rated for 0.1 ampere @ 125 Vdc.

Interface Dielectric Strength: All trip, guard, function key, and tone lines are isolated from ground and from all other circuits. Breakdown is 1500 Vrms @ 50/60 Hz, 2500 Vdc, and 2500 volts @ 1.5 MHz. The RFL 9700 meets the Surge Withstand Capability requirements of IEEE 472-1978 (ANSI C.37.90-1978). It also meets the Fast Transient requirements of ANSI-IEEE C.37.90.1.

System Performance: Each function can be individually programmed to select the degree of security and dependability, as shown in Table 1-1.

Temperature:

Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95%, non-condensing.

Input Power Requirements:

Dc-Powered Terminals:
- 24-Volt Input: 19.2 to 28.8 Vdc.
- 48-Volt Input: 42 to 60 Vdc.
- 125-Volt Input: 100 to 150 Vdc.
- 250-Volt Input: 200 to 300 Vdc.

Ac-Powered Terminals:
- 110-Volt Input: 99 to 121 Vac.
- 220-Volt Input: 198 to 242 Vac.

Power Consumption: Less than 50 watts.

Dimensions:

Width: 19 inches (48.3 cm).
Height: 5.25 inches (13.4 cm).
Depth: 13 inches (33.0 cm).

Weight: Less than 25 lbs (11.3 kg).

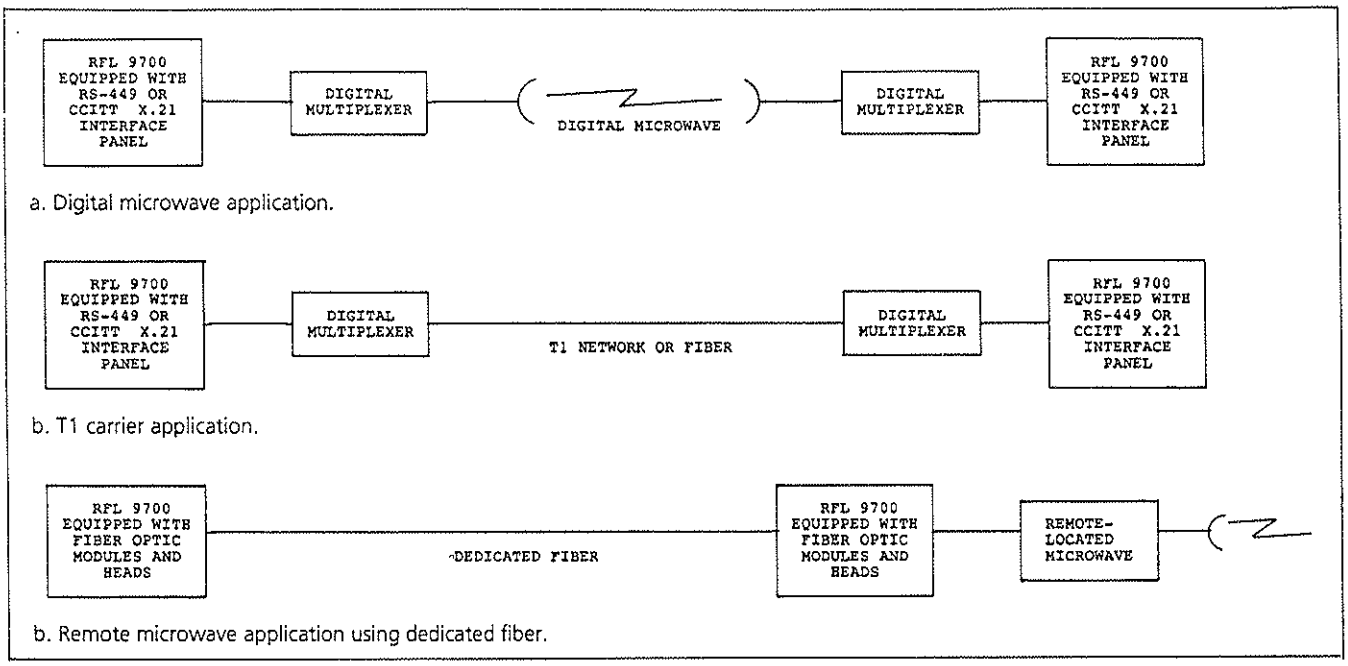


Figure 1-3. Typical communication interface application

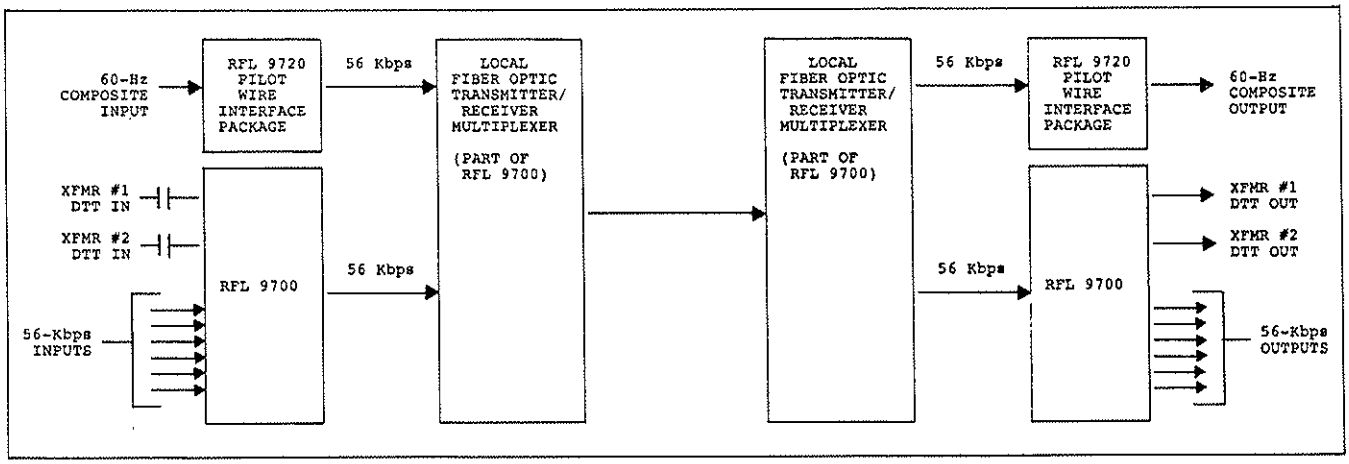


Figure 1-4. Typical fiber optic multiplex application

Table 1-1. Security and dependability, RFL 9700 Digital Protection Channel

Category	Response Time	Response Criteria	Security Acceptance	Dependability
Very Dependable	2.0 ms	1 of 1	1×10^{-14}	99.9986%
Dependable	4.0 ms	2 of 3	1×10^{-18}	99.9968%
Secure	3.0 ms	2 of 2	1×10^{-19}	99.9972%
Very Secure	5.0 ms	3 of 4	1×10^{-19}	99.9958%

NOTE: The security and dependability values given in Table 1-1 are calculated. All calculations were made assuming a bit error rate (BER) of 1×10^{-6}.

1.7. RFL 9700 SUBASSEMBLIES

56-Kbps RFL 9700 terminals can interface with digital communications links that conform to EIA Standard RS-449; 64-Kbps terminals can be used with CCITT X.21 links. The host link can be based on fiber optics, conventional wire-connected T1, microwave, or any system providing a synchronous 56-Kbps (RS-449) or 64-Kbps (CCITT X.21) link.

Each RFL 9700 terminal contains several circuit card modules and other subassemblies, which are described below. The block diagram of a typical RFL 9700 terminal is shown in Figure 1-5. The space and power requirements for all RFL 9700 modules are listed in Table 1-3. Table 1-4 gives the space and power requirements for all RFL 9700 accessory equipment. The module complements required for various terminal configurations are shown in Table 1-2.

a. Input/Output Module. Each RFL 97 I/O input/output module contains four isolated TRIP output drivers, four isolated GUARD output drivers, four HAS TRIPPED relays, four optically-isolated input circuits, and high-voltage and transient suppression circuits. This allows the RFL 9700 terminal to support four functions; two RFL 97 I/O modules are required for eight-function configuration capability. Section 5 of this manual provides additional information on the RFL 97 I/O.

b. Trip Buffer. The RFL 97 TRIP BUFFER accepts the function keying information from the input isolators on the RFL 97 I/O and implements the acceptance criteria. Additional information on the RFL 97 TRIP BUFFER can be found in Section 6 of this manual.

c. Transmitter Interface Module. The RFL 97 TX INTER accepts the function key signals from the RFL 97 TRIP BUFFER and places them on the control bus. It also contains the function programming switches for the RFL 97A LOGIC CPU, and an LED array that shows when a channel has tripped. Section 7 of this manual provides additional information on the RFL 97 TX INTER.

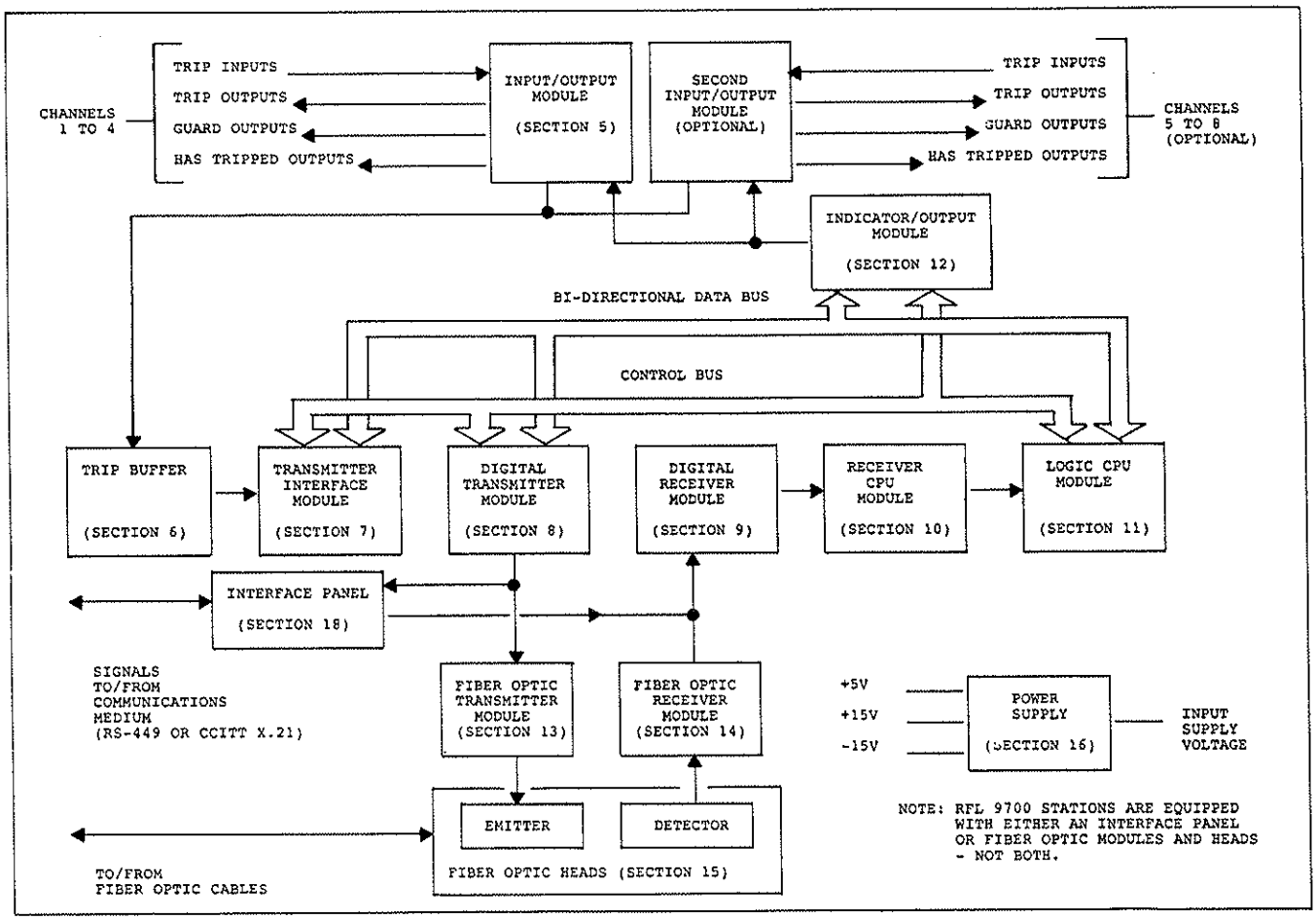


Figure 1-5. Block diagram, RFL 9700 Digital Protection Channel

Table 1-2. Space and power requirements, RFL 9700 subassemblies

Description	Model No.	Assy. No.	Current Draw (1)			Module Spaces Required	Additional Information
			+5V	+15V	-15V		
Input/Output Module (2)	RFL 97 I/O	101585	200	. . .	. . .	(3)	Section 5
Trip Buffer Module	RFL 97 TRIP BUFFER	102410	200	. . .	. . .	1	Section 6
Transmitter Interface Module	RFL 97 TX INTER	101570	125	. . .	. . .	1	Section 7
Digital Transmitter Modules:							
56-Kbps Operation	RFL 97A DIG TX 56	101565-2	150	. . .	. . .	1	Section 8
64-Kbps Operation	RFL 97A DIG TX 64	101565-3					
Digital Receiver Modules:							
56-Kbps Operation	RFL 97A DIG RX 56	101560-1	175	. . .	. . .	1	Section 9
64-Kbps Operation	RFL 97A DIG RX 64	103545-1					
Receiver CPU Module	RFL 97A RX CPU	101550-3	275	. . .	. . .	1	Section 10
Logic CPU Module	RFL 97A LOGIC CPU	103535-1	275	. . .	. . .	1	Section 11
Indicator/Output Module	RFL 97A IND/OUT	101575-1	275	10	10	1	Section 12
Fiber Optic Transmitter Modules:							
Single RS-422 Input	RFL 97 FO INTX	101530	150	20	. . .	1	Section 13
Eight RS-422 Inputs	RFL 97 FO INTX-1	101535					
Fiber Optic Receiver Modules:							
Single RS-422 Output	RFL 97 FO INRX	101540	200	25	20	1	Section 14
Eight RS-422 Outputs	RFL 97 FO INRX-1	101545					
Fiber Optic Emitter Heads:							
850-nm Multimode LED	RFL 97 FO TX-8M	102435	500	50	50	(4)	Section 15
1300-nm Multimode LED	RFL 97 FO TX-13M	102440	1200	30	50		
1300-nm Singlemode LED	RFL 97 FO TX-13S	102445	1200	30	50		
1300-nm Singlemode Laser	RFL 97 FO TX-13LS	101505	150	50	50		
Fiber Optic Detector Heads:							
850-nm Multimode	RFL 97 FO RX-8M	101515	500	50	10	(5)	
1300-nm Multimode	RFL 97 FO RX-13M	101520-1	20	40	10		
1300/1500-nm Singlemode	RFL 97 FO RX-13/15S	101520-2	1100	30	100		
50-Watt Power Supply Modules:							
24-Vdc Input	RFL 9150A 24 DCPS	101980-1	6000	1500	1500	2	Section 16
48-Vdc Input	RFL 9150B 48 DCPS	101980-2					
125-Vdc Input	RFL 9150B 125 DCPS	101980-3					
250-Vdc Input	RFL 9150A 250 DCPS	101980-4					
110-Vac Input	RFL 9150B 110 ACPS	101985-1					
220-Vac Input	RFL 9150A 220 ACPS	101985-2					
Chassis And Interface Panels:							
Chassis, single-Euro	RFL 97 CHAS	102450-5	. . .	. . .	. . .	. . .	Section 17
RS-449 Interface Panel	RFL 97 449 INTER	102490	. . .	. . .	. . .	(6)	
CCITT X.21 Interface Panel	RFL 97 X.21 INTER	103560	. . .	. . .	. . .	(6)	

1. Currents are shown in milliamperes. Values shown for power supply modules are output capacity.
2. Current draw shown is for four-channel unit; double the listed current draw for eight-channel units.
3. Mounts at rear of chassis, in the space allotted for the I/O module.
4. Mounts at rear of chassis, in the space allotted for fiber optic emitter heads.
5. Mounts at rear of chassis, in the space allotted for fiber optic emitter heads.
6. Mounts at rear of chassis, across the two spaces allotted for fiber optic heads.

Table 1-3. Space and power requirements, RFL 9700 accessory equipment

Description	Model No.	Assy. No.	Current Draw (1)			Module Spaces Required	Additional Information
			+5V	+15V	-15V		
RS-449 Multiplex Panel	RFL 97 449 MUX	102495	. . .	. . .	. . .	(2)	
1U Chassis (3)	RFL 97 1U CHAS	103500	. . .	. . .	. . .	(4)	
Voice Option (5)	RFL 97 VOICE OPTION	103510	115	45	10	(6)	
Data Option (7)	RFL 97 DATA OPTION	103505	130	5	5	(6)	
RS-449 Option For 1U Chassis	RFL 97 449 OPTION	103515	. . .	. . .	. . .	(8)	

1. Currents are shown in milliamperes.
2. Occupies three rack units (3U, or 5.25 inches) of vertical space in rack or cabinet above or below RFL 9700.
3. Required to house voice option and/or data option modules.
4. Occupies one rack units (1U, or 1.75 inches) of vertical space in rack or cabinet above or below RFL 9700.
5. Includes voice module, I/O module, handset, and wiring harness.
6. Occupies one module position in RFL 97 1U CHAS.
7. Includes data module, I/O module, adapter connector, and wiring harness.
8. Occupies one I/O module position in RFL 97 1U CHAS.

Table 1-4. RFL 9700 module complements for various station configurations

Module	Assembly Number	56-Kbps Transmit Only	56-Kbps Receive Only	56-Kbps Transmit And Receive	64-Kbps Transmit Only	64-Kbps Receive Only	64-Kbps Transmit And Receive
RFL 97 I/O (1)	101585	X	X	X	X	X	X
RFL 97 TRIP BUFFER	102410	X	. . .	X	X	. . .	X
RFL 97 TX INTER	101570	X	. . .	X	X	. . .	X
RFL 97A DIG TX 56	101565-2	X	. . .	X	. . .	. . .	. . .
RFL 97A DIG TX 64	101565-3	. . .	. . .	. . .	X	. . .	X
RFL 97A DIG RX 56	101560-1	. . .	X	X	. . .	. . .	. . .
RFL 97A DIG RX 64	103545-1	. . .	. . .	. . .	. . .	X	X
RFL 97A RX CPU	101550-3	. . .	X	X	. . .	X	X
RFL 97A LOGIC CPU	103535-1	X	X	X	X	X	X
RFL 97A IND/OUT	101575-1	X	X	X	X	X	X
RFL 97 FO INTX (single-input)	101530	(2)	. . .	(2)	. . .	. . .	. . .
RFL 97 FO INTX (eight-input)	101535	(2)	. . .	(2)	. . .	. . .	. . .
RFL 97 FO INRX (single-output)	101540	. . .	(2)	(2)	. . .	. . .	. . .
RFL 97 FO INRX (eight-output)	101545	. . .	(2)	(2)	. . .	. . .	. . .
RFL 9150* ** (power supply) (3)	(3)	X	X	X	X	X	X
RFL 97 449 INTER (RS-449)	102490	(4)	(4)	(4)	. . .	. . .	. . .
RFL 97 X.21 INTER (CCITT X.21)	103560	. . .	. . .	. . .	X	X	X

1. Each RFL 97 I/O module contains the trip input, guard output, output key function, and "has tripped" modules for four channels. If your station is to be configured for one to four channels, only the lower I/O module is required. If more than four channels will be used, both I/O modules are necessary. Check the "as supplied" drawings furnished with the equipment.

2. Fiber optic modules are optional; their presence depends on the communications link setup. Check the "as supplied" drawings furnished with the equipment. Fiber optic modules cannot be used in 64-Kbps stations.

3. Model and assembly number will vary according to the available input voltage. See Table 1-2 for choices.

4. Must be fitted if station is not equipped with fiber optic modules.

d. Digital Transmitter Modules. RFL 9700 digital transmitter modules accept data from the bi-directional data bus. They use this data to generate a digital word that contains the eight functions. This word is then prepared for transmission.

There are two different digital transmitter modules available for the RFL 9700. The RFL 97A DIG TX 56 operates at 56 Kbps and meets the requirements of EIA Standard RS-449. It can interfaces with either the RS-449 interface panel on the rear panel or the optional fiber optic transmitter module. The RFL 97A DIG TX 64 operates at 64 Kbps and meets the X.21 requirements specified in CCITT V.11. It interfaces with a CCITT X.21 interface panel on the rear panel.

Section 8 of this manual contains more information on both digital transmitter modules.

e. Digital Receiver Modules. RFL 9700 digital receiver modules decode incoming messages and passes the information over to the receiver CPU module.

Two different digital receiver modules are available for RFL 9700 terminals. The RFL 97A DIG RX 56 operates at 56 Kbps, and interfaces directly to the RS-449 connector on the 449 interface panel or the fiber optic receiver. The RFL 97A DIG RX 64 performs the same function, but operates at 64 Kbps and interfaces to the CCITT X.21 connector on the X.21 interface panel.

Section 9 of this manual provides additional information on both digital receiver modules.

f. Receiver CPU Module. The RFL 97A RX CPU Receiver CPU Module accepts the decoded information from the digital receiver module, and determines if the data is valid. Once this is done, it converts the message into eight-bit parallel data, which is passed to the logic CPU module. Checkback testing is performed by this module, and an array of sealed-in LED indicators on its front panel provide a visual indication of checkback failures. Additional information on the RFL 97A RX CPU can be found in Section 10 of this manual.

g. Logic CPU Module. The RFL 97A LOGIC CPU Logic CPU Module accepts the parallel data from the receiver CPU module, and conditions the data as determined by the switch settings on the transmitter interface module. Its standard software enables various functions, such as trip hold, command extend, guard-before-trip, and unblocking.An LED array on the front panel provides a visual indication of channel function failures.

Optional permissive coordination software adapts the RFL 97A LOGIC CPU to applications requiring permissive coordinating functions, such as echo and current reversal timing. Other functions can be accommodated through the use of customized software, developed by RFL for specific applications.

Additional information on the RFL 97A LOGIC CPU can be found in Section 11 of this manual.

h. Indicator/Output Module. The RFL 97A IND/OUT Indicator/Output Module contains the drivers for the output devices on the RFL 97 I/O. It also contains an LED array, which provides a visual display of received trips and system errors. Section 12 of this manual provides additional information on the RFL 97A IND/OUT.

i. Fiber Optic Interface Assemblies. The following fiber optic interface assemblies are available for interfacing the RFL 9700 to fiber optic cables. Block diagrams showing the relationship between these assemblies appear in Figure 1-6 (single-channel) and Figure 1-7 (eight-channel).

(1) Fiber Optic Transmitter Modules. The RFL 97 FO INTX accepts the signals generated by the digital transmitter module and conditions them for optic transmission. Multiplexer circuits on the RFL 97 FO INTX-1 allow up to eight 56-Kbps channels to be multiplexed and transmitted over a single fiber. Section 13 of this manual provides additional information on both fiber optic transmitter modules.

(2) Fiber Optic Receiver Modules. The RFL 97 FO INRX accepts an input from a fiber optic detector head and converts it back into the RS-422 signals that can be processed by the digital receiver module. The RFL 97 FO INRX-1 contains eight de-multiplexer circuits, which allow the RFL 9700 terminal to isolate one of up to eight 56-Kbps channels that are multiplexed and transmitted over a single fiber. Section 14 of this manual provides additional information on both fiber optic receiver modules.

(3) Fiber Optic Heads. Each RFL 9700 fiber optic module uses an optic head, which is mounted at the rear of the RFL 9700 chassis. This allows the fiber optic modules to be removed without drawing the fiber through the chassis.

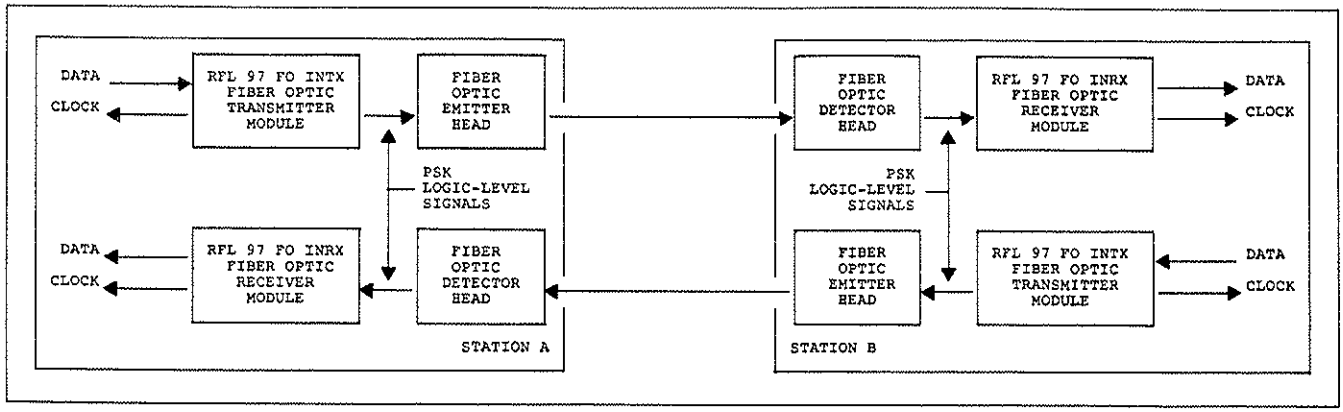


Figure 1-6. RFL 9700 single-channel fiber optic communication system

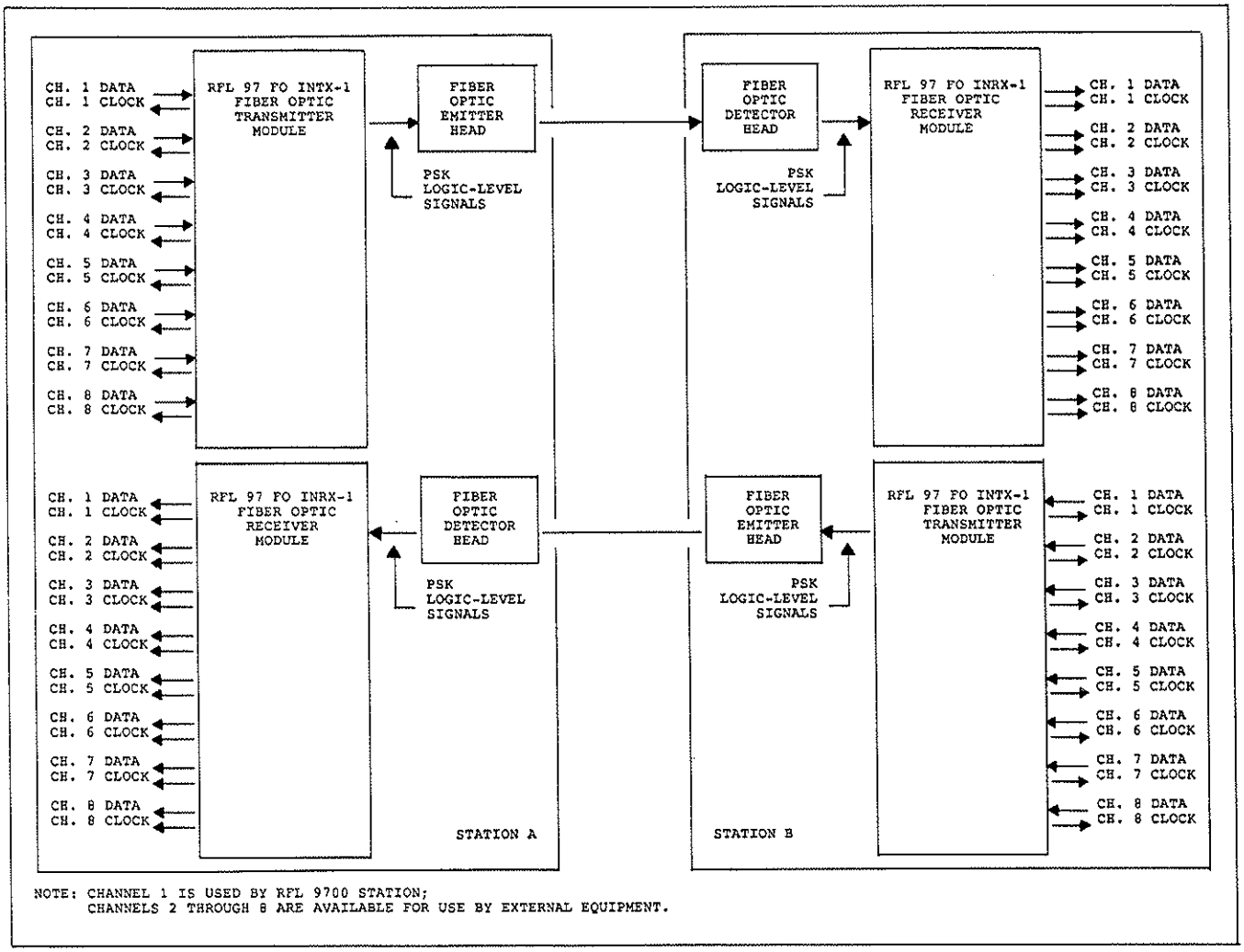


Figure 1-7. RFL 9700 eight-channel fiber optic communication system

A variety of heads are available: 850-nm or 1300-nm wavelength, singlemode or multimode LED emitter, or singlemode laser emitter. Section 15 of this manual provides additional information on all currently-available fiber optic heads.

j. Power Supply. RFL 9150 50-watt power supply modules accept the available input supply voltage and produce three dc output voltages: +5, +15, and -15. Several different versions available to accommodate a wide range of input voltages. Additional information on these power supplies can be found in Section 16 of this manual.

k. Chassis. The RFL 97 CHAS chassis serves as the main enclosure for the RFL 9700, providing a means of housing and interconnecting all the RFL 9700 modules. It can be mounted in any standard EIA 19-inch rack or cabinet, or it can be used as a standalone desk-mount cabinet. When rack-mounted, the RFL 97 CHAS occupies three vertical rack mounting spaces, or 5.25 inches of vertical panel space (13.34 cm). Adjustable mounting ears allow the chassis to be mounted so that its front panel is either flush with the rack or protruding out the front of the rack. Additional information on the RFL 97 CHAS can be found in Section 17 of this manual.

l. Accessory Equipment. Other circuit card modules and assemblies are available to enhance the operation of the RFL 9700 system, or to adapt it to special applications. If any accessory equipment was furnished with your system, Instruction Data Sheet for each item will appear in Section 18 of this manual.

Section 2. INSTALLATION

WARNING

ALL RFL 9700 TERMINALS ARE EQUIPPED WITH A PROTECTIVE COVER THAT EXTENDS ACROSS THE REAR OF THE CHASSIS. THIS COVER IS INTENDED TO PROTECT THE OPERATOR FROM POTENTIALLY HAZARDOUS VOLTAGES, WHICH MAY BE PRESENT ON THE RFL 97 I/O INTERFACE ASSEMBLY'S TERMINAL BLOCKS. THIS COVER MUST ONLY BE REMOVED BY QUALIFIED SERVICE PERSONNEL WHEN ACCESS TO THE REAR PANEL IS REQUIRED. IT MUST BE REPLACED BEFORE PLACING THE TERMINAL IN SERVICE.

CAUTION

During normal system operation, the switching of relay contacts can produce voltage spikes. These spikes can travel down the relay output leads and induce currents in other leads. These induced currents can result in false trips or system misoperation. To reduce this possibility, use a shielded twisted pair for each input lead, and ground the shield at the RFL 9700 chassis only. As an added precaution, do not bundle input, output, and power leads into the same harness - keep them as far apart as possible.

Whenever the protective cover is removed from the rear of the chassis, check all terminal block mounting screws for tightness. Loose terminal block mounting screws can result in compromised surge withstand capabilities (SWC), leading to component damage.

2.1. INTRODUCTION

This section contains installation instructions for the RFL 9700, including unpacking, mounting, and interconnection wiring.

2.2. UNPACKING

RFL 9700 equipment may be supplied as individual chassis or interconnected with other chassis or assemblies as part of a system. Paragraph 2.2.1 provides unpacking instructions for individual chassis, and paragraph 2.2.2 provides instructions for interconnected chassis.

2.2.1. Individual Chassis

RFL 9700 terminals supplied as individual chassis are packed in their own shipping cartons:

1. Open each carton carefully to make sure the equipment is not damaged.
2. After the chassis is removed from the carton, carefully examine all packing material to make sure no items of value are discarded.
3. Carefully remove any packing materials inserted into the chassis to hold circuit cards in place during transit.
4. Make sure all front-panel modules are fully seated in the chassis. The quarter-turn fasteners securing each module in place should all be in the locked position (screwdriver slots vertical.

If you notice any signs of shipping damage, immediately notify RFL Customer Service at the phone number on the front of this manual. Save all the packing material and the shipping carton, in case a damage claim needs to be filed with the shipping company that delivered the unit.

2.2.2. Interconnected Chassis

RFL 9700 terminals ordered as part of a larger system may be interconnected with other chassis and mounted in a relay rack or cabinet, or on shipping rails for installation into a rack or cabinet at the customer's site. In such cases, the entire assembly is enclosed in a wood crate or delivered by air-ride van:

1. If the equipment is crated, carefully open the crate to avoid damaging the equipment.

2. Remove the equipment from the crate and carefully examine all packing materials to make sure no items of value are discarded.

3. Carefully remove any packing materials that were inserted into the individual chassis to hold circuit cards in place during transit.

4. Make sure all front-panel modules are fully seated in the chassis. The quarter-turn fasteners securing each module in place should all be in the locked position (screwdriver slots vertical.

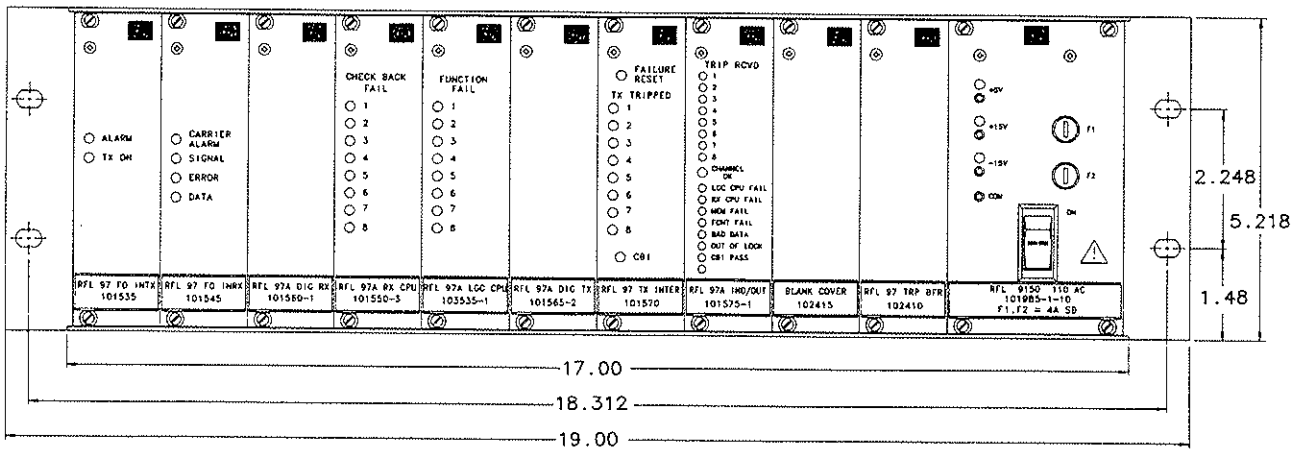
If you notice any signs of shipping damage, immediately notify RFL Customer Service at the phone number on the front of this manual. Save all the packing material and the shipping carton, in case a damage claim needs to be filed with the shipping company that delivered the unit.

2.3. MOUNTING

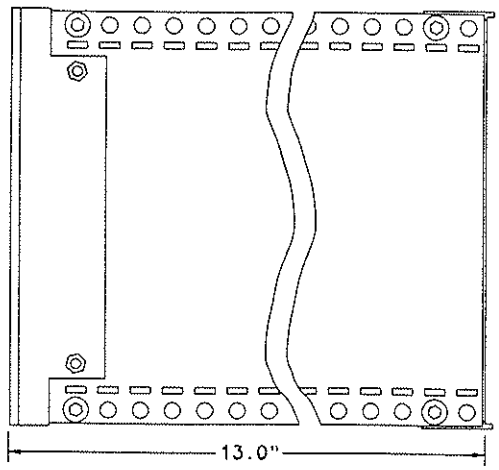
After unpacking, RFL 9700 equipment must be securely mounted, following the instructions in paragraphs 2.3.1 through 2.3.3.

2.3.1. Individual Chassis

RFL 9700 terminals housed in individual chassis have two mounting ears (one on each side). Hole sizes and spacings conform with EIA standards, so the RFL 9700 can be mounted in any standard 19-inch rack or cabinet. Complete chassis dimensions are shown in Figure 2-1.



a. Front view.



b. Side view.

Figure 2-1. Mounting dimensions, RFL 9700 Digital Protection Channel

CAUTION

Any installation using an enclosed cabinet with a swing-out rack must be securely fastened to the floor. This will prevent the cabinet from falling forward when the rack is moved outward.

2.3.2. Interconnected Chassis Installed In Rack Or Cabinet

Systems mounted in racks or cabinets at the factory are to be placed in position and then bolted to the floor or wall, as appropriate, to secure the equipment in place.

The type of hardware used will depend upon the particular surface to which the rack or cabinet is being mounted. Because of this, mounting hardware is not supplied with the rack or cabinet.

2.3.3. Interconnected Chassis Mounted On Shipping Rails

Equipment to be installed in a rack or cabinet at the customer's site is mounted on shipping rails at the factory. To remove the shipping rails and mount the equipment, proceed as follows:

1. Place the equipment as close to the front of the rack or cabinet as possible, with the rear panels of the equipment facing the front of the rack or cabinet.

2. Remove all the screws securing the shipping rails to the equipment.

3. Slide the equipment into the rack or cabinet.

4. Install and tighten screws to all panels to secure the equipment in place.

2.4. VENTILATION

The specified operating temperature range for RFL 9700 equipment is -30°C to +65°C (-22°F to +149°F). Operation at higher temperatures may affect system reliability and performance. Systems installed in enclosed cabinets should be ventilated to keep the temperature inside the cabinet within limits.

2.5. CONNECTIONS

Electrical connections are made to each RFL 9700 chassis through the terminal blocks and connectors on the chassis rear panel. The rear panels of three typical RFL 9700 terminals are shown in Figure 2-2; one equipped with fiber optic modules, one with an RS-449 interface panel, and one with a CCITT X.21 interface module.

Paragraphs 2.5.1 through 2.5.6 provide basic descriptions of all the connections that must be made. Refer to the "as supplied" drawings furnished with your RFL 9700 for more detailed descriptions of the connections that must be made to your system.

2.5.1. Making Connections To Terminal Blocks

The terminal blocks on the RFL 97 I/O interface assembly are conventional screw-type barrier blocks. Wires can either be stripped or terminated in spade or ring lugs, depending on local practice. To connect wires to the terminal blocks, proceed as follows:

1. Remove the protective cover from the rear of the chassis by pulling it out of the standoffs holding it in place.

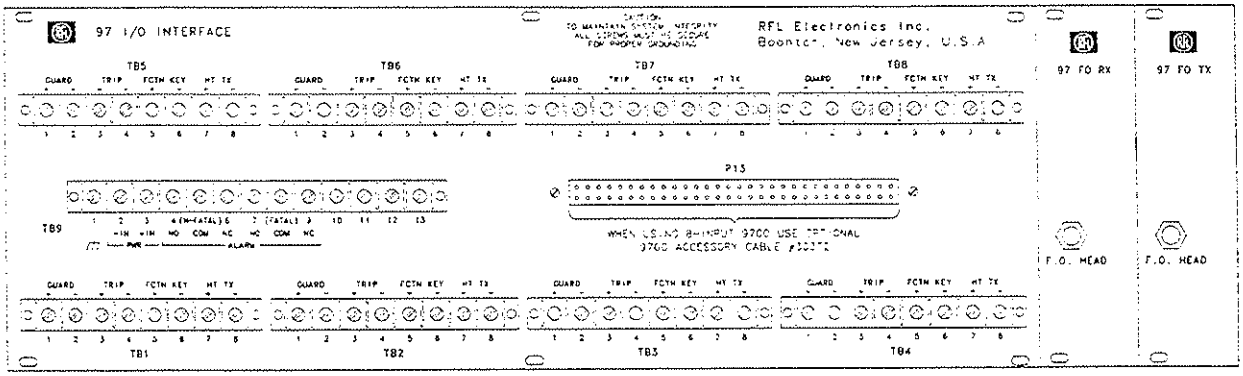
2. Using strippers, remove about 1/4 inch (10 cm) of insulation from the end of the wire to be connected.

3. If local practice calls for lugged wires, crimp a spade or ring lug onto the stripped end of the wire.

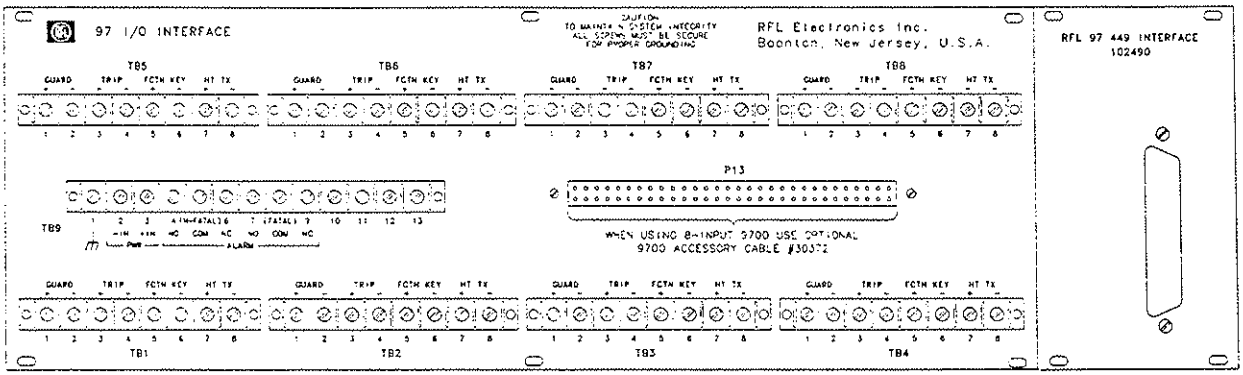
4. Locate the terminal to which the wire is to be connected.

   All terminals blocks are numbered. Terminal numbers appear on the rear panel, directly below the terminal block. Terminal block numbers are directly below the terminal numbers.

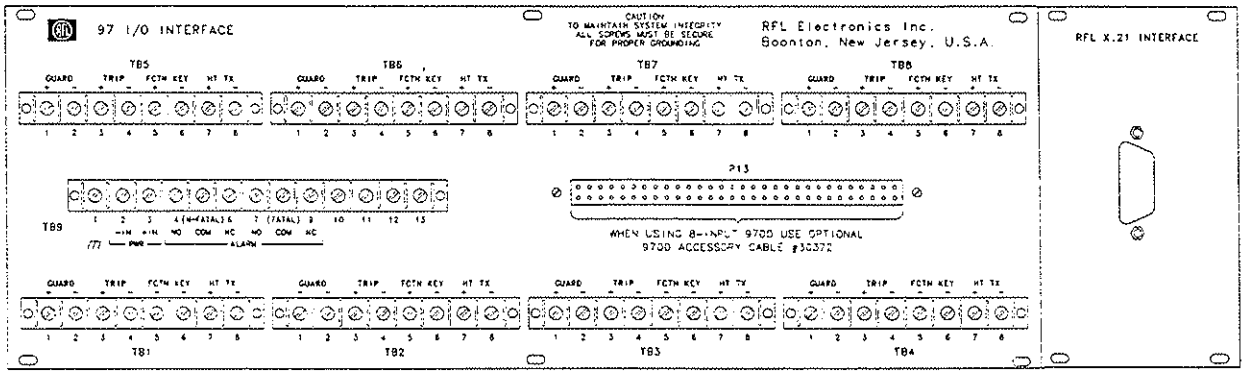
5. Using a 1/4-inch flat-blade screwdriver, turn the screw at that position counterclockwise until the wire or lug can be slipped underneath the screw head. If ring lugs are being used, remove the screw completely.



a. Terminal with fiber optic modules.



b. Terminal with RS-449 interface panel.



c. Terminal with CCITT X.21 interface panel.

Figure 2-2. Rear views of typical RFL 9700 terminals

6. Place the wire in position on the connector.

   If the wire is lugged with a spade lug, slip the lug under the screw head. If the wire is lugged with a ring lug, insert the screw removed during step 5 into the lug and into the terminal block, turning the screw until finger-tight. If lugs are not being used, use a pair of needle-nose pliers to bend the stripped end of the wire into a hook. Slip this hook under the screw head so that the hook surrounds the screw in a clockwise direction.

7. Using a 1/4-inch flat-blade screwdriver, turn the screw clockwise until tight to secure the wire in place.

8. Repeat steps 2 through 8 for all other wires to be connected.

9. Line up the mounting holes in the rear panel protective cover with the standoffs on the rear of the chassis, and push down on the protective cover until it is secured in place.

2.5.2. Channel Input/Output Connections

All RFL 97 I/O interface assemblies are equipped with four terminal blocks for channel input/output connections, designated TB5 through TB8. If the RFL 97 I/O is equipped for eight channels, four additional terminal blocks (TB1 through TB4) will be present. Connections for Channel 1 are made to TB5 in four-channel terminals, and TB5 in eight-channel terminals.

The following terminal assignments apply to all eight channel input/output terminal blocks. The "X" in the terminal designation stands for the channel being connected. For example, the GUARD output for Channel 4 is between TB8-1 and TB8-2 in four-channel terminals, and between TB4-1 and TB4-2 in eight-channel terminals.

a. GUARD. The GUARD outputs are calculated signals that are present whenever no trips are being received and no alarm conditions are detected; when the system is functioning normally, the GUARD outputs will be active. The positive GUARD output (GUARD +) is connected to TBX-1; the negative GUARD output (GUARD -) to TBX-2.

b. TRIP. Trip outputs are produced in response to received trip signals that are decoded by the digital receiver module (Section 9). They are used to send trip commands to the external equipment at the station where the RFL 9700 is located. The positive TRIP output (TRIP +) is connected to TBX-3; the negative TRIP output (TRIP -) to TBX-4.

c. FCTN KEY (Function Key). The FCTN KEY inputs accept signals generated by the fault relay contacts being monitored by the RFL 9700. If the signals meet the proper timing and logic criteria, they will be converted into trip signals that will be sent to the other end of the communications link. The positive FCTN KEY input (FCTN KEY +) is connected to TBX-5; the negative FCTN KEY input (FCTN KEY -) to TBX-6.

d. HT TX (Has Tripped). The HAS TRIPPED outputs indicate the status of the transmitted trip byte. The positive HT TX output (HT TX +) is connected to TBX-7; the negative HT TX output (HT TX -) to TBX-8.

2.5.3. Alarm Relay Connections

The contacts of the two alarm relays are wired to terminal block TB9 on the RFL 97 I/O interface assembly (Section 5). Terminal assignments are as follows:

a. Non-Fatal Alarms. Non-fatal alarms are generated by conditions that will not result in a system shutdown, such as function failures and checkback failures. If the RFL 97 IND/OUT module (Section 12) detects a non-fatal alarm condition, Relay #1 will change state. Its contacts are wired to the following terminals on TB9:

N.O.	TB9-4
COM	TB9-5
N.C.	TB9-6

b. Fatal Alarms. Fatal alarms are generated by conditions that are severe enough to shut down the RFL 9700 system; these include component failures on the RFL 97 RX CPU and RFL 97 LOGIC CPU modules (Sections 10 and 11), memory failures, the detection of bad data, and loss of sync.

If the RFL 97 IND/OUT module (Section 12) detects a fatal alarm condition, Relay #2 will change state. Its contacts are wired to the following terminals on TB9:

N.O.	TB9-7
COM	TB9-8
N.C.	TB9-9

WARNING

RFL 97 FO TX-13LS FIBER OPTIC EMITTER HEADS USE A LASER LIGHT SOURCE THAT PRODUCES INVISIBLE RADIATION. IF YOUR RFL 9700 TERMINAL IS EQUIPPED WITH ONE OF THESE HEADS, STARING DIRECTLY INTO THE LIGHT BEAM MAY RESULT IN EYE DAMAGE AND/OR BLINDNESS. NEVER LOOK DIRECTLY INTO THE LIGHT BEAM AND BE CAREFUL NOT TO SHINE THE LIGHT AGAINST ANY REFLECTIVE SURFACE.

THE LASER SOURCE IS A CLASS IIIb LASER PRODUCT, USING GALLIUM INDIUM ARSENIDE PHOSPHIDE. ITS RECOMMENDED MAXIMUM POWER OUTPUT IS 7 mW. IT COMPLIES WITH APPLICABLE DHHS STANDARDS UNDER THE RADIATION CONTROL FOR HEALTH AND SAFETY ACT OF 1968.

2.5.4. Fiber Optic Connections

If your RFL 9700 terminal is equipped with fiber optic modules, fiber optic pigtails must be connected to the fiber optic heads on the rear panel of the chassis. Amphenol 906 Series fiber optic connectors (or their equivalent) are used with multimode fibers; Type ST connectors are used with singlemode fibers. The exact connector used will depend upon the head that is installed in the terminal, and the specific optic cable being used.

When connecting the fiber optic pigtails, make sure the connectors are properly aligned before tightening, and then fully tighten them. This will help minimize losses in the connector.

2.5.5. RS-449 And X.21 Interface Connections

If your RFL 9700 terminal is equipped with an RS-449 interface panel, there will be a 37-pin male D-subminiature connector (DC-37) on the rear of the chassis that mates with any standard female RS-449 connector. If the terminal is equipped with an X.21 interface panel, there will be a 15-pin male D-subminiature connector (DA-15) that mates with any standard female X.21 connector. Table 2-1 shows the pins on these connectors that are supported by the RFL 9700.

When fastening a mating connector to the interface panels, make sure the retaining screws at both ends of the mating connector are tightened to secure the cable connector to the panel.

Table 2-1. RS-449 and X.21 interface connections, RFL 9700 Digital Protection Channel

RS-449 Signal	RS-449 Pin No.	X.21 Signal	X.21 Pin No.
RD -	24	Receive A	4
RD +	6	Receive B	11
RS -	25	Control A	3
RS +	7	Control B	10
RT +	8	Sig. Timing B	13
RT -	26	Sig. Timing A	6
SD -	22	Transmit A	2
SD +	4	Transmit B	9
ST +	5	Sig. Timing B	13
ST -	23	Sig. Timing A	6
SG	19	Sig. Ground	8
Shield	1	Shield	1

If an RFL 97 449 MUX multiplexer panel was supplied along with the RFL 9700, the ribbon cable attached to the multiplexer panel must be plugged into the mating connector on the rear of the RFL 9700, which is next to terminal block TB9. (See Figure 2-2 for location.) The RS-449 pins that are supported by the RFL 9700 are the same as for the RFL 97 449 inter panel, as listed in Table 2-1.

The RFL 97 449 MUX is an eight-channel multiplexer. The RS-449 connectors on the rear of this panel can accept up to seven RS-449 I/O connectors. The eighth channel is reserved for the RFL 9700.

WARNING

THE RFL 9700 CHASSIS MUST BE PROPERLY GROUNDED AS DESCRIBED IN THE FOLLOWING PARAGRAPH BEFORE ATTEMPTING TO CONNECT INPUT POWER. IMPROPER GROUND CONNECTIONS MAY RESULT IN SYSTEM MALFUNCTIONS, EQUIPMENT DAMAGE, OR ELECTRICAL SHOCK.

2.5.6. Chassis Ground Connections

TB9-1 on the RFL 97 I/O Input/Output Module (Section 5) is the main ground for the RFL 9700 terminal. Grounding is accomplished in dc-powered terminals by connecting a wire 16 AWG or larger between TB9-1 and a solid earth ground. The grounding wire should be kept as short and straight as possible, to keep its resistance and inductance to a minimum.

CAUTION

RFL 9700 terminals utilizing ribbon cable connections for RS-449 communications must have a positive circuit common connection between the RFL 9700 and all related equipment. System misoperation may result if the equipment is not properly grounded.

CAUTION

Before attempting to make power connections, make sure the RFL 9700 terminal is equipped with a power supply designed to operate at the available input supply voltage. This can be determined by checking the model designator on the module handle; if an external power supply is being used, check the markings on the external power supply. If the wrong voltage is connected to the power supply, component damage will result.

2.5.7. Input Power Connections

After all other connections have been made to the RFL 9700, input power connections can be made to terminal block TB9.

If the RFL 9700 terminal is equipped with a dc-input RFL 9150A or RFL 9150B power supply module, connect the positive input to TB9-3, and the negative input to TB9-2.

If the RFL 9700 terminal is equipped with an ac-input RFL 9150A or RFL 9150B power supply module, connect the "hot" side of the ac line to TB9-3, and the "neutral" side of the line to TB9-2.

Section 3. OPERATING INSTRUCTIONS

3.1. INTRODUCTION

This section contains the instructions necessary for operating the RFL 9700. All controls and indicators are shown and described. The jumper and switch settings are also described, and a procedure is included for verifying operation before placing the RFL 9700 into continuous service.

3.2. CONTROLS AND INDICATORS

The front panels of the circuit card modules in each RFL 9700 contain controls and indicators which are used to prepare it for use, monitor system functions during normal operation, initiate checkback tests, and reset alarms. Figure 3-1 shows the module locations in a typical RFL 9700 terminal. Table 3-1 lists the figures and tables in this section that describe the controls and indicators on each module.

If your RFL 9700 was equipped with any accessory equipment containing controls and indicators, refer to the Instruction Data Sheets in Section 18 of this manual for further information.

(Text continued on page 3-11)

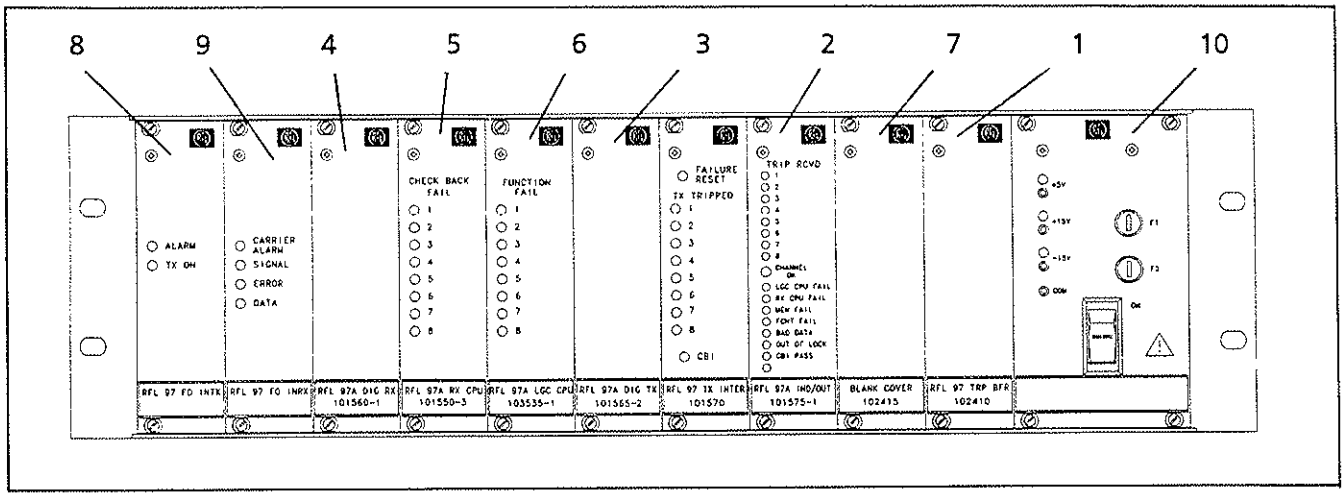


Figure 3-1. Circuit board module locations in typical RFL 9700 terminal

Table 3-1. Circuit board modules in typical RFL 9700 terminal

Item	Description	Control And Indicator Information	Page
1	RFL 97 TRIP BUFFER Trip Buffer Module	No controls or indicators	. . .
2	RFL 97 TX INTER Transmitter Interface Module	Figure 3-2/Table 3-2	3-2
3	RFL 9700 Digital Transmitter Modules	Figure 3-3/Table 3-3	3-3
4	RFL 9700 Digital Receiver Modules	Figure 3-4/Table 3-4	3-4
5	RFL 97A RX CPU Receiver CPU Module	Figure 3-5/Table 3-5	3-5
6	RFL 97A LOGIC CPU Logic CPU Module	Figure 3-6/Table 3-6	3-6
7	RFL 97A IND/OUT Indicator/Output Module	Figure 3-7/Table 3-7	3-7
8	RFL 97 FO INTX Fiber Optic Transmitter Module (optional)	Figure 3-8/Table 3-8	3-8
9	RFL 97 FO INRX Fiber Optic Receiver Module (optional)	Figure 3-9/Table 3-9	3-9
10	RFL 9150A or 9150B 50-watt power supply module	Figure 3-10/Table 3-10	3-10
. . .	RFL 97 INTER Chassis Motherboard	Figure 3-11/Table 3-11	3-11

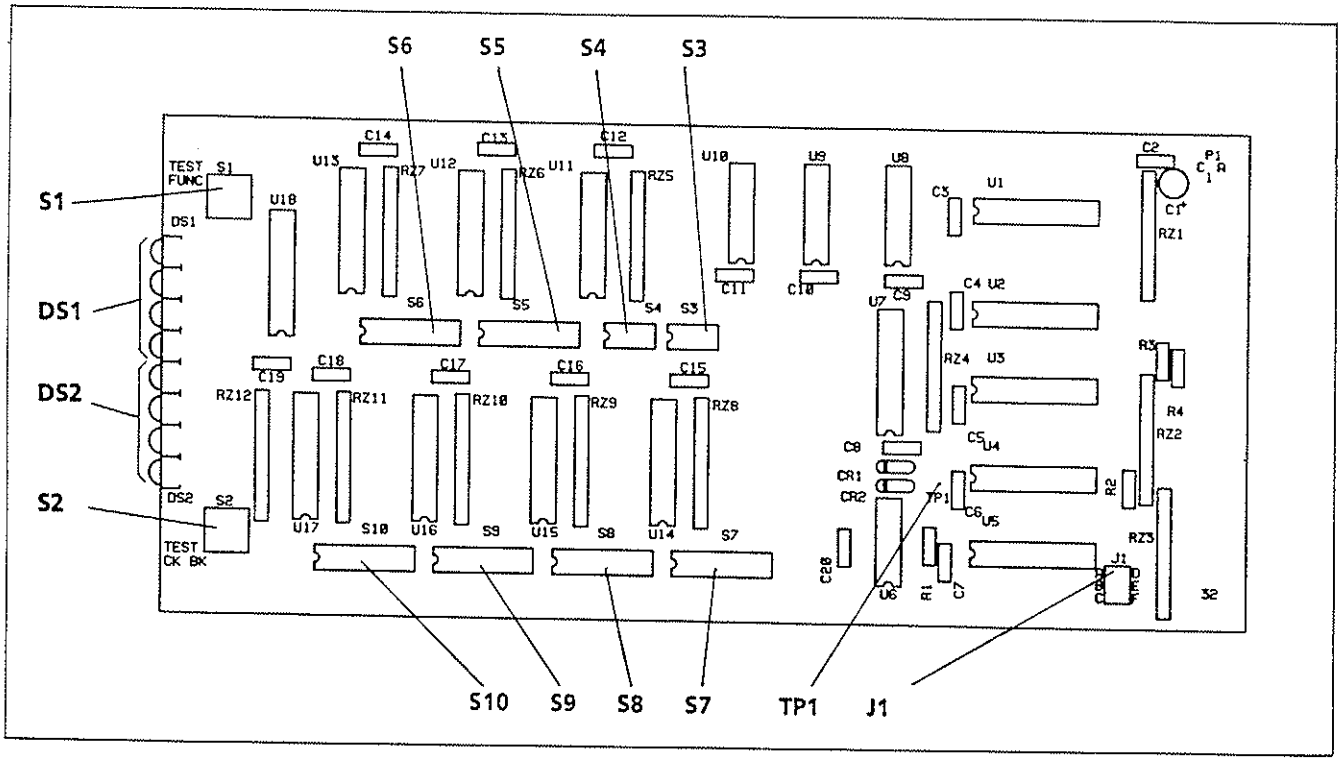


Figure 3-2. Controls and Indicators, RFL 97 TX INTER Transmitter Interface Modules

Table 3-2. Controls and Indicators, RFL 97 TX INTER Transmitter Interface Modules

Symbol	Name/Description	Function
DS1, DS2	TX TRIPPED indicators	Light if any channel is in the trip mode, will light.
J1	Transmitter/Receiver enabling/disabling jumper	Controls the RFL 9700's transmitter and receiver software functions: ABC Controls receiver software functions. (See para 3.3.1a.) DEF Controls transmitter software functions. (See para 3.3.1b.) For proper operation, jumpers should be in Positions A-B and D-E.
S1	FAILURE RESET switch	Manually resets alarm after a checkback or function failure has occurred.
S2	CBI switch	Manually initiates a checkback test.
S3	Unblock DIP switch	Enables/disables unblocking function on Channels 5 through 8. (See para 3.3.1c.)
S4	Trip hold time constant DIP switch	Selects the desired time constant for the trip hold function. (See para 3.3.1d.)
S5	Guard-before-trip DIP switch	Controls guard-before-trip function on all channels. (See para 3.3.1e.)
S6	Trip hold DIP switch	Controls trip hold function on all channels. (See para 3.3.1f.)
S7	Command extend time constant DIP switch	Selects the desired time constant for the command extend function. (See para 3.3.1g.)
S8	Command extend DIP switch	Controls command extend function on all channels. (See para 3.3.1h.)
S9	Echo time constant DIP switch	Selects the desired echo time constant for permissive coordinating. (See para 3.3.1i.)
S10	Current reversal time constant DIP switch	Selects the desired current reversal time constant for permissive coordinating. (See para 3.3.1j.)
TP1	Test turret	Measuring point for the bus test signal.

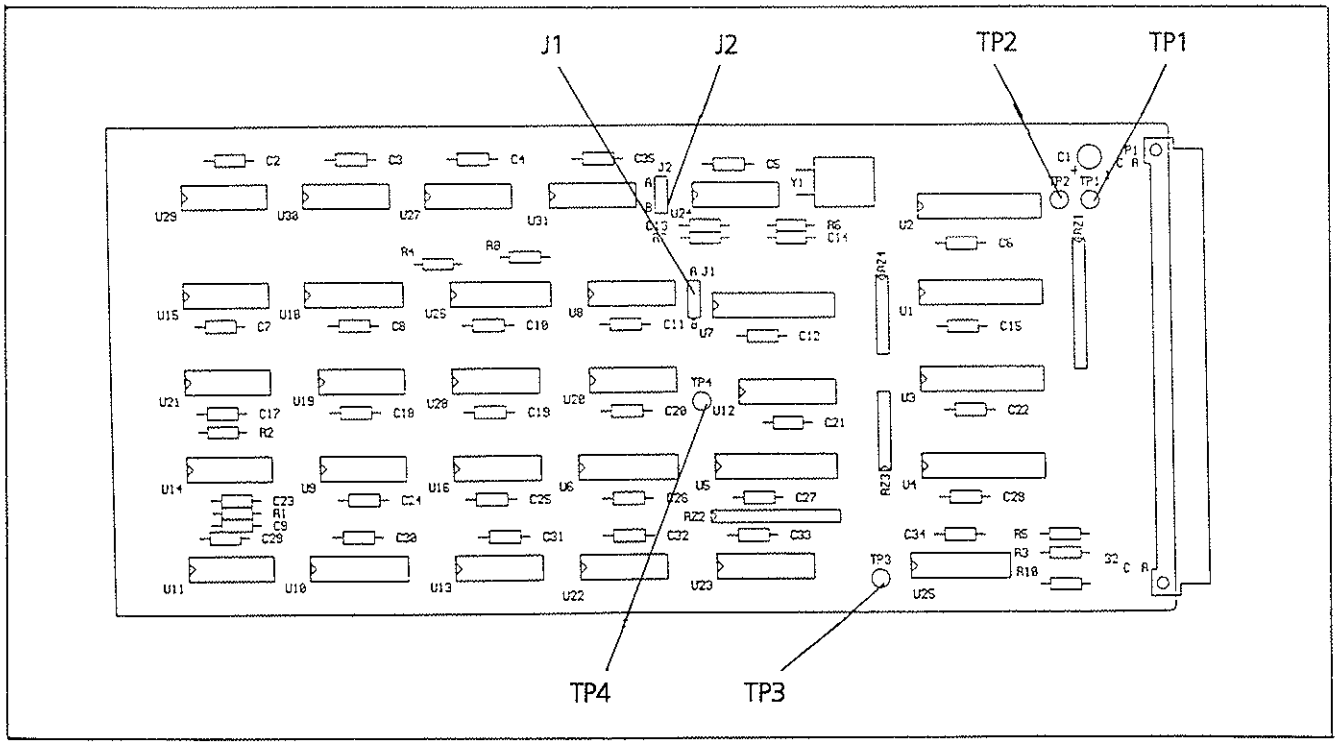


Figure 3-3. Controls and indicators, RFL 9700 digital transmitter modules

Table 3-3. Controls and indicators, RFL 9700 digital transmitter modules

Symbol	Name/Description	Function
J1	Hardware error check jumper	Used for factory testing; must be in Position A for normal operation. (See para 3.3.2a.)
J2	Clock polarity jumper	Inverts clock polarity if required. (See para 3.3.2b.)
TP1	Test turret	Measuring point for +5-volt supply voltage.
TP2	Test turret	Ground reference.
TP3	Test turret	Measuring point for clock signal.
TP4	Test turret	Measuring point for data output signal.

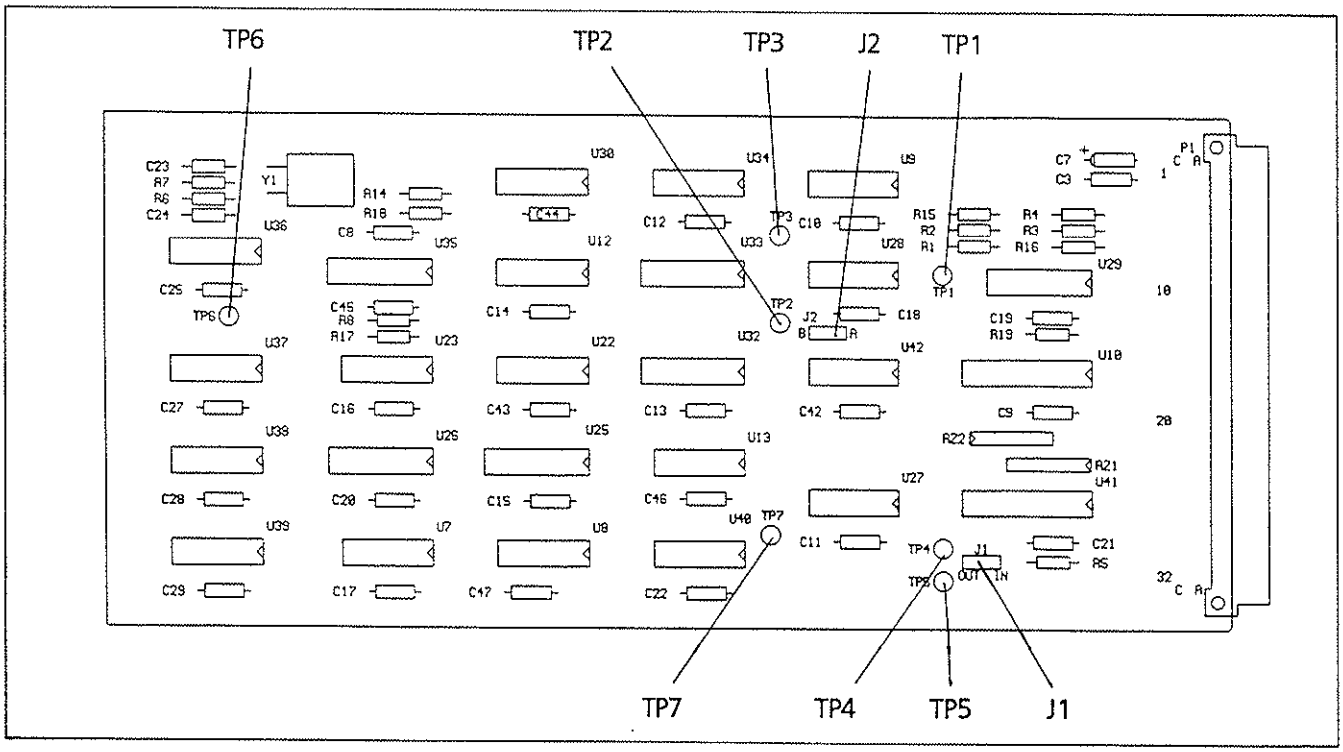


Figure 3-4. Controls and indicators, RFL 9700 digital receiver modules

Table 3-4. Controls and indicators, RFL 9700 digital receiver modules

Symbol	Name/Description	Function
J1	Jumper, IN/OUT	Determines the source of the interrupt pulses used to control the RFL 9700's interrupt-driven software: IN Interrupt pulses generated on the digital receiver module will be used. This position is used if the RFL 9700 is being used as the receiver end of a half-duplex unidirectional system. OUT Interrupt pulses generated on the digital transmitter module will be used. This position is used if the RFL 9700 is being used in a full-duplex system, or as the transmitter end of a half-duplex unidirectional system. See para 3.3.3 for more information.
J2	Clock polarity jumper	Inverts clock polarity if required. (See para 3.3.2b.)
TP1	Test turret	Measuring point for input data stream.
TP2	Test turret	Measuring point for input clock.
TP3	Test turret	Measuring point for framing pulse.
TP4	Test turret	Measuring point for CRC2 test output.
TP5	Test turret	Measuring point for CRC1 test output.
TP6	Test turret	Measuring point for 8-MHz clock output.
TP7	Test turret	Measuring point for frequency discriminator output.

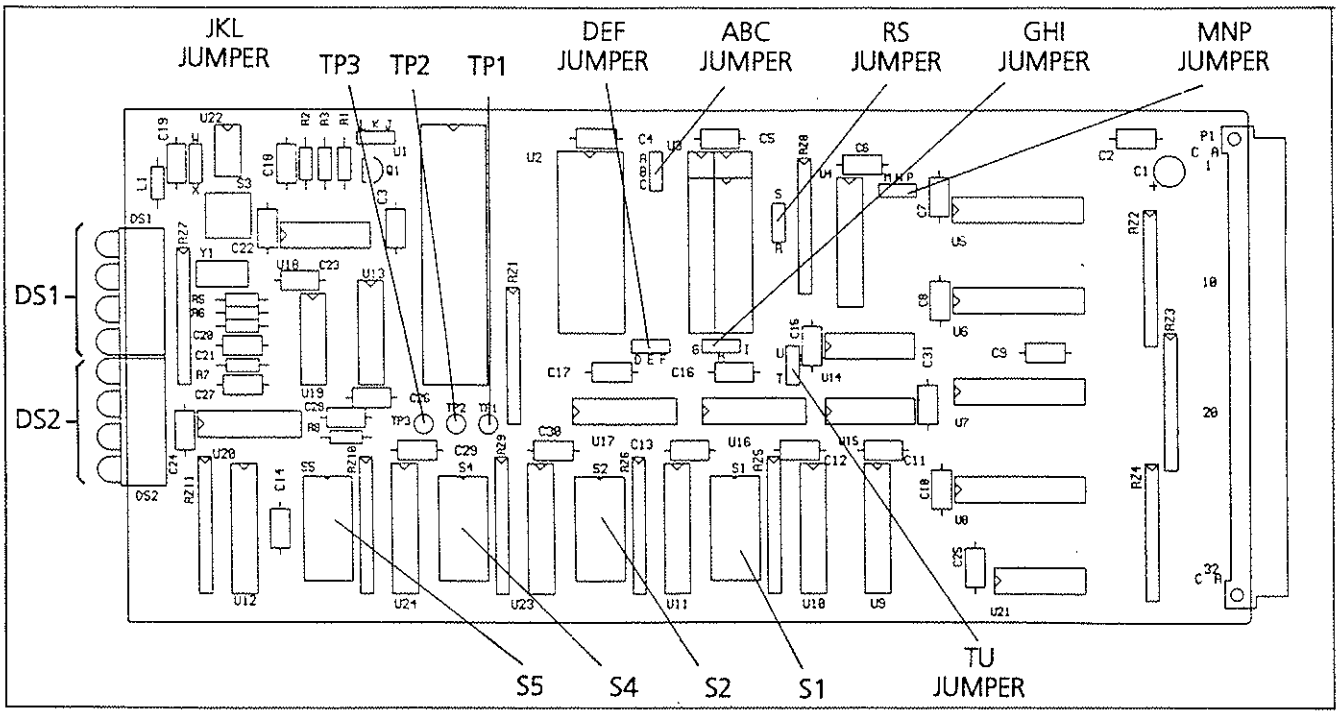


Figure 3-5. Controls and indicators, RFL 97A RX CPU Receiver CPU Module

Table 3-5. Controls and Indicators, RFL 97A RX CPU Receiver CPU Module

Symbol	Name/Description	Function
DS1, DS2	CHECKBACK FAIL indicators	Flash while checkback test is in progress. If any channel fails the checkback test, its indicator will remain lit.
S1, S2	DIP switches	Used to program the desired security and dependability. (See para 3.3.4h.)
S4, S5	DIP switches	Used to set the addressing feature and select the desired operating speed. (See paragraphs 3.3.4i through 3.3.4k.)
ABC	EPROM selection jumper	Set at the factory according to EPROM device being used: A-B 64K or 128K devices. B-C 256K devices.
DEF	EPROM enabling/disabling jumper	Used for factory testing purposes only; place in Position D-E for proper operation.
GHI	Static RAM enabling/disabling jumper	Used for factory testing purposes only; place in Position G-H for proper operation.
JKL	Clock control jumper	Selects clock source for microprocessor: J-K Microprocessor's internal clock will be used. K-L External clock signal will be used.
MNP	Alarm enabling/disabling jumper	Enabled/disabled alarms. Must be placed in Position M-N for proper operation.
RS	Static RAM type selection jumper	Set at the factory according to the type of RAM device being used: R 8K x 8 or 32K x 8 devices. S 2K x 8 devices.
TU	Software checkback selection jumper	Set according to how the receiver CPU module is to signal the logic CPU module: T Receiver CPU will signal the logic CPU when a transmitted address is received from the remote terminal. Must be used when addressing feature is enabled. U Receiver CPU will send CPU ACTIVE signals to the logic CPU. Must be used when addressing feature is disabled. See para 3.3.4g for more information.
TP1	Test turret	Measuring point for CPU RESET line.
TP2	Test turret	Measuring point for INTERRUPT CLEAR line.
TP3	Test turret	Measuring point for CPU ALARM signal.

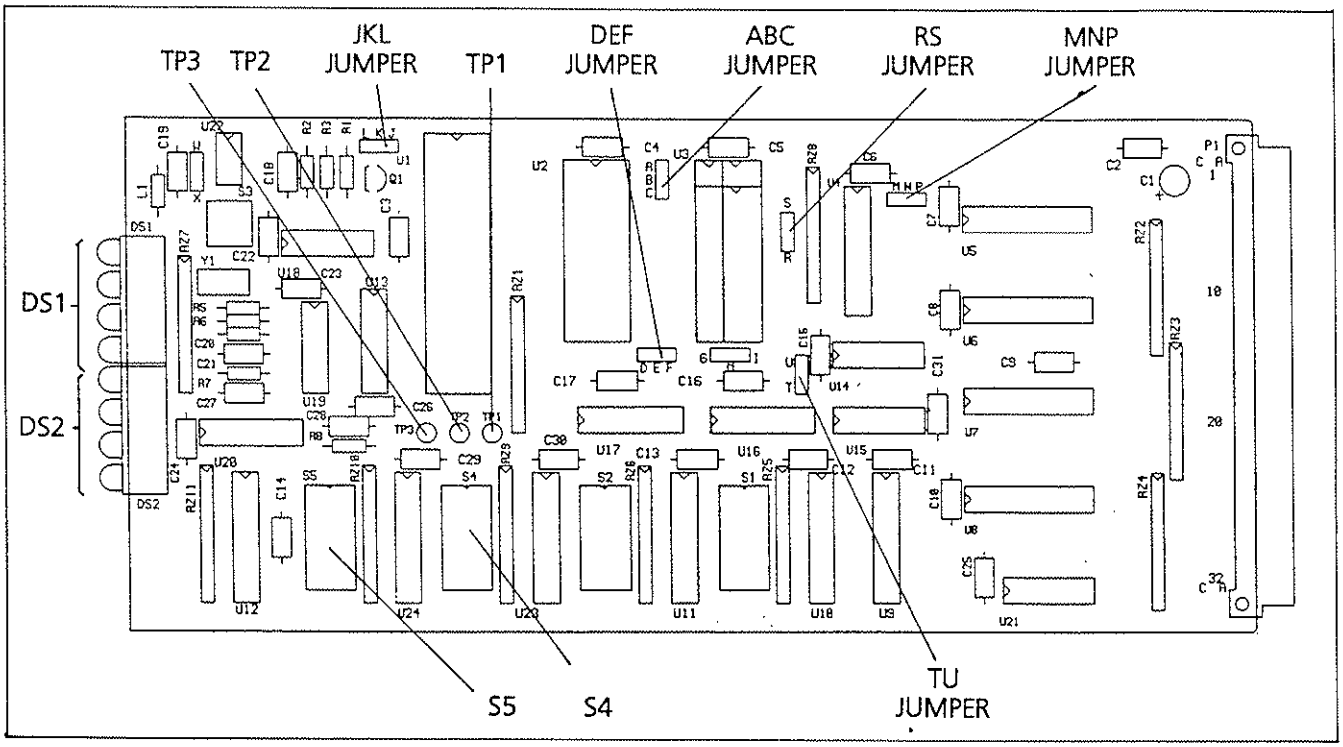


Figure 3-6. Controls and Indicators, RFL 97A LOGIC CPU Logic CPU Module

Table 3-6. Controls and Indicators, RFL 97A LOGIC CPU Logic CPU Module

Symbol	Name/Description	Function
DS1, DS2	FUNCTION FAIL indicators	Off during normal system operation. If any channel fails a diagnostic test, its indicator will remain lit.
S1, S2	DIP switches	Used to program the desired security and dependability. (See para 3.3.4h.)
S4, S5	DIP switches	Used to set the addressing feature and select the desired operating speed. (See paragraphs 3.3.4i through 3.3.4k.)
ABC	EPROM selection jumper	Set at the factory according to EPROM device being used: A-B 64K or 128K devices. B-C 256K devices. See para 3.3.4a for more information.
DEF	EPROM enabling/disabling jumper	Used for factory testing purposes only; place in Position D-E for proper operation.
GHI	Static RAM enabling/disabling jumper	Used for factory testing purposes only; place in Position G-H for proper operation.
JKL	Clock control jumper	Selects clock source for microprocessor: J-K Microprocessor's internal clock will be used. K-L External clock signal will be used.
MNP	Alarm enabling/disabling jumper	Enables/disables alarms. Must be placed in Position N-O for proper operation.
RS	Static RAM type selection jumper	Set at the factory according to the type of RAM device being used: R 8K x 8 or 32K x 8 devices. S 2K x 8 devices. See para 3.3.4f for more information.
TU	Software checkback selection jumper	Must be placed in Position U for proper module operation.
TP1	Test turret	Measuring point for CPU RESET line.
TP2	Test turret	Measuring point for INTERRUPT CLEAR line.
TP3	Test turret	Measuring point for CPU ALARM signal.

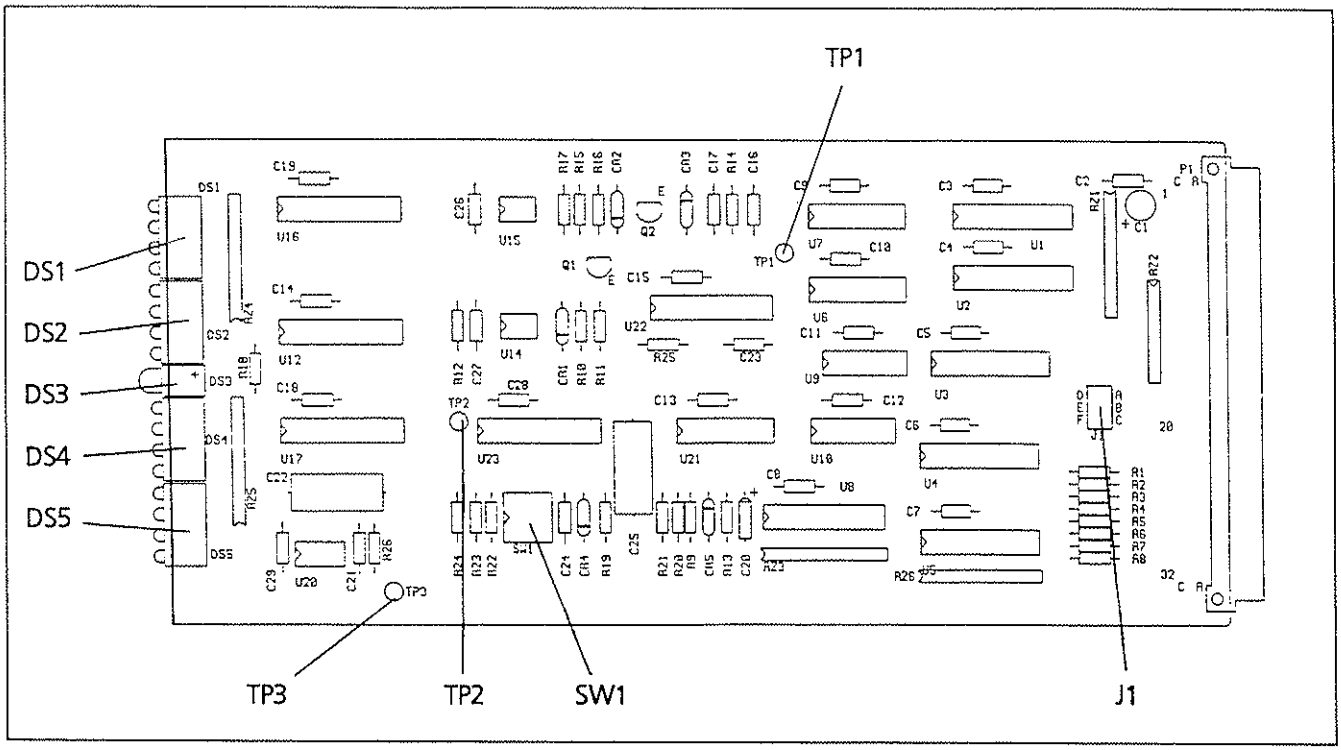


Figure 3-7. Controls and indicators, RFL 97A IND/OUT Indicator/Output Module

Table 3-7. Controls and indicators, RFL 97A IND/OUT Indicator/Output Module

Symbol	Name/Description	Function
DS1, DS2	TRIP RCVD indicators	Off during normal system operation. If a trip is received on any channel, its indicator will light.
DS3	CHANNEL OK indicator	Lights when communications channel is functioning properly (healthy channel).
DS4, DS5	Alarm indicators	Light to indicate what condition has caused the terminal to enter an alarm mode: LOGIC CPU FAIL — A failure detected on the logic CPU module. RX CPU FAIL — A failure detected on the receiver CPU module. MEM FAIL — A MEMORY FAILURE signal has been received from the receiver CPU module. FCTN FAIL — The logic CPU module has detected a function failure. BAD DATA — Invalid CRC data has been received. OUT OF LOCK — A TRANS FAIL* alarm has been received from the receiver CPU module. For more information, see paragraph 3.3.5a.
J1	Configuration jumper	Configures the module for the specific application: A-B, D-E — Phase comparison applications. B-C, E-F — Transfer trip applications.
SW1	Alarm delay DIP switch	Controls the alarm delay function. (See para 3.3.5b.)
TP1	Test turret	Monitoring point for the valid address signal.
TP2	Test turret	Monitoring point for raw communications alarm status; goes high to indicate an alarm state.
TP3	Test turret	Monitoring point for clock signal; a 5-volt square wave between 3886 Hz and 4286 Hz.

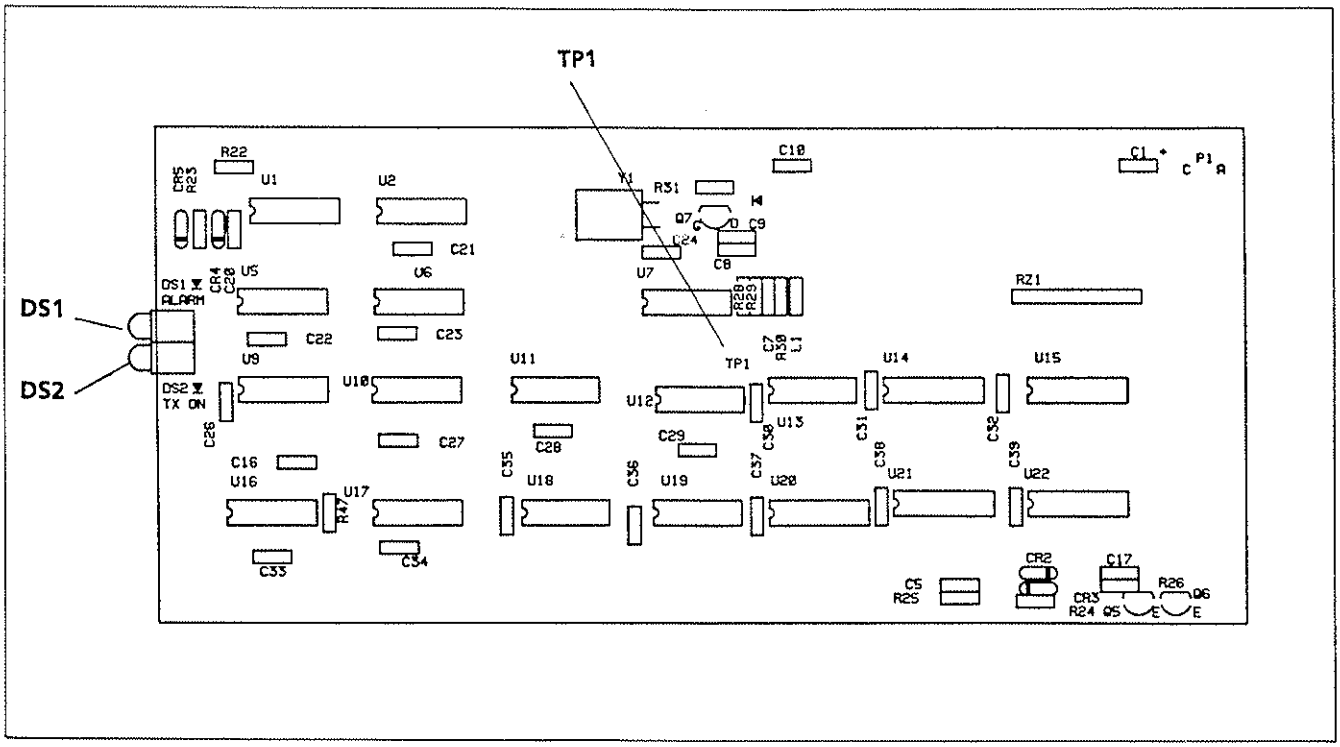


Figure 3-8. Controls and indicators, RFL 97 FO INTX Fiber Optic Transmitter Module

Table 3-8. Controls and indicators, RFL 97 FO INTX Fiber Optic Transmitter Module

Symbol	Name/Description	Function
DS1	ALARM indicator	Lights when an alarm condition has been detected, and the fiber optic head is no longer producing a light signal.
DS2	XMTR ON indicator	Lights when light is being transmitted over the fiber.
TP1	Test turret	Measuring point for the 6.272-MHz clock signal.

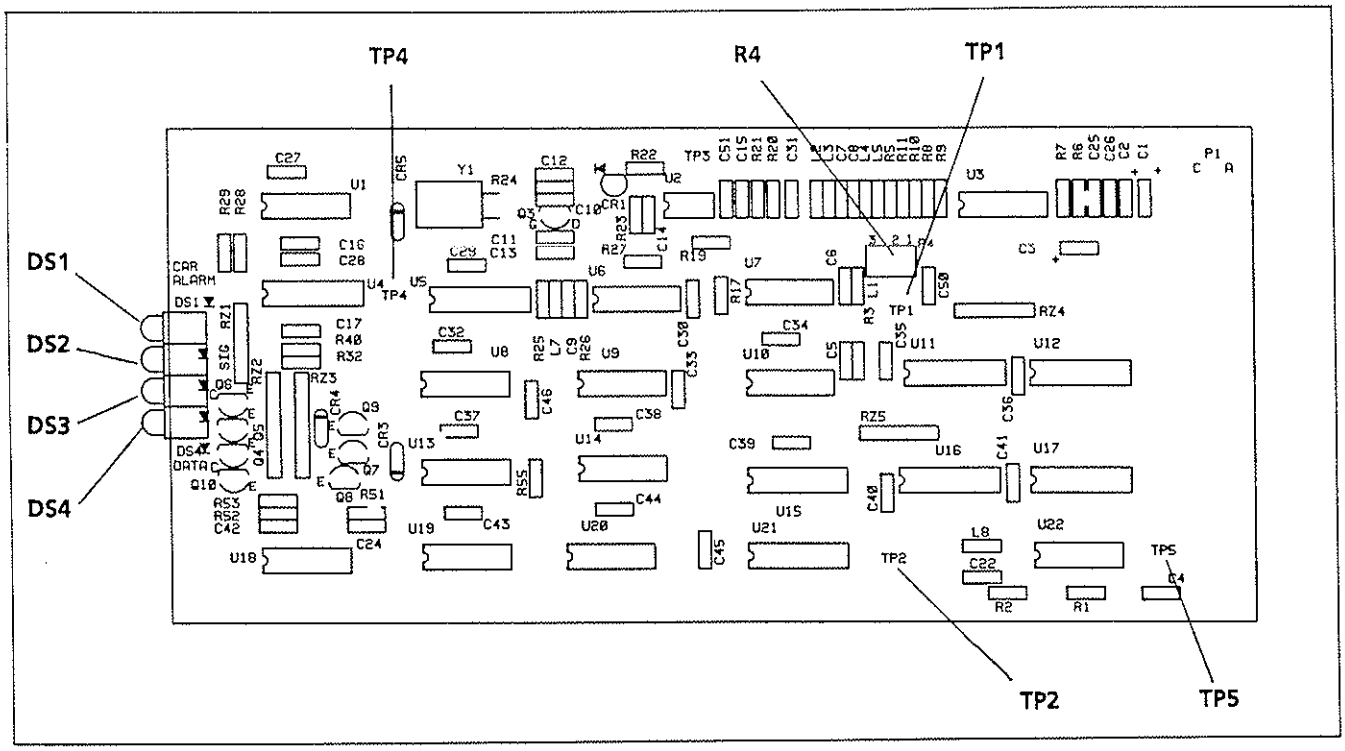


Figure 3-9. Controls and Indicators, RFL 97 FO INRX Fiber Optic Receiver Module

Table 3-9. Controls and Indicators, RFL 97 FO INRX Fiber Optic Receiver Module

Symbol	Name/Description	Function
DS1	CARRIER ALARM indicator, red	Lights when fiber optic carrier is lost.
DS2	SIGNAL indicator, green	Lights when a valid signal is being received.
DS3	ERROR indicator, red	Lights when an error is detected.
DS4	DATA indicator, green	Lights when data is being decoded.
R4	Potentiometer	Sets the threshold voltage for the window comparator.
TP1	Test turret	Monitoring point for demodulated signal.
TP2	Test turret	Ground point.
TP4	Test turret	Monitoring point for the output of the phase-locked loop.
TP5	Test turret	Monitoring point for input signal from fiber optic detector head.

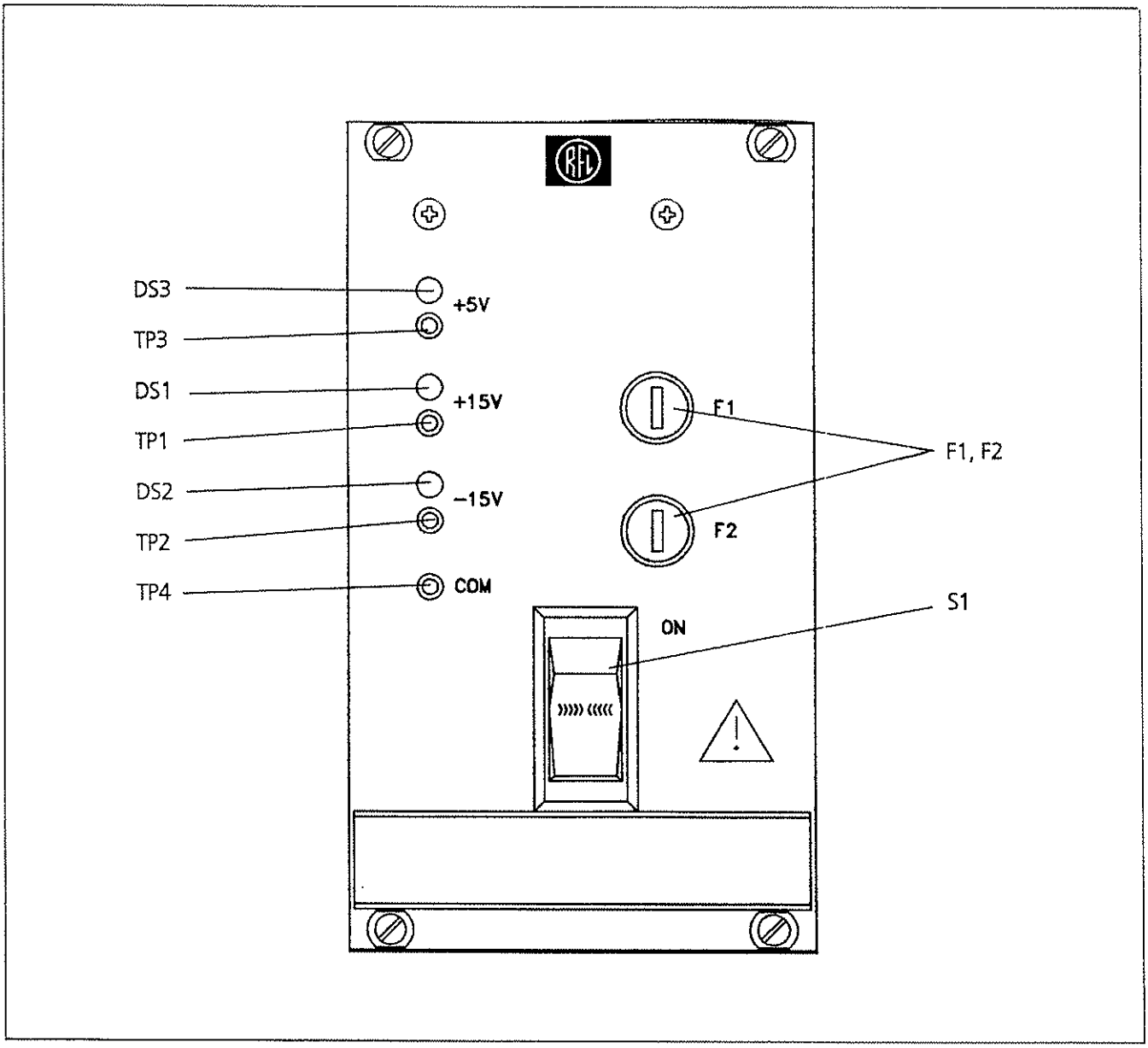


Figure 3-10. Controls and Indicators, RFL 9150A or 9150B 50-watt power supply modules

Table 3-10. Controls and Indicators, RFL 9150A or 9150B 50-watt power supply modules

Symbol	Name/Description	Function
F1,F2	Input fuses	Protect input converter board against excessive input current.
DS1	+15V indicator	Lights when +15-volt supply is functioning.
DS2	-15V indicator	Lights when -15-volt supply is functioning.
DS3	+5V indicator	Lights when +5-volt supply is functioning.
S1	Power switch	Applies input power to the input converter board; serves as power switch for entire chassis.
TP1	+15V test point	Allows output of +15-volt supply to be monitored.
TP2	-15V test point	Allows output of -15-volt supply to be monitored.
TP3	+5V test point	Allows output of +5-volt supply to be monitored.
TP4	COM test point	Ground point.

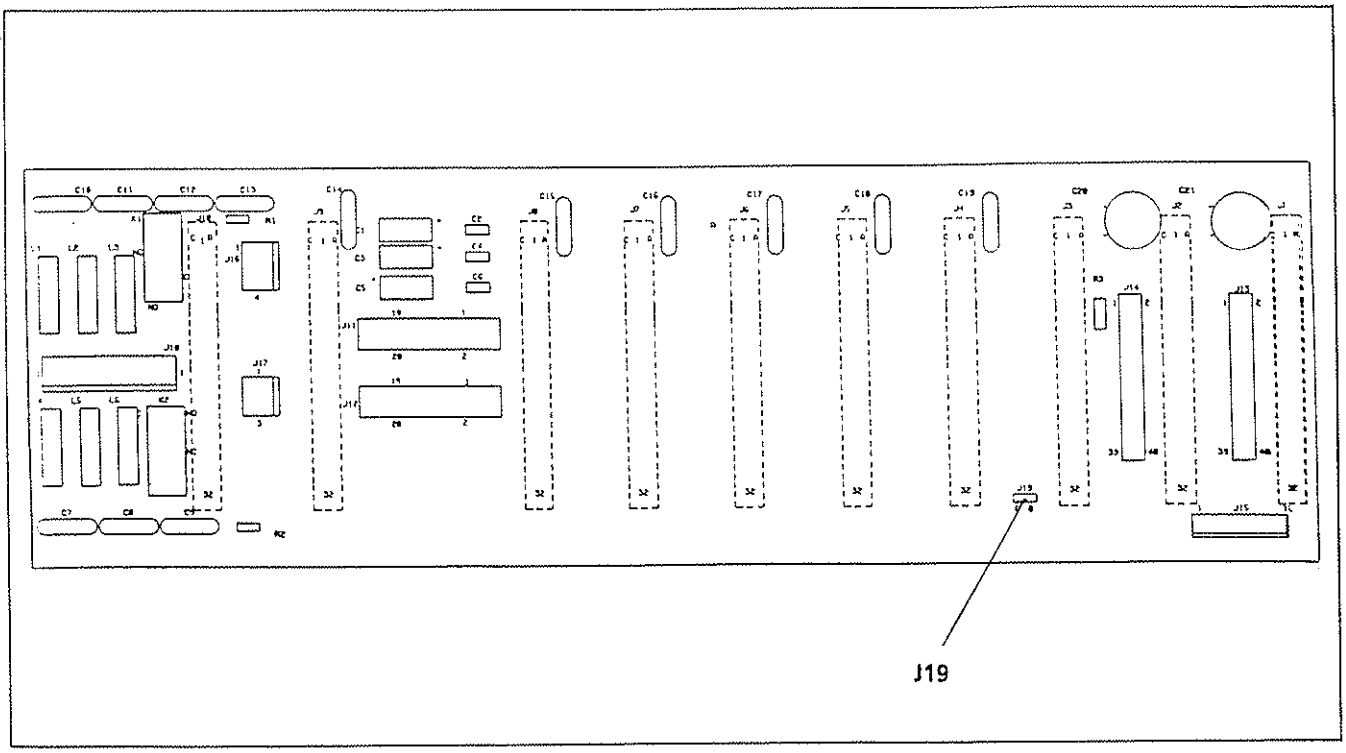


Figure 3-11. Controls and Indicators, RFL 97 INTER Chassis Motherboard

Table 3-11. Controls and Indicators, RFL 97 INTER Chassis Motherboard

Symbol	Name/Description	Function
J19	CARRIER ALARM selection jumper	Controls CARRIER ALARM signal generated by fiber optic receiver module. Must be in Position A if fiber optic receiver module is present. (See para 3.3.6.)

(Text continued from page 3-1)

3.3. JUMPER AND SWITCH SETTINGS

Some RFL 9700 circuit card modules and assemblies are equipped with programmable jumpers and DIP switches. These jumpers and DIP switches must be set before the RFL 9700 can be placed in service.

Paragraphs 3.3.1 through 3.3.6 describe the jumper and switch settings that must be made. Circuit cards modules and assemblies supplied as part of a system have their jumpers and DIP switches set at the factory, according to the EPROM and static RAM devices installed in the modules, the overall system configuration, and the requirements of the specific application. Under normal circumstances, jumpers and DIP switches should only have to be reset in the field if a replacement module is being installed or a change in system configuration is desired.

3.3.1. RFL 97 TX INTER Module

There is a single jumper block on the RFL 97 TX INTER module, labeled "J1." J1 enables or disables the terminal's transmitter and receiver software functions. DIP switches S3 through S10 on the RFL 97 TX INTER control various software functions on the logic CPU module. Figure 3-2 on page 3-2 shows the location of these jumpers and DIP switches.

a. Receiver Enabling/Disabling. The side of J1 labeled "ABC" controls the terminal's receiver software functions. Placing a shorting bar from pin A to pin B (Position A-B) will enable the receiver software; to disable the receiver software, place the shorting bar from pin B to pin C (Position B-C).

If Position A-B is selected, the terminal must contain receiver CPU and digital receiver modules; otherwise, the terminal will not operate. Also, it will not operate if either of these modules are installed and receiver functions are disabled.

b. Transmitter Enabling/Disabling. The side of J1 labeled "DEF" controls the terminal's transmitter software functions. Placing a shorting bar from pin D to pin E (Position D-E) will enable the transmitter software; to disable the transmitter software, place the shorting bar from pin E to pin F (Position E-F).

If Position D-E is selected, the terminal must contain digital transmitter and trip buffer modules; otherwise, the terminal will not operate. Also, it will not operate if both of these modules are installed and transmitter functions are disabled. However, if only one of these modules is missing, the terminal will operate.

c. Unblock Enable/Disable. Unblocking is used in permissive overreaching transfer trip (POTT) applications. When unblock is enabled, a 150-ms unblock trip will be generated on all enabled channels if a communications failure lasting more than 20 ms is detected.

Four-section DIP switch S3 controls the unblock function on Channels 5 through 8; unblock cannot be enabled on Channels 1 through 4. S3-1 controls the unblock function for Channel 5, S3-2 for Channel 6, and so on. To enable unblock, place the switch section in the ON position; if the switch section is placed in the OFF position, unblock is disabled for that channel.

d. Trip Hold Time Constant. Four-section DIP switch S4 selects the time constant for the trip hold function. Only four settings of this switch are valid:

S4-1 ON, all others OFF	50 ms
S4-2 ON, all others OFF	100 ms
S4-3 ON, all others OFF	150 ms
S4-4 ON, all others OFF	200 ms

If more than one section of S4 is placed in the ON position, or if all sections are placed in the OFF position, a default trip hold value of 100 ms will be used.

e. Guard-Before-Trip. Guard-before-trip is a logic condition, that requires that a valid guard signal be received for a minimum amount of time before a trip can be recognized as valid. This is done to reduce the possibility of false trips.

Eight-section DIP switch S5 controls the guard-before-trip function on all eight channels. S5-1 controls the guard-before-trip function for Channel 1, S5-2 controls Channel 2, and so on. To enable guard-before-trip, place the switch section in the ON position; if the switch section is placed in the OFF position, guard-before-trip is disabled for that channel.

f. Trip Hold. Eight-section DIP switch S6 controls the trip hold function on all eight channels. When trip hold is enabled, the digital receiver module's trip output is held high for a fixed amount of time, even if the trip condition ceases to exist.

S6-1 controls trip hold for Channel 1, S6-2 for Channel 2, and so on. To enable trip hold, place the switch section in the ON position; if the switch section is placed in the OFF position, trip hold is disabled for that channel.

g. Command Extend Time Constant. Eight-section DIP switch S7 selects the time constant for the command extend function. A binary value is assigned to each section of S7:

S7-1	1 ms
S7-2	2 ms
S7-3	4 ms
S7-4	8 ms
S7-5	16 ms
S7-6	32 ms
S7-7	64 ms
S7-8	Do not use - leave in OFF position.

To set S7, convert the desired time to a binary number. Once this is done, set S7 as required so the ON sections equal ones and the OFF sections equal zeroes. If a binary value greater than 100 is programmed into S7, a default command extend value of 50 ms will be used.

Example:

Desired Time Constant	75 ms
Converted To Binary Value	01001011
Switch Settings:	

Switch	Value	Setting
S7-1	1	ON
S7-2	2	ON
S7-3	4	OFF
S7-4	8	ON
S7-5	16	OFF
S7-6	32	OFF
S7-7	64	ON
S7-8	. . .	OFF

h. Command Extend. Eight-section DIP switch S8 controls the command extend function on all eight channels. When command extend is enabled, the digital transmitter module's trip output is held high for a fixed amount of time, even if the trip condition ceases to exist.

S8-1 controls command extend for Channel 1, S8-2 for Channel 2, and so on. To enable command extend, place the switch section in the ON position; if the switch section is placed in the OFF position, command extend is disabled for that channel.

i. Permissive Coordinating. DIP switches S9 and S10 are only set if your RFL 9700 terminal is equipped with the optional permissive coordinating software. If this software is not present, these switches will be ignored.

NOTE

1. When an RFL 9700 is equipped with permissive coordinating software, one permissive coordinating function is available on rear-panel terminal blocks TB5 and TB6. A second permissive coordinating function is available on rear-panel terinal blocks TB7 and TB8.

2. If the RFL 9700 is equipped for eight functions (two RFL 97 I/O modules), direct transfer trip functions will only be active on Channels 1 and 2, and the unblock and combinational logic functions will not be available on any channel.

3. The ability to combine trip input signals using combinational logic functions is an available software option. If your RFL 9700 has this feature, supplementary instructions will be furnished describing its use.

4. Differential phase protection for Channels 1 and 2 can be enabled by jumper settings on the RFL 97A IND/OUT module (para 3.3.5). If differential phase protection is selected for Channels 1 and 2, any other functions selected for these channels will be ignored.

(a) Echo Time Constant. Eight-section DIP switch S9 selects the echo time constant used in permissive coordinating. A binary value is assigned to each section of S9:

S9-1	1 ms
S9-2	2 ms
S9-3	4 ms
S9-4	8 ms
S9-5	16 ms
S9-6	32 ms
S9-7	64 ms
S9-8	128 ms

The echo time constant can be set to any value between 30 ms and 285 ms (the setting of S9 plus a 30-ms offset). To set the desired echo time constant, subtract 30 from the desired time constant and convert the result to a binary number. Set S9 as required so the ON sections equal ones and the OFF sections equal zeroes in the binary number.

Example:

Desired Time Constant	250 ms
Minus 30-ms Offset	220
Converted To Binary Value	11011100

Switch Settings:

Switch	Value	Setting
S9-1	1	OFF
S9-2	2	OFF
S9-3	4	ON
S9-4	8	ON
S9-5	16	ON
S9-6	32	OFF
S9-7	64	ON
S9-8	128	ON

(b) Current Reversal Time Constant. Eight-section DIP switch S10 selects the current reversal time constant used in permissive coordinating. A binary value is assigned to each section of S10:

S10-1	1 ms
S10-2	2 ms
S10-3	4 ms
S10-4	8 ms
S10-5	16 ms
S10-6	32 ms
S10-7	Do not use - leave in OFF position.
S10-8	Do not use - leave in OFF position.

To set the current reversal time constant, convert the desired time constant to a binary number. Set S10 as required so the ON sections equal ones and the OFF sections equal zeroes in the binary number. If the binary number programmed into S10 is less than 5, the time constant will default to 5 ms. If the number is higher than 50, a 25-ms default value will be used.

Example:

Desired Time Constant	40 ms
Binary Value	00101000

Switch Settings:

Switch	Value	Setting
S10-1	1	OFF
S10-2	2	OFF
S10-3	4	OFF
S10-4	8	ON
S10-5	16	OFF
S10-6	32	ON
S10-7	. . .	OFF
S10-8	. . .	OFF

3.3.2. Digital Transmitter Module

There are two two-position jumpers on RFL 97A DIG TX 56 and RFL 97A DIG TX 64 digital transmitter module, labeled "J1" and "J2." (See Figure 3-3 on page 3-3 for location.)

a. Hardware Error Check Control. Jumper J1 controls the digital transmitter module's hardware error check feature. Position A enables this feature, and Position B disables it. J1 must be in Position A (error check enabled) for normal system operation. Position B (error check disabled) is used for factory testing only.

b. Clock Signal Polarity. Jumper J2 controls the polarity of the digital transmitter module's clock signal. Position A selects normal polarity, and Position B selects inverted polarity. In most installations, J2 will be placed in Position A; if tests indicate that the clock polarity needs to be reversed, place J2 in Position B. (See the "RS-449 Or X.21 Signal Verification" procedure in paragraph 3.4.6 on page 3-23 for further information.)

3.3.3. Digital Receiver Modules

There are two two-position jumpers on each RFL 9700 digital receiver module, labeled "J1" and "J2." (See Figure 3-4 on page 3-4 for location.)

a. Interrupt Pulse Source Selction. Jumper J1 determines the source of the interrupt pulses used to control the RFL 9700 interrupt-driven software. When J1 is in the OUT position, the interrupt strobe is supplied by the digital transmitter module. This position is used if the RFL 9700 is being used in a full-duplex communications system, or as the transmitter end of a half-duplex unidirectional system.

When J1 is in the IN position, the interrupt strobe is generated on the digital receiver module module itself. This position is used if the RFL 9700 is being used as the receiver end of a half-duplex unidirectional system.

b. Clock Signal Polarity. Jumper J2 controls the polarity of the digital receiver module's clock signal. Position A selects normal polarity, and Position B selects inverted polarity. In most installations, J2 will be placed in Position A; if tests indicate that the clock polarity needs to be reversed, place J2 in Position B. (See the "RS-449 Or X21 Signal Verification" procedure in paragraph 3.4.6 on page 3-23 for further information.)

3.3.4. CPU Modules

There are two CPU modules in each RFL 9700 terminal: an RFL 97A RX CPU Receiver CPU Module and an RFL 97A LOGIC CPU Logic CPU Module. Each CPU module has seven programmable jumpers. RFL 97A RX CPU modules have four DIP switches, and RFL 97A LOGIC CPU modules have two DIP switches. Figure 3-5 on page 3-5 and Figure 3-6 on page 3-6 show the location of these jumpers and switches.

a. EPROM Selection. Jumper ABC is set at the factory according to the EPROM device installed on the CPU module. If a 64K (27C64) or 128K (27C128) device is installed, place this jumper in Position A-B; use Position B-C for 256K (27C256) devices.

b. EPROM Enabling/Disabling. Jumper DEF controls the EPROM Enable line. Position D-E connects the Enable line to the EPROM; this is the position used for normal operation. Position E-F disconnects the EPROM Enable line, and forces all of its data output lines into their high-impedance state. This position is used for testing purposes only.

c. Static RAM Enabling/Disabling. Jumper GHI controls the static RAM's Enable line. Position G-H connects the Enable line to the static RAM; this is the position used for normal operation. Position H-I disconnects the static RAM's Enable line, and forces all of its data output lines into their high-impedance state. This position is used for testing purposes only.

d. Microprocessor Clock Control. Jumper JKL controls the CPU module's internal microprocessor clock. Position J-K enables the clock; this is the position used for normal operation. If an external clock signal is being used to run the microprocessor, place this jumper in Position K-L.

e. Alarm Enabling/Disabling. Jumper MNP determines whether carrier alarm signals received from the fiber optic receiver module will be used to control the status latch READY line.

On RFL 97A RX CPU modules, this jumper must be placed in Position M-N for proper operation. When it is, an active CARRIER ALARM signal will disable the output contact latch and place the status latch READY signal in the NOT READY condition (logic high).

On RFL 97A LOGIC CPU modules, this jumper must be placed in Position N-P. When it is, an active CARRIER ALARM signal cannot interfere with the operation of the output contact latch or the READY line.

f. Static RAM Type Selection. Jumper RS is set at the factory according to the static RAM device installed on the CPU module. Position R is used for 8K x 8 or 32K x 8 devices; Position S is used for 2K x 8 devices.

The rows of pins on the static RAM device can be either 0.3 inches (7.6 mm) or 0.6 inches (15.2 mm) apart; the circuit board is designed to accommodate both pin spacings. If a 24-pin, 2K x 8 device is being used, it should be justified to the bottom of the 28-pin socket. (In other words, pins 1, 2, 27, and 28 should be left open.)

g. Software Checkback Enabling/Disabling. Jumper TU controls the CPU module's software checkback scheme. It has two positions: "T" and "U." Position T allows the RFL 97A RX CPU module to signal the logic CPU module that a transmitted address has been received; this position should be used when the RFL 9700's addressing feature is being used. Position U allows the RFL 97A RX CPU module to send CPU ACTIVE signals to the logic CPU module; this position should be used when the RFL 9700's addressing feature is not being used.

On RFL 97A LOGIC CPU modules, this jumper must be placed in Position U.

h. Security/Dependability Programming. DIP switches S1 and S2 on the RFL 97A RX CPU module are used to program the desired security and dependability for the terminal. (On the RFL 97A LOGIC CPU module, S1 and S2 are not fitted.) The security and dependability of each channel can be independently programmed, as shown in Table 3-12.

i. Address Selection. The first six sections of DIP switches S4 and S5 are used to set the address used by the RFL 9700's addressing feature. The receiver address is set on the receiver CPU module, and the transmit address is set on the logic CPU module. S4-1 through S4-6 set the lower six bits of the address. The upper six bits are set by S5-1 through S5-6.

S4 and S5 are configured so that ON equals logic zero and OFF equals logic one. To set the address to "110000 001010," for example, the switches would be set as follows:

Switch	Setting	Switch	Setting
S4-1	ON	S5-1	ON
S4-2	OFF	S5-2	ON
S4-3	ON	S5-3	ON
S4-4	OFF	S5-4	ON
S4-5	ON	S5-5	OFF
S4-6	ON	S5-6	OFF

Table 3-12. Security and dependability programming, RFL 97A RX CPU Receiver CPU Module

Ch. #	Switch And Position	Very Dependable	Dependable	Secure	Very Secure
1	S2-1	ON	OFF	ON	OFF
	S2-2	ON	ON	OFF	OFF
2	S2-3	ON	OFF	ON	OFF
	S2-4	ON	ON	OFF	OFF
3	S2-5	ON	OFF	ON	OFF
	S2-6	ON	ON	OFF	OFF
4	S2-7	ON	OFF	ON	OFF
	S2-8	ON	ON	OFF	OFF
5	S1-1	ON	OFF	ON	OFF
	S1-2	ON	ON	OFF	OFF
6	S1-3	ON	OFF	ON	OFF
	S1-4	ON	ON	OFF	OFF
7	S1-5	ON	OFF	ON	OFF
	S1-6	ON	ON	OFF	OFF
8	S1-7	ON	OFF	ON	OFF
	S1-8	ON	ON	OFF	OFF

j. Address Enabling/Disabling. DIP switch S4-7 controls whether the RFL 9700's addressing feature is used. Place S4-7 in the ON position to enable addressing; if the addressing feature is not being used, place S4-7 in the OFF position.

k. Operating Speed Selection. DIP switch S4-8 must be set according to the terminal operating speed. Place S4-8 in the ON position if the terminal is equipped with RFL 97A DIG TX 64 and RFL 97A DIG RX 64 modules; this will set the transmit and receive logic for 64-Kbps operation. If the terminal is equipped with RFL 97A DIG TX 56 and RFL 97A DIG RX 56 modules, place S4-8 in the OFF position; this will set the logic for 56-Kbps operation.

3.3.5. RFL 97A IND/OUT Module

There is a single jumper block on the RFL 97A IND/OUT module labeled "J1," and a four-section DIP switch labeled "SW1." (See Figure 3-7 on page 3-7 for location.)

a. Application Selection. Jumper block J1 is set according to the type of application where the RFL 9700 is being used. If the RFL 9700 is being used in a phase comparison application, the side of J1 labeled "ABC" is placed in Position A-B and the side labeled "DEF" is

placed in Position D-E. If the RFL 9700 is being used in a transfer trip application, J1 is to be set in Positions B-C and E-F.

b. Delay Circuit Programming. DIP switch SW1 programs the communications alarm delay circuit. It selects the delay time, enables and disabled the delay circuit, and determines which output alarms will be subject to the delay.

SW1-1 and 1-2 select the delay time:

Delay Time	SW1-1	SW1-2
125 ms	ON	ON
500 ms	OFF	ON
1 sec	ON	OFF
2 sec	OFF	OFF

SW1-3 controls the alarm delay function. To enable the function (add a delay), place SW1-3 in the ON position. To disable it (no added delay), place SW1-3 in the OFF position.

SW1-4 determines which alarm outputs are subject to the delay set by SW1-1 and SW1-2. When SW1-4 is placed in the ON position, non-fatal alarm outputs are not subject to the delay but fatal alarms are delayed. To delay all alarm outputs (fatal and non-fatal), place SW1-4 in the OFF position.

3.3.6. RFL 97 INTER Chassis Motherboard

There is a single jumper on the RFL 97 INTER chassis motherboard, labeled "J19." (For location, see Figure 3-11 on page 3-11 of this section.) J19 controls the CARRIER ALARM signal generated by the fiber optic receiver module. If your RFL 9700 is equipped with a fiber optic receiver module, place this jumper in Position A; place it in Position B if the RFL 9700 does not contain a fiber optic receiver module.

3.4. INITIAL STARTUP AND SYSTEM VERIFICATION PROCEDURES

All RFL 9700 terminals are checked and adjusted at the factory. Once all electrical connections and jumper settings have been made, the terminals at each end of the communication line should be checked for proper operation. To do this, an operator must be at each terminal, and the operators must be in contact with each other, either by telephone, PLC voice channel, or similar means.

The following procedures can be used to check the RFL 9700 terminals at each end of a communications line for proper operation, either at time of installation or any time system operation needs to be verified. Perform all steps in each procedure in the order presented. Expected results or comments are indented and appear in **boldface** type.

3.4.1. Equipment Requirements

The following equipment will be required to perform the initial startup procedures:

1. Digital multimeter, 3 1/2-digit with test leads; Fluke Model 8010A or equivalent.

2. Optical power meter; Photodyne Model 22XL or equivalent (for terminals equipped with fiber optic modules only). If meter has interchangeable sensor heads, select the proper head for the wavelength being used (850 nm or 1300 nm).

3. Regulated dc power supply, 0 to 50 volts, 0 to 0.2 amps; Hewlett-Packard Model 6218C or equivalent (only required for unidirectional transmit-only terminals).

4. Pushbutton switch, SPDT momentary contact with hand-held housing; Switchcraft Type E913 or equivalent (for unidirectional transmit-only terminals).

5. Hook-up wire for connecting power supply and switch to transmitting terminal (for unidirectional transmit-only terminals).

CAUTION

To prevent damage to the multimeter, the input voltage being fed to the power supply must be known before attempting to perform the following procedure.

3.4.2. Power Supply Output Verification

RFL 9700 terminals require three regulated voltages for proper operation: +5 volts, +15 volts, and -15 volts. These voltages are obtained from an RFL 9150A or RFL9150B power supply module mounted inside the RFL 9700 chassis. Because the power supply outputs cannot be adjusted, this procedure will only verify

whether or not the power supply is working. Perform the following procedure at both terminals.

1. Remove the protective cover from the rear of the chassis by pulling it out of the standoffs holding it in place.

2. Check all terminal block mounting screws on the RFL 97 I/O for tightness.

   Mounting screws should be checked every time the protective cover is removed. Loose terminal block mounting screws can result in compromised surge withstand capabilities (SWC), leading to component damage.

3. Set the multimeter for dc voltage measurements. Set the multimeter range control as required to produce a reading that does not force the multimeter to overrange.

4. At terminal block TB9 on the rear panel, measure the input supply voltage by connecting the positive multimeter lead to terminal TB9-3, and the negative lead to terminal TB9-2. Note the multimeter indication.

   The multimeter indication must be within the following limits:

   24-Vdc Terminals - 19.2 to 28.8 volts
   48-Vdc Terminals - 38.4 to 57.6 volts
   125-Vdc Terminals - 100 to 150 volts
   250-Vdc Terminals - 200 to 300 volts
   110-Vac Terminals - 99 to 121 volts
   220-Vac Terminals - 198 to 242 volts

   The power supply may not be able to produce enough power to operate the terminal with input voltages below these limits; voltages above these limits may result in damage to the power supply.

5. Disconnect the multimeter from terminal block TB9.

6. Set the multimeter for dc voltage measurements, on a range that will produce 15-volt readings without over-ranging.

7. Turn on the power supply by placing the POWER switch in the ON position.

8. Connect the negative multimeter lead to the COM test point on the front of the power supply; connect the positive multimeter lead to the +5V test point. Note the multimeter indication.

   The multimeter indication should be between 4.75 and 5.25 volts.

9. Move the positive meter lead to the +15V test point on the front of the power supply. Note the multimeter indication.

   The multimeter indication should be between +14.25 and +15.75 volts.

10. Move the positive meter lead to the -15V test point on the front of the power supply. Note the multimeter indication.

    The multimeter indication should be between -14.25 and -15.25 volts.

11. Turn off the power supply by placing the POWER switch in the OFF position.

If the above procedure can be successfully completed at both terminals, the power supplies are functioning properly. If not, refer to the fuse replacement procedures in Section 4 before proceeding with paragraph 3.4.3. If fuse replacement does not correct the problem, either replace or troubleshoot the power supply before proceeding to paragraph 3.4.3.

NOTE

During communications link verification, the terminal that initiates a function is called the "local" terminal; the other terminal is the "remote" terminal. In bi-directional systems, either terminal can initiate functions, so either can be the local. In unidirectional systems, the transmitting terminal is always the local, and the receiving terminal is always the remote.

3.4.3. Communications Link Verification

The following procedures will test the communications link between two RFL 9700 terminals. Before attempting the following procedures, all jumpers and switches on all modules at both terminals must be properly set. (Refer to paragraph 3.3 on page 3-11 for further information.) In addition, the operators at each terminal must be able to talk with each other.

Two different communications link verification procedures are provided below: one for fiber optic communications links, and one for RS-449 or X.21 links.

a. Fiber Optic Link Verification. To verify a fiber optic communications link, proceed as follows:

1. Make sure both RFL 9700 terminals contain the proper module complement. (See Table 1-2 in Section 1 for further information.)

2. Make sure both terminals are turned off (the power switches on the power supply modules in the OFF position).

3. Designate one terminal the local terminal; if its protective cover is in place over the rear panel, remove it by pulling the cover out of the standoffs holding it in place.

4. Temporarily disconnect the local terminal from the communications medium by disconnecting the fiber optic cables from their mating connectors on the fiber optic heads.

6. At both terminals, place the main power switch on the power supply module in the ON position.
   The following indicators must be lit at both terminals:
   a. **All four indicators on the power supply module.**
   b. **TX ON indicator DS2 on the fiber optic transmitter module.**
   c. **CARRIER ALARM indicator DS1 and ERROR indicator DS3 on the fiber optic receiver module.**
   d. **The BAD DATA and OUT OF LOCK indicators on the RFL 97A IND/OUT module.**

7. At the local terminal, press the CBI (checkback initiate) switch on the RFL 97 TX INTER module.
   The FUNCTION FAIL indicator on the local terminal's RFL 97A IND/OUT module must light.

8. At the local terminal, press the FAILURE RESET switch on the RFL 97 TX INTER module.
   The FUNCTION FAIL indicator will go out.

9. Turn off the local terminal by placing the power switch on the power supply module in the OFF position.
   All indicators will go out.

10. Reconnect the local terminal to the communications medium by inserting the fiber optic cables into their mating connectors on the fiber optic heads.

11. Line up the mounting holes in the rear panel protective cover with the standoffs on the rear of the local terminal, and push down on the protective cover until it is secured in place.

12. Turn the local terminal back on by placing the main power switch on the power supply module in the ON position.
   If the communications link is functioning properly, the following indicators will be lit at both terminals:
   a. **All four indicators on the power supply module.**
   b. **The TX ON indicator on the fiber optic transmitter module.**
   c. **The SIGNAL and DATA indicators on the fiber optic receiver module.**
   d. **The CHANNEL OK indicator on the RFL 97A IND/OUT module.**

   All other indicators must be off.

13. If your system is bi-directional, repeat steps 1 through 12, initiating all tests at the other terminal.

b. RS-449 or X.21 Link Verification. To verify an RS-449 or CCITT X.21 communications link, proceed as follows:

1. Make sure both RFL 9700 terminals contain the proper module complement. (See Table 1-2 in Section 1 for further information.)

2. Make sure both terminals are turned off (the power switches on the power supply modules in the OFF position).

3. Designate one terminal the local terminal; if its protective cover is in place over the rear panel, remove it by pulling the cover out of the standoffs holding it in place.

4. Temporarily disconnect the local terminal from the communications medium by disconnecting the RS-449 or X.21 connector from its mating connector on the interface panel.

6. At both terminals, place the main power switch on the power supply module in the ON position.

   The following indicators must be lit at both terminals:

   a. All four indicators on the power supply module.

   b. The LOGIC CPU FAIL, OUT OF LOCK, and RX CPU FAIL indicators on the RFL 97A IND/OUT module.

7. At the local terminal, press the CBI (checkback initiate) switch on the RFL 97 TX INTER module.

   The FUNCTION FAIL indicator on the local terminal's RFL 97A IND/OUT module must light.

8. At the local terminal, press the FAILURE RESET switch on the RFL 97 TX INTER module.

   The FUNCTION FAIL indicator will go out.

9. Turn off the local terminal by placing the power switch on the power supply module in the OFF position.

   All indicators will go out.

10. Reconnect the local terminal to the communications medium by inserting the RS-449 or X.21 connector into its mating connector on the interface panel.

11. Line up the mounting holes in the rear panel protective cover with the standoffs on the rear of the local terminal, and push down on the protective cover until it is secured in place.

12. Turn the local terminal back on by placing the main power switch on the power supply module in the ON position.

    If the communications link is functioning properly, all four indicators on the power supply module and the CHANNEL OK indicator on the RFL 97A IND/OUT module will be lit; all other indicators must be off.

13. If your system is bi-directional, repeat steps 1 through 12, initiating all tests at the other terminal.

If the above steps can be successfully completed, the communications link between both terminals is functioning properly. If there appears to be a problem with the communications link and both terminals are equipped with fiber optic modules, perform the fiber optic signal level verification procedure in paragraph 3.4.5 to make sure there is enough light being passed over the fiber optic cable.

If the light levels are within limits or the terminals do not contain fiber optic modules, refer to Section 2 and check all connections at both terminals to be sure they were properly made. Once this is done, repeat the above procedure. If it still cannot be successfully completed, refer to Section 4 (Maintenance).

If the RFL 9700's addressing feature is enabled and the OUT OF LOCK indicator on the indicator/output module is lit, make sure the addresses set by S4 and S5 on the CPU modules in both terminals match. The remote terminal's logic CPU and the local terminal's receiver CPU must be set for the same address. In addition, the local terminal's logic CPU and the remote terminal's receiver CPU must also be set for the same address.

When checking the address settings, make sure jumper TU has been properly set. This jumper must be in Position U on both logic CPU modules; if the addressing feature is being used, it should be in Position T on both receiver CPU modules.

3.4.4. Verification Procedures

The following procedures are used to verify terminal operation. They can be performed when the system is first put into operation, or anytime its operation needs to be verified. Before attempting the procedures in this paragraph, one of the communications link verification procedures in paragraph 3.4.3 must be successfully completed. Perform all steps in the order presented. Expected results and/or comments are indented and appear in **boldface** type.

a. Bi-Directional Systems. The terminals in bi-directional systems are verified by using the RFL 9700's checkback test feature. This will verify that the RFL 9700 terminals at both ends of the communications medium are functioning properly. It also checks the integrity of the link between the terminals. In case of a test failure, the indicators on the front panels can be used to determine where the failure occurred.

During checkback testing, the terminal that initiates the checkback test is called the "transmitting" terminal. The terminal that responds to the transmitting terminal's checkback request is called the "receiving" terminal. An operator must be at each terminal during the checkback test, to manually initiate the test and monitor the front panel indicators. The operators should be in contact with each other, by telephone, voice channel, radio, or similar means.

The checkback test is started when the operator at the transmitting terminal presses the CBI (checkback initiate) switch on the RFL 97 TX INTER module. This causes the transmitting terminal to signal the receiving terminal to test itself. The receiving terminal will start its self-test routine, checking each channel for proper operation. When it is finished, it will tell the transmitting terminal to test itself. The transmitting terminal then goes into an identical self-test routine, checking all of its channels in order.

During the checkback test, the operators at both terminal should watch the front-panel indicators. If the system is functioning properly, the CHECKBACK FAIL indicators on both terminals should light in turn; the indicator for Channel 1 should light for about 4/10 second and go out, followed by the indicators for Channels 2, 3, and so on. This is referred to as a "normal flash sequence."

Once the test has been completed, each operator should note the status of the indicators on the front of their RFL 9700. These indicators show the test results. Refer to Table 3-13 to interpret their meaning.

If both terminals pass the checkback test, they are ready for continuous service. If one or more CHECKBACK FAIL indicators remains lit, this may indicate a problem in one of the RFL 97A RX CPU processor modules. Refer to Section 4 (Maintenance) for further instructions.

b. Unidirectional Systems. Unidirectional systems contain at least one transmit-only RFL 9700 terminal, and one receive-only terminal. These systems are tested by forcing the transmitting terminal to trip, and checking to make sure the trip is detected at the receiving terminal.

1. Turn off both terminals by placing the power switches on the power supply modules in the OFF position.

2. Remove the protective cover from the rear of the transmitting terminal by pulling the cover out of the standoffs holding it in place.

3. Disconnect the FCTN KEY + and FCTN KEY - leads from TB1-5 and TB1-6 on the transmitting terminal's RFL 97 I/O input/output module.

4. Connect the regulated power supply and the pushbutton switch to the transmitting terminal, as shown in Figure 3-12.

   Make sure the power supply is turned off while making connections.

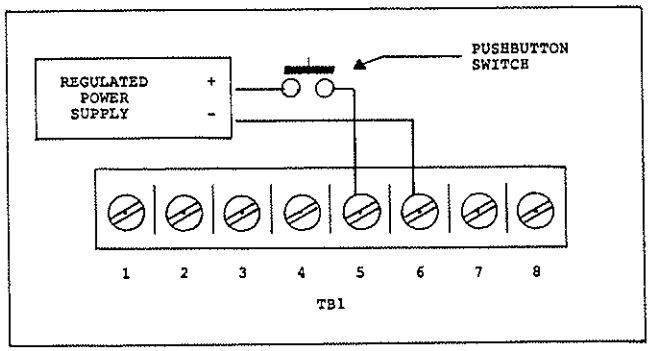


Figure 3-12. Connecting an external power supply and trip switch to the transmitting terminal in a unidirectional system

5. Turn on the regulated power supply, and set its controls for an output of 48 volts.

6. Remove the protective cover from the rear of the receiving terminal by pulling the cover out of the standoffs holding it in place.

7. Disconnect the TRIP + and TRIP - leads from TB1-3 and TB1-4 on the receiving terminal's RFL 97 I/O input/output module.

8. At the transmitting terminal, press and hold the pushbutton switch.

   At the transmitting terminal, the TX TRIPPED 1 indicator on the transmitter interface module (97 TX INTER) should light, meaning that Channel 1 has tripped.

   At the receiving terminal, the TRIP RCVD 1 indicator should light, meaning that Channel 1 has received the trip sent by the transmitting terminal.

Table 3-13. Interpreting checkback test results in bi-directional systems

Transmitting Terminal Conditions	Receiving Terminal Conditions	Test Status
1. Normal flash sequence. 2. FUNCTION FAIL indicator OFF.	1. Normal flash sequence. 2. FUNCTION FAIL indicator OFF.	Both channels have passed the checkback test.
1. No flash sequence. 2. FUNCTION FAIL indicator ON.	1. No flash sequence. 2. FUNCTION FAIL indicator OFF.	The checkback signal never reached the receiving terminal. This is probably due to noise on the line; wait ten seconds and try again.
1. No flash sequence. 2. FUNCTION FAIL indicator ON.	1. Normal flash sequence. 2. FUNCTION FAIL indicator OFF.	The receiving terminal passed the checkback test, but the return signal telling the transmitting terminal to initiate the test was lost, probably due to transmission noise.
1. No flash sequence. 2. FUNCTION FAIL indicator ON.	1. One or more CHECKBACK FAIL indicators remain lit after flash sequence. 2. FUNCTION FAIL indicator ON.	The receiving terminal failed the checkback test, and no testing was done at the transmitting terminal.
1. One or more CHECKBACK FAIL indicators remain lit after flash sequence. 2. FUNCTION FAIL indicator ON.	1. Normal flash sequence. 2. FUNCTION FAIL indicator OFF.	The receiving terminal passed the checkback test, but the indicated channel(s) failed at the transmitting terminal.

9. Release the pushbutton switch.

   At the transmitting terminal, the TX TRIPPED 1 indicator on the RFL 97 TX INTER module will go out, meaning that the trip has been removed from Channel 1. At the receiving terminal, the TRIP RCVD 1 indicator will go out, meaning that Channel 1 is no longer receiving a trip from the transmitting terminal.

10. Turn off both terminals by placing the power switches on the power supply modules in the OFF position.

11. Turn off the regulated power supply, and disconnect it and the pushbutton switch from the transmitting terminal.

12. Reconnect the FCTN KEY + lead to TB1-5 on the transmitting terminal's RFL 97 I/O input/output module; reconnect the FCTN KEY - lead to TB1-6.

13. Line up the mounting holes in the rear panel protective cover with the standoffs on the rear of the transmitting terminal, and push down on the protective cover until it is secured in place.

14. Reconnect the TRIP + lead to TB1-3 on the receiving terminal's RFL 97 I/O input/output module; reconnect the TRIP - lead to TB1-4.

15. Line up the mounting holes in the rear panel protective cover with the standoffs on the rear of the receiving terminal, and push down on the protective cover until it is secured in place.

If the above procedure can be successfully completed, the RFL 9700 system is working properly. Turn both terminals back on, and they will be ready for continuous service. If the procedure cannot be completed, or if a malfunction is suspected, go to Section 4 (Maintenance).

NOTE

The following procedure can only be performed on terminals equipped with fiber optic modules. If your terminal is equipped with an RS-449 or CCITT X.21 interface panel, go on to paragraph 3.4.6.

3.4.5. Fiber Optic Signal Level Verification

The RFL 9700 fiber optic modules and fiber optic heads contain no field-adjustable components. The following procedures verify their operation by measuring outgoing and incoming light levels with a photometer.

At bi-directional terminals (terminals that both transmit and receive), the outgoing and incoming light levels must both be checked. The outgoing light level must be checked at all transmit-only terminals, and the incoming light level must be checked at all receive-only terminals.

All light signal levels given in this procedure are dBm average. The minimum signal levels listed in this procedure are 3 dB below the specified values for each emitter and detector head. This 3-dB difference compensates for the 50-percent duty cycle used in the RFL 9700 system.

WARNING

RFL 97 FO TX-13LS FIBER OPTIC EMITTER HEADS USE A LASER LIGHT SOURCE THAT PRODUCES INVISIBLE RADIATION. STARING DIRECTLY INTO THE LIGHT BEAM MAY RESULT IN EYE DAMAGE AND/OR BLINDNESS. NEVER LOOK DIRECTLY INTO THE LIGHT BEAM AND BE CAREFUL NOT TO SHINE THE LIGHT AGAINST ANY REFLECTIVE SURFACE.

THE RFL 97 FO TX-13LS'S LASER SOURCE IS A CLASS IIIb LASER PRODUCT, USING GALLIUM INDIUM ARSENIDE PHOSPHIDE. ITS RECOMMENDED MAXIMUM POWER OUTPUT IS 7 mW. IT COMPLIES WITH APPLICABLE DHHS STANDARDS UNDER THE RADIATION CONTROL FOR HEALTH AND SAFETY ACT OF 1968.

a. Outgoing Light Level Check. To check the output of a fiber optic emitter head, proceed as follows:

1. Disconnect the outgoing fiber optic cable from its mating connector on the emitter head.

2. Connect the photometer input cable to the emitter head output connector and note the photometer indication.

   The photometer indication will vary according to the head being used:

RFL 97 FO TX-8M	**-21 dBm**
RFL 97 FO TX-13M	**-16 dBm**
RFL 97 FO TX-13S	**-30 dBm**
RFL 97 FO TX-13LS	**-10 dBm**

3. Disconnect the photometer from the emitter head.

4. Reconnect the outgoing fiber optic cable to the emitter head.

If the proper light levels are obtained, the fiber optic transmitter module and the fiber optic emitter head are functioning properly. If not, replace or troubleshoot the fiber optic transmitter module and/or the fiber optic emitter head. (See Sections 4, 13, and 15.)

b. Incoming Light Level Check. To check the amount of light being applied to a fiber optic detector head, proceed as follows:

1. Disconnect the incoming fiber optic cable from its mating connector on the detector head.

2. Connect the photometer input cable to the end of the incoming fiber optic cable and note the photometer indication.

   The incoming light level will vary according to the heads being used at both terminals and the system losses encountered. The photometer indication will vary according to the head being used:

   For RFL 97 FO RX-8M Heads
   -51 dBm to -21 dBm

   For All 1300nm And 1500nm Heads
   -51 dBm to -30 dBm

   -30 dBm is the maximum light input level permitted for 1300nm or 1500nm heads. If the photometer indication is greater than -30 dBm, attenuation must be added.)

3. Disconnect the photometer from the incoming fiber optic cable.

4. Reconnect the incoming fiber optic cable to the detector head.

If the light level is within limits, the fiber optic receiver module and the fiber optic detector head should be able to function properly. If the light level is below the minimum listed in step 2 above, the fiber optic cable may be defective. Determine the cause of the problem before proceeding.

NOTE

The following procedure can only be performed on RFL 9700 terminals equipped with RS-449 or X.21 interface panels. If your terminal is equipped with fiber optic modules and heads, go on to paragraph 3.5

3.4.6. RS-449 Or X.21 Signal Verification

RFL 9700 terminals equipped with RS-449 or X.21 interface panels clock data into their digital receiver modules on the positive-going edge of the clock signal. The relationship between the clock and data pulses should be check for proper polarity before placing the terminal in service.

To check the clock and data signals, proceed as follows:

1. Place the POWER switch on the power supply module in the OFF position.

2. Using a flat-blade screwdriver, turn the two quarter-turn fasteners on the front panel of the digital receiver module (97A DIG RX 56 or 97A DIG RX 64) counterclockwise until they are loose.

3. Grab the handle on the front of the digital receiver module, and pull until the module is out of the chassis.

4. Line up the edges of the card extender with the card guides in the chassis slot vacated by the digital receiver module, and slide the card extender into the chassis until it is firmly seated.

5. Plug the digital receiver module into the card extender.

6. Place the POWER switch on the power supply module in the ON position.

7. Connect an oscilloscope probe from the oscilloscope's Channel 1 vertical input to test point TP1 on the digital receiver module.

   Channel 1 will be monitoring the data signal.

8. Connect another oscilloscope probe from the oscilloscope's Channel 2 vertical input to test point TP2 on the digital receiver module.

   Channel 2 will be monitoring the clock signal.

9. Connect the ground leads from both oscilloscope probes to any convenient chassis ground point.

10. Set the oscilloscope controls for dual-channel operation, with the Channel 2 input used as the triggering source. Adjust the vertical and horizontal controls for a clean display on the oscilloscope screen.

11. Looking at the oscilloscope screen, note when the data signal (Channel 1) changes state, with respect to the clock signal (Channel 2).

    The data signal should not change state at the same time the clock signal goes positive. If it does, reverse the polarity of the incoming clock with respect to the incoming data.

    Jumper J2 on the digital receiver module controls the polarity of the clock signal. Place J2 in Position A for normal polarity, or Position B for inverted polarity.

    Once the clock polarity has been reversed, repeat step 11; if the data no longer changes state at the same time the clock signal goes positive, go on to step 12.

12. Disconnect the oscilloscope probes from the digital receiver module.

13. Place the POWER switch on the power supply module in the OFF position.

14. Remove the digital receiver module from the card extender, and pull the card extender out of the chassis.

15. Line up the edges of the digital receiver module circuit board with the card guides in the chassis slot vacated by the card extender.

16. Slide the digital receiver module into the chassis until it is firmly seated and its front panel is against the horizontal rails at the front of the chassis.

17. Using a flat-blade screwdriver, turn the two captive screws on the front panel of the digital receiver module fully clockwise to secure it in place.

18. Using a flat-blade screwdriver, turn the two quarter-turn fasteners on the front panel of the digital transmitter module (97A DIG TX 56 or 97A DIG TX 64) counterclockwise until they are loose.

19. Grab the handle on the front of the digital transmitter module, and pull until the module is out of the chassis.

20. Line up the edges of the card extender with the card guides in the chassis slot vacated by the digital transmitter module, and slide the card extender into the chassis until it is firmly seated.

21. Plug the digital transmitter module into the card extender.

22. Place the POWER switch on the power supply module in the ON position.

23. Connect an oscilloscope probe from the oscilloscope's Channel 1 vertical input to test point TP4 on the digital transmitter module.

    Channel 1 will be monitoring the data signal.

24. Connect another oscilloscope probe from the oscilloscope's Channel 2 vertical input to test point TP3 on the digital transmitter module.

    Channel 2 will be monitoring the clock signal.

25. Connect the ground leads from both oscilloscope probes to test point TP2.

26. Set the oscilloscope controls for dual-channel operation, with the Channel 2 input used as the triggering source. Adjust the vertical and horizontal controls for a clean display on the oscilloscope screen.

27. Looking at the oscilloscope screen, note when the data signal (Channel 1) changes state, with respect to the clock signal (Channel 2).

    The data signal should not change state at the same time the clock signal goes positive. If it does, reverse the polarity of the incoming clock with respect to the incoming data.

    Jumper J2 on the digital transmitter module controls the polarity of the clock signal. Place J2 in Position A for normal polarity, or Position B for inverted polarity.

    Once the clock polarity has been reversed, repeat step 27; if the data no longer changes state at the same time the clock signal goes positive, go on to step 28.

28. Disconnect the oscilloscope probes from the digital transmitter module.

29. Place the POWER switch on the power supply module in the OFF position.

30. Remove the digital transmitter module from the card extender, and pull the card extender out of the chassis.

31. Line up the edges of the digital transmitter module circuit board with the card guides in the chassis slot vacated by the card extender.

32. Slide the digital transmitter module into the chassis until it is firmly seated and its front panel is against the horizontal rails at the front of the chassis.

33. Using a flat-blade screwdriver, turn the two captive screws on the front panel of the digital transmitter module fully clockwise to secure it in place.

34. Place the POWER switch on the power supply module in the ON position.

3.5. SYSTEM OPERATION

Once the initial startup procedures have been performed on the RFL 9700 terminals at both ends of the communications link, they are ready for continuous operation. The following paragraphs briefly describe how the RFL 9700 system operates. More detailed information can be found in the theories of operation for the individual circuit card modules. These theories of operation appear in Sections 5 through 16 of this manual.

The RFL 9700 system comprises two parts: an eight-input digital link, and a multi-function programmable logic section. A cyclic redundancy check (CRC) is incorporated into the digital transmission to achieve a high level of security. The status of the eight protective relaying inputs is continuously transmitted to the receiving end. A six-bit CRC word is also sent to the receiving end. A fifteenth bit is used as a transmission synchronizing bit. The synchronizing bit is high with one word and low with the next; this alternation is uniquely detectable, as no other bit in the transmitted data has this characteristic.

Figure 3-13 shows the transmission order of the data. The eight data bits are sent first, followed by the CRC bits and the synchronizing bit. Because the data transmission is continuous (no start or stop bits), the actual order of the bit stream is not important; the synchronizing bit can be either be considered the first bit in the transmission, or the last.

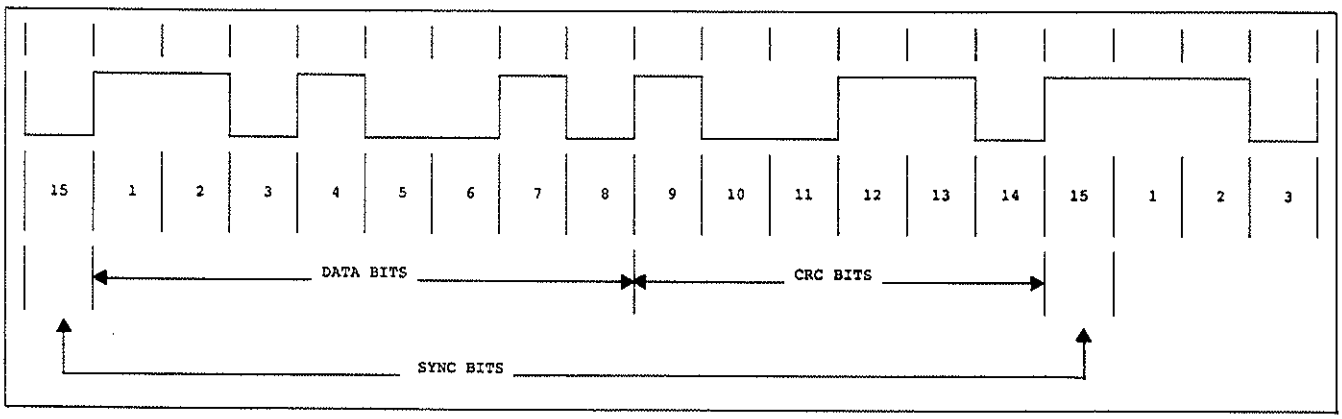


Figure 3-13. Transmission data format, RFL 9700 Digital Protection Channel

Because the data transmission is continuous, the received data is framed in relation to the sync bit. The data transmission technique used does not contain start or stop bits, because they are not effective with static data; too much time would be required to achieve synchronization. If the system achieves a false lock on two of the data bits, the static nature of the data will not allow resynchronization until the state of one of the bits changes. Because of this, a single synchronizing bit is provided that changes state with each data word.

The eight data bits are limited to limited changes of state; a bit that changes state cannot change state again for about 2 ms. This is permissible in protective relaying applications, and would typically be done to de-bounce relay and switch contacts. Only the synchronizing bit can change state each transmission; any change of state in a data bit will result in the bit remaining static for at least 2 ms. This will prevent false lock on data bits. CRC bits can change sooner than once every 2 ms if a change in data occurs on a different channel.

Each digital input can be individually programmed to select the degree of security and dependability. This is achieved by modifying the acceptance criteria for the generation of a trip output. Enhanced security will result in longer system response times.The received digital data is applied to a shift register that is controlled by a local clock. The data is stored and analyzed in a 16-stage shift register. An Exclusive-OR gate is used to detect the presence of the synchronizing bit by sampling the first and last stages of the 16-stage shift register.

A digital edge detector automatically centers the received data pulses, relative to the internal sampling clock. The edge detector also tracks differences in the transmitter and receiver clock frequencies, bias distortion due to the transmission medium, and other distortions.

Error checking and signal quality analysis is performed by a CRC check. Any received transmission with a valid CRC code will be accepted as a valid transmission; if the system has been programmed for the fastest response time, a trip output will occur. Slower response times will require more than one valid transmission to be accepted before a trip output occurs. This lengthens the response time, but results in greater security. The number of correct CRC codes is used to indicate received signal quality and whether the system is synchronized.

To enhance CRC checking, every other data bit is inverted. In a system where all eight inputs are inactive (the normal quiescent state), this will prevent all ones from being transmitted. A data transmission with an overabundance of one logic state is undesirable, though not catastrophic. The inversion of the data bits minimizes the likelihood of this occurrence.

Section 4. MAINTENANCE

WARNING

HAZARDOUS VOLTAGES CAN BE PRESENT INSIDE THE RFL 9700 SYSTEM. BEFORE ATTEMPTING MAINTENANCE, BE SURE TO READ AND COMPLY WITH THE HIGH VOLTAGE WARNING AND SAFETY SUMMARY INFORMATION ON PAGES iii AND iv OF THIS MANUAL.

ALL RFL 9700 TERMINALS ARE EQUIPPED WITH A PROTECTIVE COVER THAT EXTENDS ACROSS THE REAR OF THE CHASSIS. THIS COVER IS INTENDED TO PROTECT THE OPERATOR FROM POTENTIALLY HAZARDOUS VOLTAGES, WHICH MAY BE PRESENT ON THE 97 I/O INTERFACE ASSEMBLY'S TERMINAL BLOCKS. THIS COVER MUST ONLY BE REMOVED BY QUALIFIED SERVICE PERSONNEL WHEN ACCESS TO THE REAR PANEL IS REQUIRED. IT MUST BE REPLACED BEFORE PLACING THE RFL 9700 IN SERVICE.

CAUTION

Whenever the protective cover is removed from the rear of the chassis, check all terminal block mounting screws for tightness. Loose terminal block mounting screws can result in compromised surge withstand capabilities (SWC), leading to component damage.

4.1. INTRODUCTION

This section provides maintenance instructions for the RFL 9700 Digital Protective Relaying Channel. Topics discussed include removal and replacement procedures and corrective maintenance information. Information is also provided on how to arrange for service by RFL personnel.

CAUTION

Each module position in the RFL 9700 chassis is dedicated to a specific module type, as indicated by a label along the front of the chassis. Modules can suffer component damage if they are installed in the wrong chassis slot. When removing and replacing modules, use the label in the chassis as a guide to make sure each module is in the proper slot.

4.2. REMOVAL AND REPLACEMENT

Paragraphs 4.2.1 through 4.2.4 provide procedures to be used when removing and replacing RFL 9700 modules and I/O assemblies.

4.2.1. Plug-In Modules

All plug-in modules mounted at the front of the RFL 9700 are held in place by two quarter-turn fasteners. To remove any of these modules, proceed as follows:

1. Place the POWER switch on the power supply module in the OFF position.
2. Using a flat-blade screwdriver, turn the two quarter-turn fasteners on the front panel of the module counterclockwise, until they are loose.
3. Grab the handle on the front of the module and pull until the module is out of the chassis.

To replace the module, proceed as follows:

1. Using the label along the front of the chassis as a guide, determine the slot in the chassis where the module is to be installed.
2. Line up the edges of the module circuit board with the card guides in the chassis.

3. Slide the module into the chassis until it is firmly seated and its front panel is against the horizontal rails at the front of the chassis.

4. Using a flat-blade screwdriver, turn the two captive screws on the front panel of the module fully clockwise to secure it in place.

5. Place the POWER switch on the power supply module in the ON position.

4.2.2. Fiber Optic Heads

Two fiber optic heads are mounted at the rear of all RFL 9700 terminals equipped with fiber optic modules. Each head is held in place with two quarter-turn fasteners. To remove a fiber optic head, proceed as follows:

1. Place the POWER switch on the power supply module in the OFF position.

2. Remove the protective cover from the rear panel by pulling it out of the standoffs holding it in place.

3. Disconnect the fiber optic cable from its mating connector on the fiber optic head.

4. Using a flat-blade screwdriver, turn the two quarter-turn fasteners on the panel of the fiber optic head counterclockwise, until they are loose.

5. Grab the connector on the panel of the fiber optic head and gently pull until the head is out of the chassis.

To replace a fiber optic head, proceed as follows:

1. Determine the slot in the chassis where the fiber optic head is to be installed.

   RFL 97 FO TX emitter heads are installed in the right-hand slot in the rear panel, as viewed from the rear of the chassis. RFL 97 FO RX** detector heads are installed in the slot closest to the RFL 97 I/O Interface Assembly.**

2. Line up the connector on the back of the fiber optic head with its mating connector on the chassis motherboard.

3. Push the fiber optic head into the chassis until it is firmly seated and its panel is against the horizontal rails at the rear of the chassis.

4. Using a flat-blade screwdriver, turn the two captive screws on the panel of the fiber optic head fully clockwise to secure it in place.

5. Reconnect the fiber optic cable to its mating connector on the fiber optic head.

6. Line up the mounting holes in the rear panel protective cover with the standoffs on the rear of the chassis, and push down on the protective cover until it is secured in place.
7. Place the POWER switch on the power supply module in the ON position.

4.2.3. RS-449 And X.21 Interface Panels

If your RFL 9700 is not equipped with fiber optic modules, either an RFL 97 449 INTER RS-449 Interface Panel or an RFL 97 X.21 INTER CCITT X.21 Interface Panel is mounted where the fiber optic heads are usually located. It is held in place with four quarter-turn fasteners. To remove an interface panel, proceed as follows:

1. Place the POWER switch on the power supply module in the OFF position.

2. Remove the protective cover from the rear panel by pulling it out of the standoffs holding it in place.

3. Disconnect the RS-449 or CCITT X.21 cable from its mating connector on the interface panel.

4. Using a flat-blade screwdriver, turn the four quarter-turn fasteners on the interface panel counterclockwise, until they are loose.

5. Pull the interface panel out of the chassis until the cable behind it and its mating connector on the chassis motherboard are visible.

6. Reach into the chassis and disconnect the cable from its mating connector.

To replace the interface panel, proceed as follows:

1. Connect the cable behind the interface panel to its mating connector on the chassis motherboard.

2. Push the interface panel into the chassis until it is against the horizontal rails at the rear of the chassis.

3. Using a flat-blade screwdriver, turn the four captive screws on the interface panel fully clockwise to secure it in place.

4. Reconnect the RS-449 or CCITT X.21 cable to its mating connector on the interface panel.

5. Line up the mounting holes in the rear panel protective cover with the standoffs on the rear of the chassis, and push down on the protective cover until it is secured in place.

6. Place the POWER switch on the power supply module in the ON position.

4.2.4. Input/Output Module

The RFL 97 I/O Input/Output Module is mounted at the rear of every RFL 9700 chassis. It is held in place with six quarter-turn fasteners. To remove the RFL 97 I/O, proceed as follows:

1. Place the POWER switch on the power supply module in the OFF position.

2. Remove the protective cover from the rear panel by pulling it out of the standoffs holding it in place.

3. Disconnect all wiring from all terminal blocks on the rear of the RFL 97 I/O.

   Be sure to tag all wires before removing them; this will make reconnection easier.

4. Using a flat-blade screwdriver, remove the two screws from the RFL 97 I/O that are just past the ends of terminal block TB9.

5. Using a flat-blade screwdriver, turn the six quarter-turn fasteners on the RFL 97 I/O counterclockwise, until they are loose.

6. Pull the RFL 97 I/O out of the chassis until the ribbon cables behind it and their mating connectors on the chassis motherboard are visible.

   RFL 97 I/O modules equipped for four channels have one ribbon cable; those equipped for eight channels have two.

7. Reach into the chassis and disconnect the ribbon cables from their mating connectors.

To replace the RFL 97 I/O, proceed as follows:

1. Connect the ribbon cables behind the RFL 97 I/O to their mating connectors on the chassis motherboard.

   Four-channel modules have one cable, which must be connected to the mating connector closest to the bottom edge of the motherboard. Eight-channel modules have two cables (one from each circuit board). Connect the top cable to the mating connector closest to the top of the motherboard, and the bottom cable to the mating connector closest to the bottom of the motherboard.

2. Push the RFL 97 I/O into the chassis until it is against the horizontal rails at the rear of the chassis.

3. Using a flat-blade screwdriver, turn the six captive screws on the RFL 97 I/O fully clockwise to secure it in place.

4. Insert two screws into the two holes that are just past the ends of terminal block TB9. Using a flat-blade screwdriver, tighten these screws.

5. Reconnect all wiring to the terminal blocks on the rear of the RFL 97 I/O.

   If the wires were tagged during removal, follow the markings on the tags. If they weren't tagged, refer to Section 2 for wiring instructions.

6. Line up the mounting holes in the rear panel protective cover with the standoffs on the rear of the chassis, and push down on the protective cover until it is secured in place.

7. Place the POWER switch on the power supply module in the ON position.

4.3. FUSE REPLACEMENT

The input fuses for RFL 9700 terminals equipped with internal power supplies are located on the front panel of the power supply module. Fuses can be changed without removing the power supply module from the chassis. If your RFL 9700 is equipped with an external power supply, refer to the documentation furnished with the power supply for fuse replacement procedures.

To check and/or replace the fuses in an internal power supply, proceed as follows:

CAUTION

Never attempt to remove or replace a fuse with the power supply module energized; component damage may result.

1. Place the POWER switch on the power supply module in the OFF position.

2. Remove one of the input fuses from its fuseholder by pushing in on the fuseholder cap and turning it counter clockwise about 1/4 turn.

   Some fuseholders require a screwdriver to remove the fuse, while others can be turned with the fingers.

3. Remove the fuse from the fuseholder cap and inspect it for damage.

   If the fuse is bad, it must be replaced. If the fuse is good, check for presence of input voltage TB9-2 and TB9-3 on the RFL 97 I/O input/output module. If voltage is present and the power supply does not function, troubleshoot the supply to determine the cause of failure.

CAUTION

For continued safe operation, always replace a fuse with one having the same voltage and current ratings. (See power supply documentation for proper replacements.)

4. Insert a fuse with the proper voltage and current ratings into the fuseholder cap and push it in until it is firmly seated.

5. Insert the fuse and fuseholder cap into the fuseholder. Using a flat-blade screwdriver, push in on the cap and turn clockwise about one quarter-turn.

   This will secure the fuse in place.

6. Repeat steps 2 through 5 for the other fuse.

7. Once both fuses have been checked and/or replaced, place the power switch in the ON position.

   If the +5V, +15V, and -15V indicators light, the power supply module is working properly. If one or more indicators do not light or if one or both fuses blow again, troubleshoot the power supply module.

4.4. CORRECTIVE MAINTENANCE

The RFL 9700 Digital Protection Channel has been designed for years of trouble-free service. Should a malfunction occur involving the RFL 9700, use standard troubleshooting techniques to determine if the problem is in the RFL 9700, or in some other connected equipment. If the problem lies within the RFL 9700, use the schematics in this section to try and determine which module is defective. Once this is done, replace the module; this should solve the problem.

Defective modules can be repaired locally, or they can be returned to RFL for repair (para 4.5).

4.5. HOW TO ARRANGE FOR SERVICING

If necessary, RFL 9700 modules and subassemblies may be returned to RFL for repair. Contact our Customer Service Department using the telephone number listed on the cover of this manual. You will be given an authorization number and shipping instructions.

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Section 5. INPUT/OUTPUT MODULE

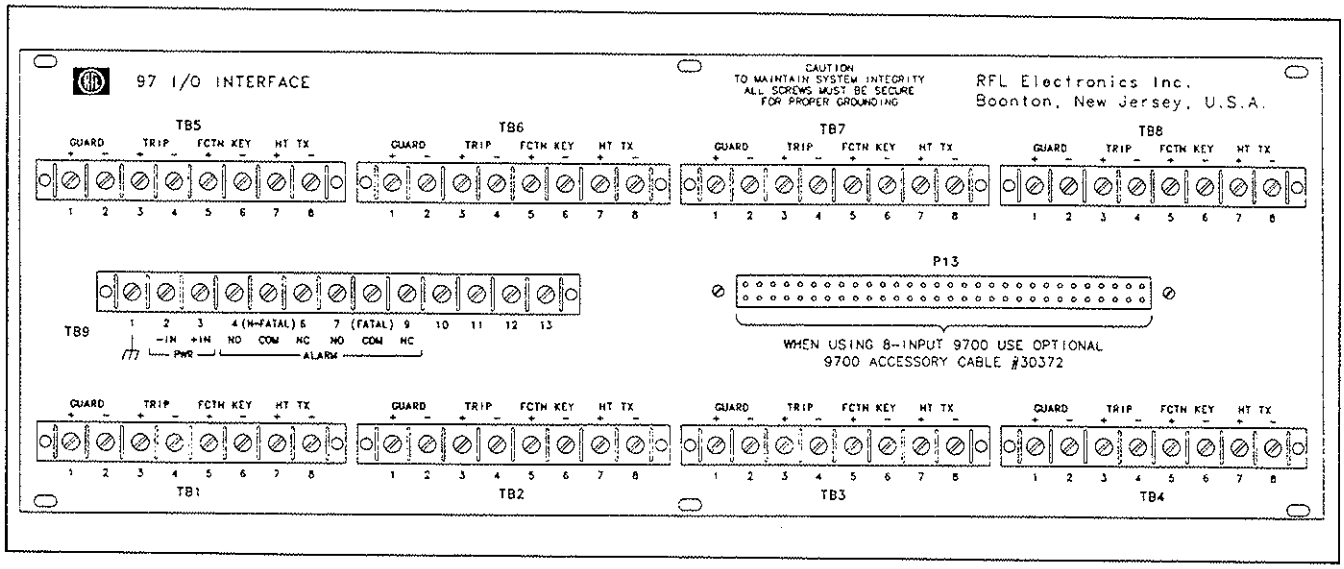


Figure 5-1. RFL 97 I/O Input/Output Module

5.1. DESCRIPTION

The RFL 97 I/O Input/Output Module (Fig. 5-1) provides the interface connections between the RFL 9700 and external equipment. All high-voltage and transient suppression is performed on the RFL 97 I/O module.

The RFL 97 I/O is mounted at the rear of the RFL 97 CHAS chassis, and is connected to the chassis motherboard by ribbon cables. The RFL 97 I/O can be equipped with either one circuit board for four-function capability, or two circuit boards for eight-function capability. Each circuit board contains four isolated one-amp TRIP output drivers, four isolated one-amp GUARD output drivers, four HAS TRIPPED relays, four optically-isolated input circuits, and four eight-position terminal blocks (one for each channel).

A 13-position terminal block is also included on the RFL 97 I/O for input power and alarm relay connections. A 60-pin connector is also provided for connections to the RFL 9700's RS-449 multiplexer and voice and data accessories, which are described in Section 18 of this manual.

5.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to the RFL 97 I/O module. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

FUNCTION KEY Inputs: 42 Vdc to 142 Vdc @ 18 mA maximum.

GUARD And TRIP Outputs: Capable of switching 1 ampere @ 25° and 0.675 ampere @ 65°, with a load voltage or 125 Vdc. Minimum load voltage is 4 Vdc, and minimum load current is 0.1 ampere.

HAS TRIPPED Output: Capable of switching 0.1 ampere @ 125 Vdc.

Interface Dielectric Strength: All trip, guard, function key, and tone lines are isolated from ground and from all other circuits. Breakdown is 1500 Vrms @ 50/60 Hz, 2500 Vdc, and 2500 volts @ 1.5 MHz, meeting the requirements of IEEE Surge Withstand Capability Specification 472-1978 (ANSI C.37.90-1978).

The RFL 97 I/O also meets the requirements of ANSI-IEEE Fast Transient Specification C.37.90.1.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F)
Operating: -30°C to +65°C (-22°F to +149°F)

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements: 4.75 to 5.25 Vdc @ 200 mA; obtained from chassis power supply.

Dimensions:
Width: 14.2 inches (360 mm).
Height: 5.1 inches (130 mm).
Depth (behind panel): 2.6 inches (67 mm).

5.3. THEORY OF OPERATION

The RFL 97 I/O contains an array of solid-state modules that control the inputs to and outputs from the RFL 9700. A block diagram of the RFL 97 I/O appears in Figure 5-2.

a. Input Modules. K3, K7, K11, and K15 are optically-isolated solid-state input modules. Typically, the current input signal to these modules is derived from the station battery through fault relay contacts and 5000Ω limiting resistors. A trip signal will force the relay output (pin 4) to pull down to a logic zero through 1000Ω resistors on the trip buffer module (Section 6). Each solid-state module contains circuitry to protect itself against high-voltage transients.

b. HAS TRIPPED Relays. K4, K8, K12, and K16 are optically-isolated solid-state, which serve as HAS TRIPPED relays. The trip signals from the input modules are de-bounced by the trip buffer module, and passed to TX INPUT contact latch U3 on the transmitter interface module (Section 7). This latch is read once every message interval by the logic CPU module (Section 11). The trip signals are passed through the COMMAND EXTEND and COMBINATIONAL LOGIC FUNCTION software blocks; the trip byte that is produced is transmitted to the remote station by the digital transmitter module (Section 8).

The HAS TRIPPED relays indicate the state of the transmitted trip byte. Signal current to drive these relays is supplied by output latch U5 on the indicator/output module (Section 12). The solid-state relays are protected against high-voltage transients by the inductors, capacitors, and transient suppressors connected across their input terminals.

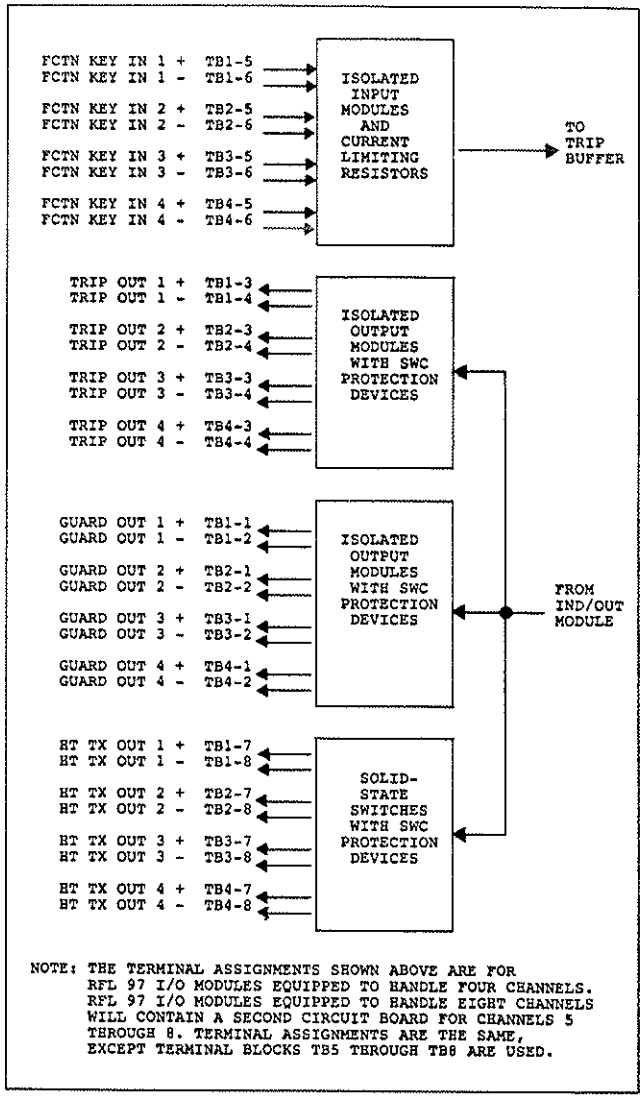


Figure 5-2. Block diagram, RFL 97 I/O Input/Output Module

c. TRIP Output Drivers. K2, K6, K10, and K14 are optically-isolated 1-amp output drivers, used for the TRIP outputs. The signal current required to operate these devices is supplied by output latch U4 on the indicator/output module. The TRIP OUTPUT drivers will trip in response to signals received from remote stations and decoded by the digital receiver module. The capacitors and inductors connected to their output terminals protect the output drivers against high-voltage transients.

d. GUARD Output Drivers. K1, K5, K9, and K13 are optically-isolated 1-amp output drivers, used for the GUARD outputs. The signal current required to operate these devices is supplied by output latch U3 on the indicator/output module. The GUARD OUTPUT drivers will trip in response to signals originating on the logic CPU module; GUARD is a calculated signal, and is based on the channel TRIP signal and any alarm conditions that may be present. The capacitors and inductors connected to their output terminals protect the output drivers against high-voltage transients.

Table 5-1. Replaceable parts, RFL 97 I/O Input/Output Module Assembly No. 101585

Circuit Symbol (Figs. 5-3 & 5-4)	Description	Part Number
C1-24	Capacitor,ceramic disc,0.005µF,20%,3kV,Centralab DD30-502 or equiv.	1007 1264
C25-28	Capacitor,X7R ceramic,0.1µF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
CR1-4	Transient suppressor,190- to 210-volt breakdown,General Semiconductor 1.5KE200CA or equiv.	30266
K1,2,5,6,9,10,13,14	Optical output module,5-volt input,4- to 200-volt output @ 1 amp load current, Grayhill 70M-ODC-5A or equiv.	30267
K3,7,11,15	Optical input module,3- to 32-Vdc input A 18 mA, 5-volt logic output @ 50 mA, Grayhill 70M-IDC5 or equiv.	98098
K4,8,12,16	Solid-state switch,200 Vdc @ 150 mA,3750-volt isolation,Theta-J Corp. LCA120E or equiv.	98097
L1-24	Inductor,rf,10µH,5%,J.W. Miller 4622 or equiv.	30285
R1-8	Resistor,wirewound,5K,5%,3.25W,Ohmite 4442 Style 995-3A or equiv.	1100 460

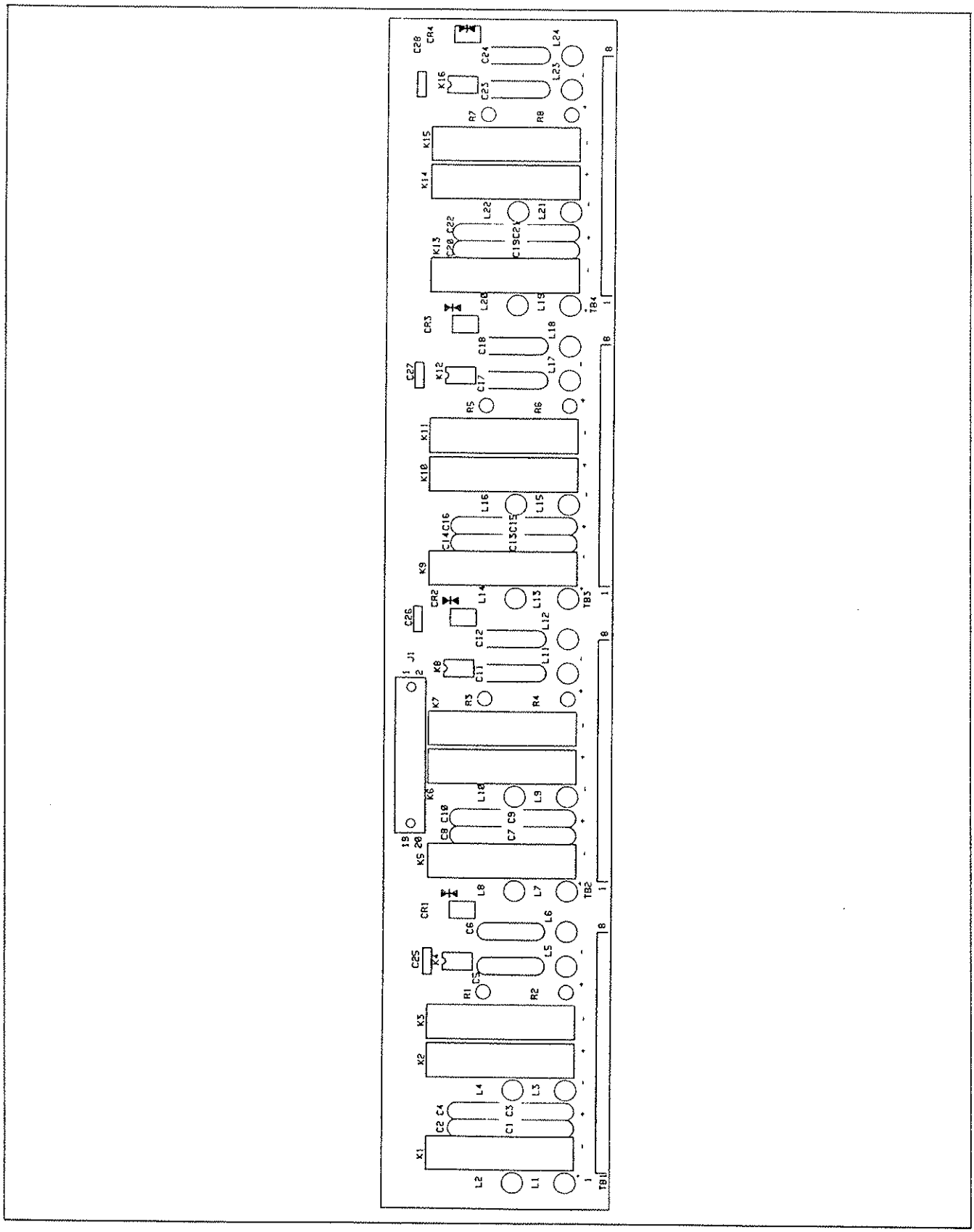


Figure 5-3. Component locator drawing, RFL 97 I/O Input/Output Module (Assembly No. 101585; Drawing No. D-101588, Rev. B)

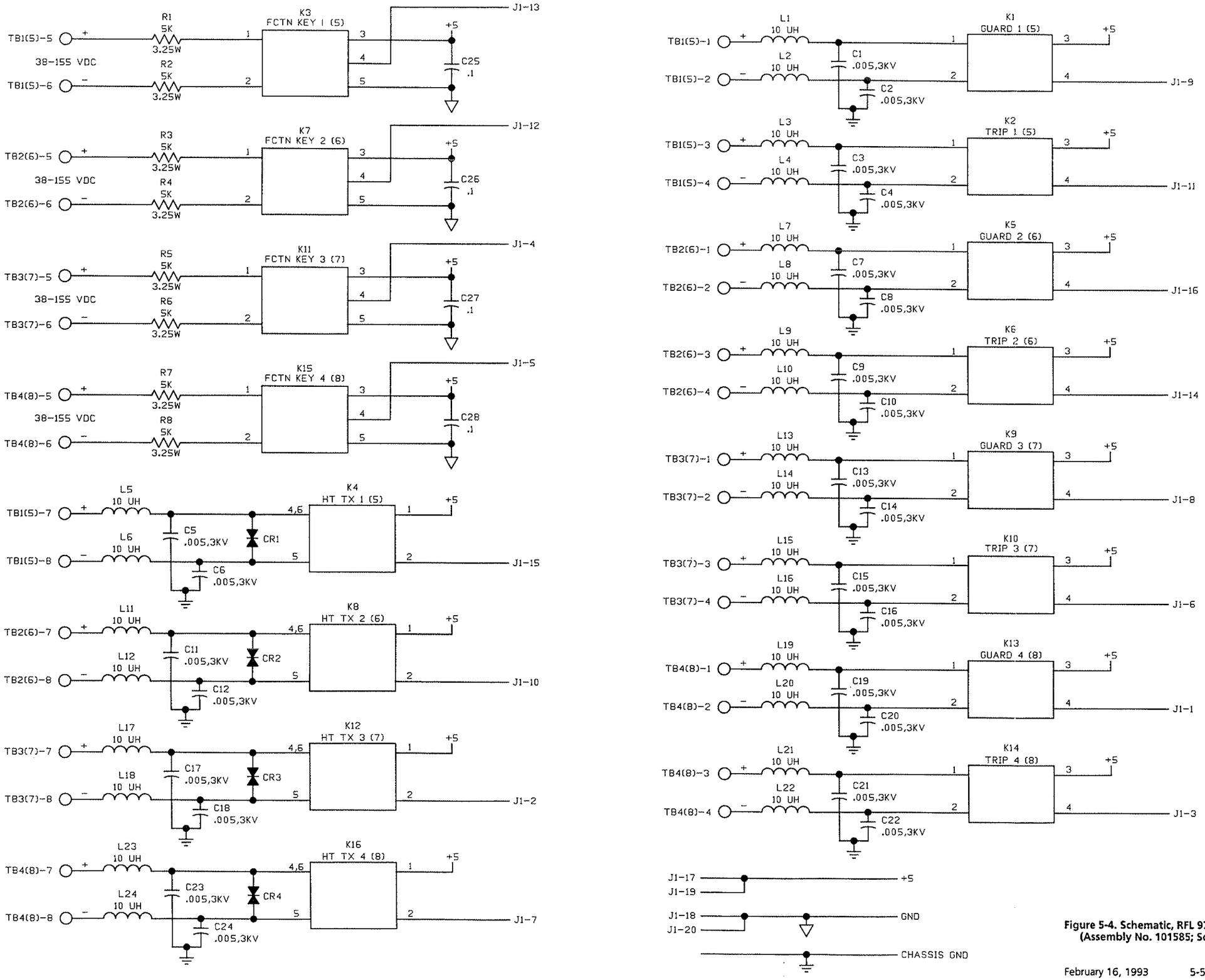


Figure 5-4. Schematic, RFL 97 I/O Input/Output Module (Assembly No. 101585; Schematic No. D-101589, Rev. D)

Section 6. TRIP BUFFER MODULE

6.1. DESCRIPTION

The RFL 97 TRIP BUFFER Trip Buffer Module (Fig. 6-1) accepts the function keying information from the optical isolators on the input/output module (Section 5) and decides the acceptance criteria. It occupies one dedicated module space in the RFL 97 CHAS chassis.

6.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to the RFL 97 TRIP BUFFER module. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Inputs:
Type: Eight contact inputs that accept switched ground signals.
Switch Rate: 200 Hz maximum.

Outputs:
Type: Eight CMOS-level outputs.
Pulse Rate: 1.9 to 3.8 ms maximum.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements: 4.75 to 5.25 Vdc @ 20 mA; obtained from chassis power supply.

Dimensions:
Panel Height: 5.1 inches (130 mm).
Panel Width: 1.4 inches (36 mm).
Depth (behind panel): 9.1 inches (231 mm).

6.3. THEORY OF OPERATION

The RFL 97 TRIP BUFFER checks the incoming FCTN KEY signals applied to the input/output module. If the signals meet the acceptance criteria, they are accepted as valid and passed on to the transmitter interface module (Section 7). The RFL 97 TRIP BUFFER contains eight delay circuits and eight latch circuits (one for each FCTN KEY input), and an octal latch that provides the interface to the transmitter interface module.

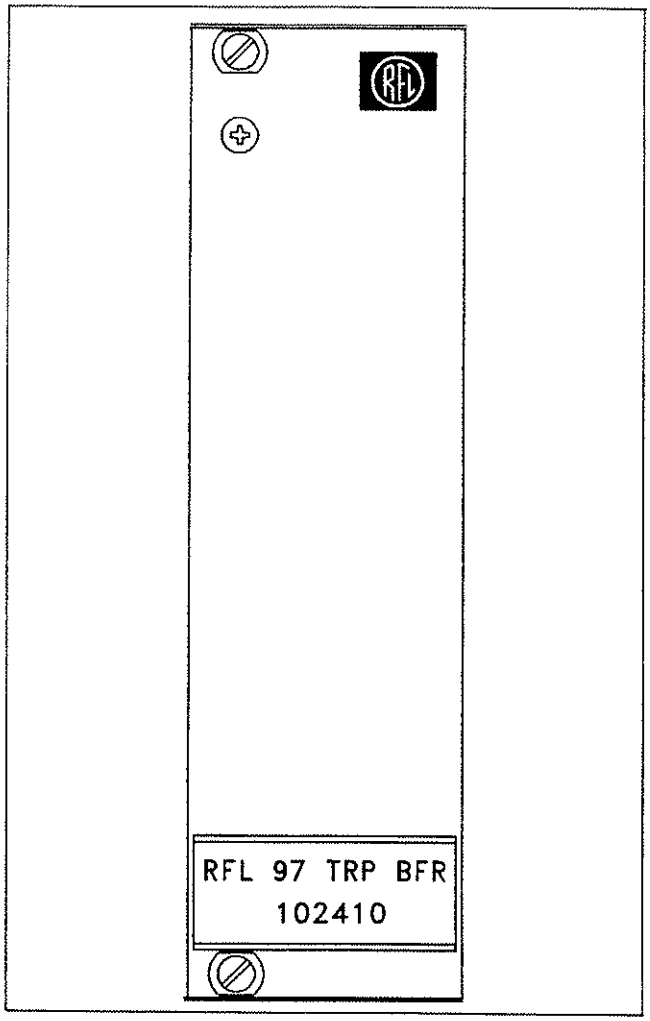


Figure 6-1. RFL 97 TRIP BUFFER Trip Buffer Module

A block diagram of the RFL 97 TRIP BUFFER appears in Figure 6-2. For clarity, the input circuitry is only shown for the FCTN KEY 1 input; the other seven input circuits are identical, though they use different components.

Each FCTN KEY input is fed through a 100-µs delay circuit. The delay circuits make sure that state changes at the FCTN KEY inputs do not trigger the latch circuits unless they last longer than 100 microseconds. This provides immunity against noise spikes and glitches, and helps prevent false trips.

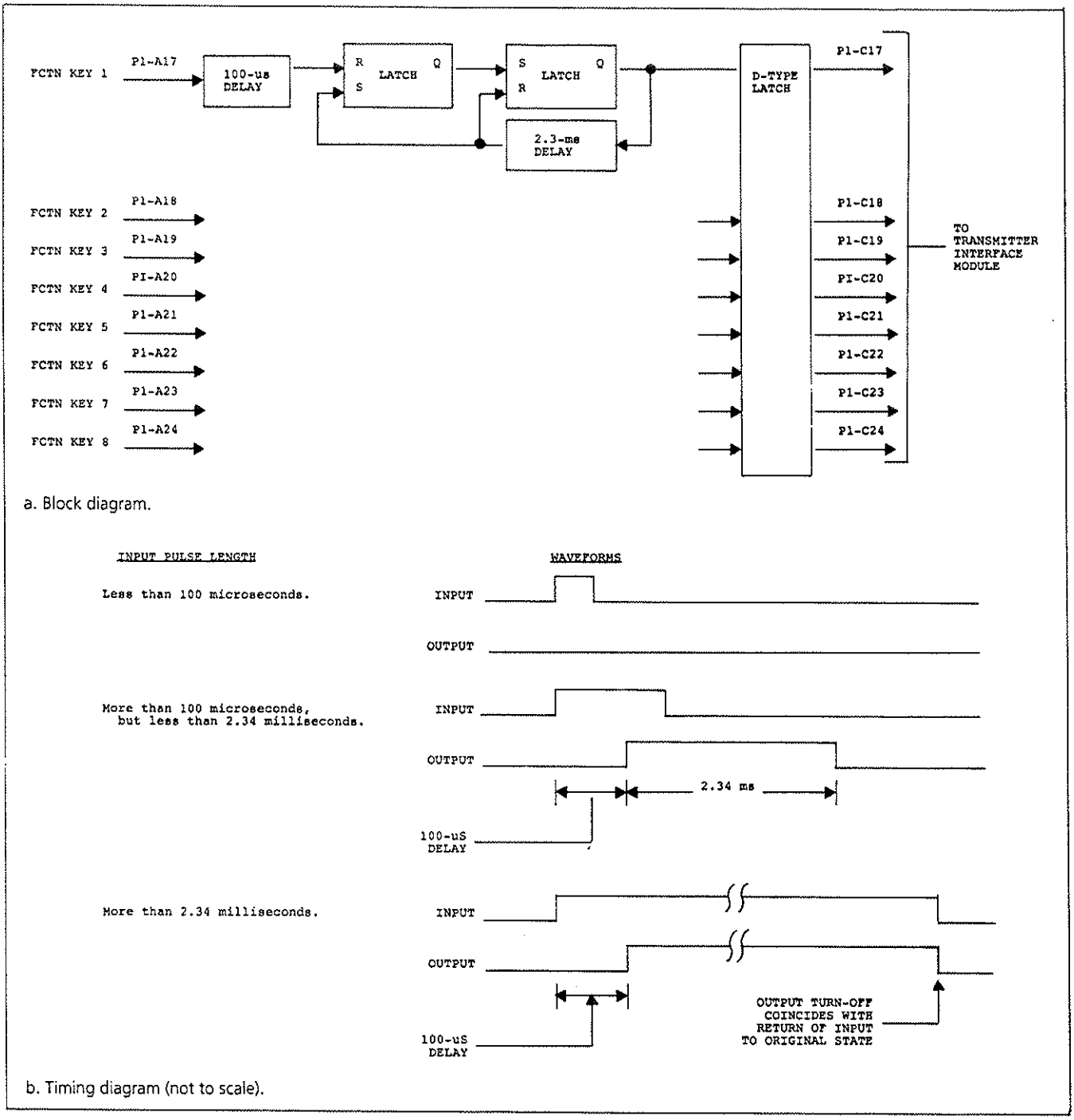


Figure 6-2. Block diagram, RFL 97 TRIP BUFFER Trip Buffer Module

The output from the delay circuit is fed to a latch circuit formed from quad latches U3 through U6. FCTN KEY 1 through FCTN KEY 4 are handled by U4 and U6, and FCTN KEY 5 through FCTN KEY 8 are handled by U3 and U5.

c. Octal Latch. The outputs of the latch circuits are passed to octal latch U9. Its output lines pass through edge connector pins P1-C17 through P1-C24 to the transmitter interface module.

Table 6-1. Replaceable parts, RFL 97 TRIP BUFFER Trip Buffer Module
Assembly No. 102410

Circuit Symbol (Figs. 6-3 & 6-4)	Description	Part Number
C1	Capacitor,electrolytic,47µF,20%,16V,Nichicon ULB1C470M or equiv.	1007 1629
C2	Capacitor,ceramic,47pF,5%,100V,AVX SA101A470JAA or equiv.	0125 14705
C3	Capacitor,ceramic,0.001µF,5%,100V,AVX SA201A102JAA or equiv.	0125 11025
C4-7	Capacitor,X7R ceramic,0.01µF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
RZ1	Resistor network,nine 1K 2% resistors,1.1W total,10-pin SIP,Allen-Bradley 110A102 or equiv.	32349
U1,2,7,8	MOS hex contact bounce eliminator,16-pin DIP,Motorola MC14490FP or equiv.	0615 74
U3,4	MOS quad tri-state R/S latch,16-pin DIP,RCA CD4044BE or equiv.	0615 324
U5,6	MOS quad tri-state R/S latch,16-pin DIP,RCA CD4043BE or equiv.	0615 18
U9	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U10	MOS hex inverter/buffer,16-pin DIP,RCA CD4049AE or equiv.	0615 7

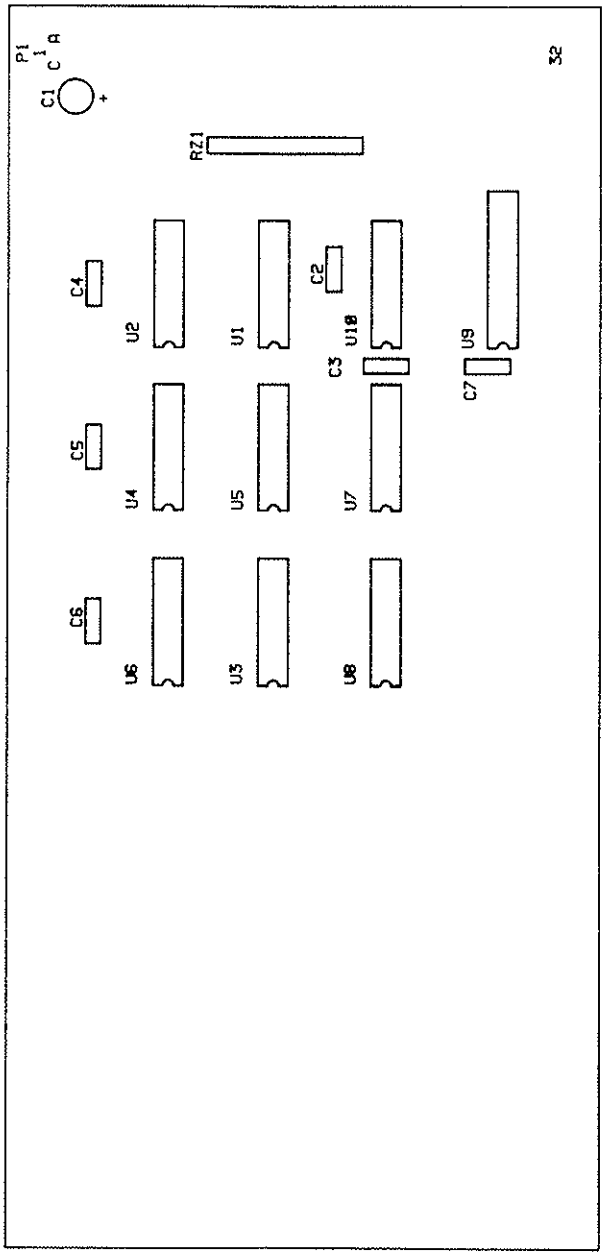
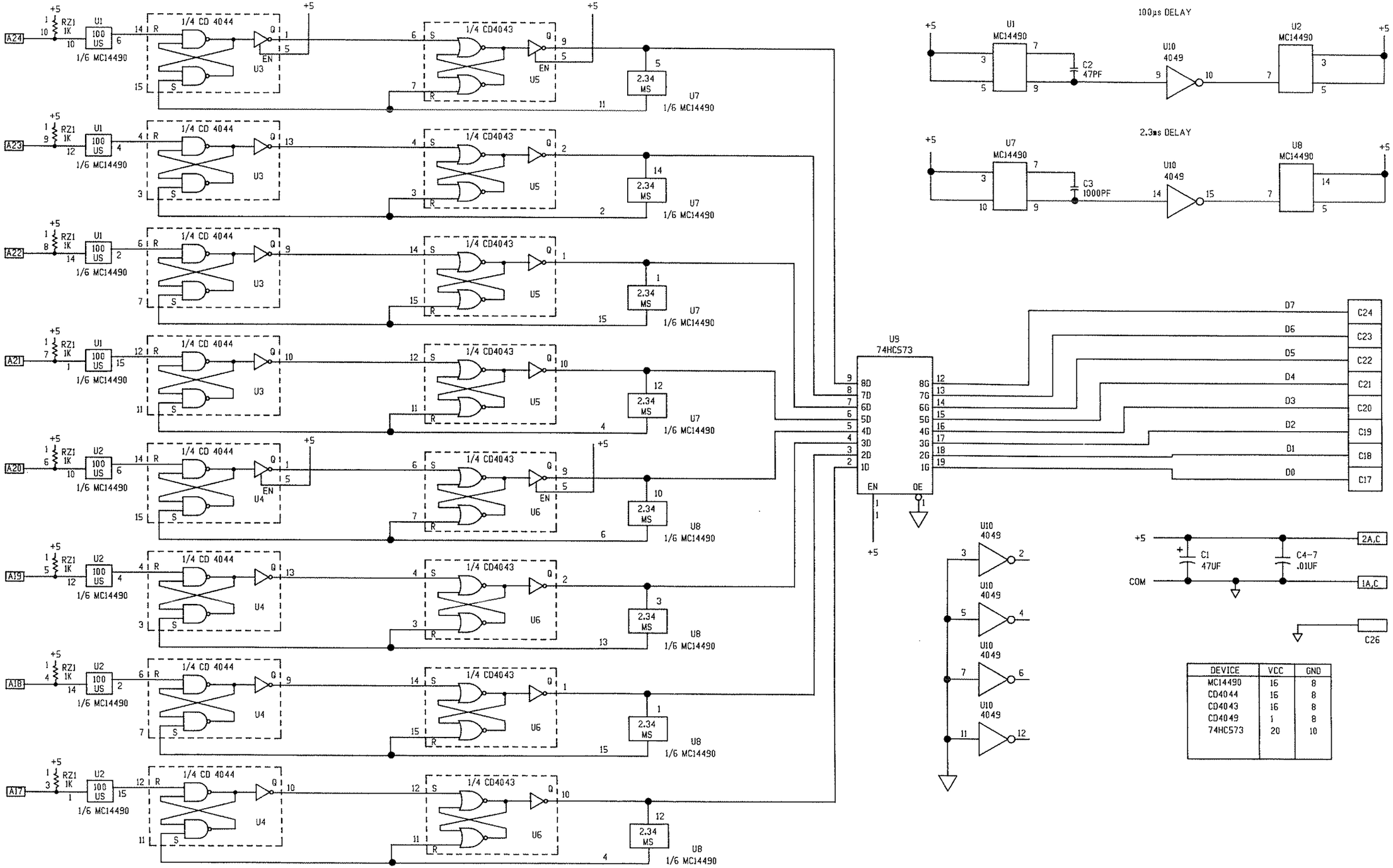


Figure 6-3. Component locator drawing, RFL 97 TRIP BUFFER Trip Buffer Module (Assembly No. 102410; Drawing No. D-102413, Rev. A)



DEVICE	VCC	GND
MC14490	16	8
CD4044	16	8
CD4043	16	8
CD4049	1	8
74HC573	20	10

Figure 6-4. Schematic, RFL 97 TRIP BUFFER Trip Buffer Module (Assembly No. 102410; Schematic No. D-102414, Rev. A)

Section 7. TRANSMITTER INTERFACE MODULE

7.1. DESCRIPTION

The RFL 97 TX INTER Transmitter Interface Module (Fig. 7-1) accepts the function key signals from the trip buffer module (Section 6) and places them on the control bus. It also contains all of the function programming switches for the logic CPU module (Section 11). Eight LED indicators on its front panel show when a channel has tripped. It occupies one dedicated module space in the RFL 97 CHAS chassis.

7.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to the RFL 97 TX INTER module. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

LED Display: Eight red light-emitting diodes on the front panel; each lights when the channel it is monitoring has tripped.

Inputs: CMOS logic level. Voltage thresholds will vary according to the type of CMOS devices installed on the module:

KS74AHCT Devices: 2.0 volts minimum logic high, 0.8 volts maximum logic low.

74HC Devices: 3.15 volts minimum logic high, 0.9 volts maximum logic low.

Outputs: Two: CHECKBACK TEST and TEST FUNCTION FAIL RESET. These outputs will go low when the corresponding switches on the front panel are pressed.

Output Levels: CMOS logic levels (0 to 5 Vdc). Both outputs are capable of sinking 5 mA at a V_{ol} of 0.33 Vdc maximum.

Temperature:

Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements: 4.75 to 5.25 Vdc @ 125 mA; obtained from chassis power supply.

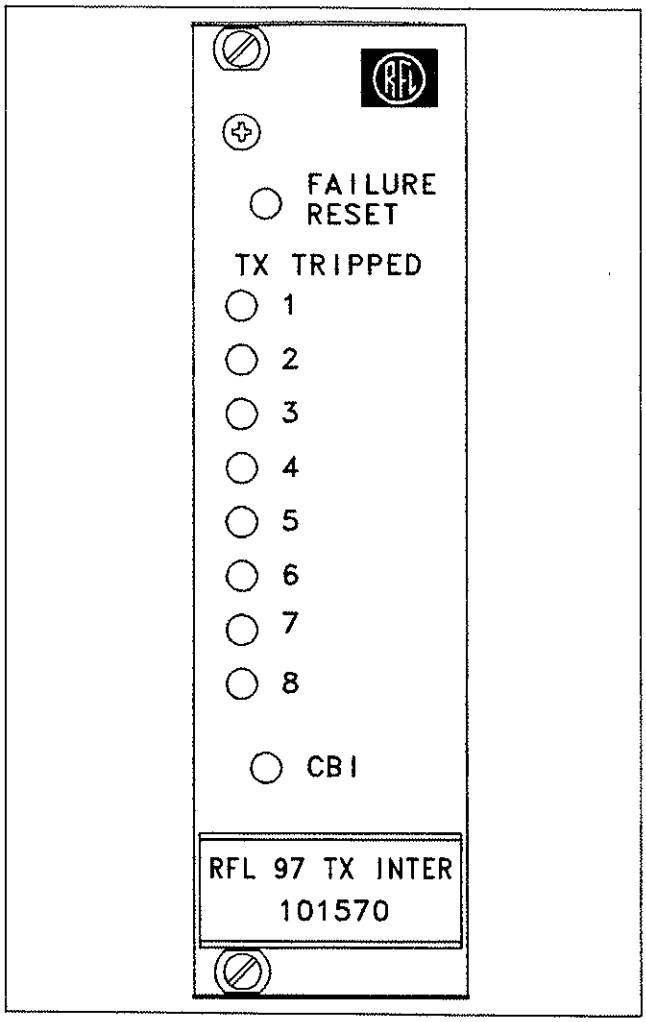


Figure 7-1. RFL 97 TX INTER Transmitter Interface Module

Dimensions:

Panel Height: 5.1 inches (130 mm).
Panel Width: 1.4 inches (36 mm).
Depth (behind panel): 9.1 inches (231 mm).

7.3. THEORY OF OPERATION

The RFL 97 TX INTER Transmitter Interface Module contains all the DIP switches used to program the software functions found on the logic CPU module. In addition, an array of light-emitting diodes on its front panel displays all transmitted input trip signals. (Information on switch settings can be found in Section 3 of this manual; the logic CPU module is covered in Section 11.)

Two pushbutton switches on the front panel allow the station operator to manually initiate a checkback test, or reset the alarm indicators after a checkback test failure or function failure has occurred. A block diagram of the RFL 97 TX INTER appears in Figure 7-2.

a. Data Transfer With Logic CPU Module. The RFL 97 TX INTER interfaces with the logic CPU module through the data and control buses found on the RFL 97 INTER chassis motherboard (Section 17). When the logic CPU module wishes to access a latch on the RFL 97 TX INTER, it sends a control address over the control bus to the input of buffer U1.

The address is decoded by three 3-line to 8-line decoder chips, U8, U9, and U10. The selected latch will have its tri-state output buffers enabled. The data applied to its input pins will appear on the internal data bus. Whenever any latch on this module is accessed, output Y0 on U10 will go low, enabling the tri-state outputs of buffer U2. This allows the data appearing on the internal data bus to appear on the motherboard data bus and become available to the logic CPU module.

The transmitter input contact signals appear on the input of U3 after being de-bounced by the trip buffer module (Section 6). When output Y0 of U9 goes low, these signals appear on the data bus and are read by the logic CPU module. On the next rising edge of U9 output Y0, these signals are latched into octal flip-flop U18 and appear on front-panel LED arrays DS1 and DS2.

The receiver output contact signals which drive the trip relays on the input/output module (Section 5) are accessed by the logic CPU through tri-state latch U4. The processor compares the contact signal byte with the contents of its output contact register. If the channel bit positions don't match, a non-responsive channel output is indicated. This will result in a non-fatal alarm, and the FUNCTION FAIL indicator on the indicator/output module will light. In addition, the logic CPU module will indicate any failed channels by lighting the channel indicators on its front panel.

b. Programmable DIP Switches. Buffers U11 through U17 interface programmable DIP switches S3 through S10 to the internal data bus. Some of these switches enable functions on various channels: S3 controls unblock on channels 5 through 8, S5 controls guard-before-trip on all channels, S6 controls trip hold on all channels, and S8 controls command extend on all channels. Some of these functions are mutually exclusive; unblock and guard-before-trip cannot be selected for the same channel (guard-before-trip will be enabled by default), and unblock and trip hold cannot be used on the same channel (they will cancel each other out).

DIP switches S4, S7, S9, and S10 are used to select time constants for various functions on the RFL 97 TX INTER; S4 controls the trip hold time constant, and S7 the command extend time constant. S9 controls the permissive coordinating echo time constant, and S10 the permissive coordinating current reversal time constant; S9 and S10 settings will have no effect on logic CPU modules that do not contain the optional permissive coordinating software. The selected time constant will apply to all channels on which the related function is enabled.

Additional information on the DIP switch settings can be found in Section 3 of this manual.

c. Bus Testing. Latches U6 and U7 are used to test the data and control buses and the backplane integrity once every 200 milliseconds. When Address 84H is applied to the control bus inputs, pin 11 of decoder U9 will go low, setting pin 5 of U6 low and pin 6 of U6 high. This signal will also enable U7, causing its input signals to appear on the data bus. In this case, the output of U7 will be 55H, which is read by the microprocessor on the logic CPU module. In the same manner, address 83H is applied to the control bus inputs to cause pin 12 of U9 to go low, presetting U6 through pin 4. This will cause pin 5 of U6 to go high and pin 6 to go low, placing AAH on the data bus. Should the microprocessor not be able to verify these readings, a watchdog CPU alarm will occur; the logic CPU module will de-energize all outputs and return to its initialization mode, where it will remain until the problem is corrected.

The rest of U6 is used to latch the CHECKBACK OK signal received from the receiver CPU module (Section 9). The presence of this signal indicates that the system has passed a checkback test. The logic CPU module's microprocessor can access this signal through buffer U5; if necessary, it can reset the signal by sending Address 8FH to the RFL 97 TX INTER over the control bus.

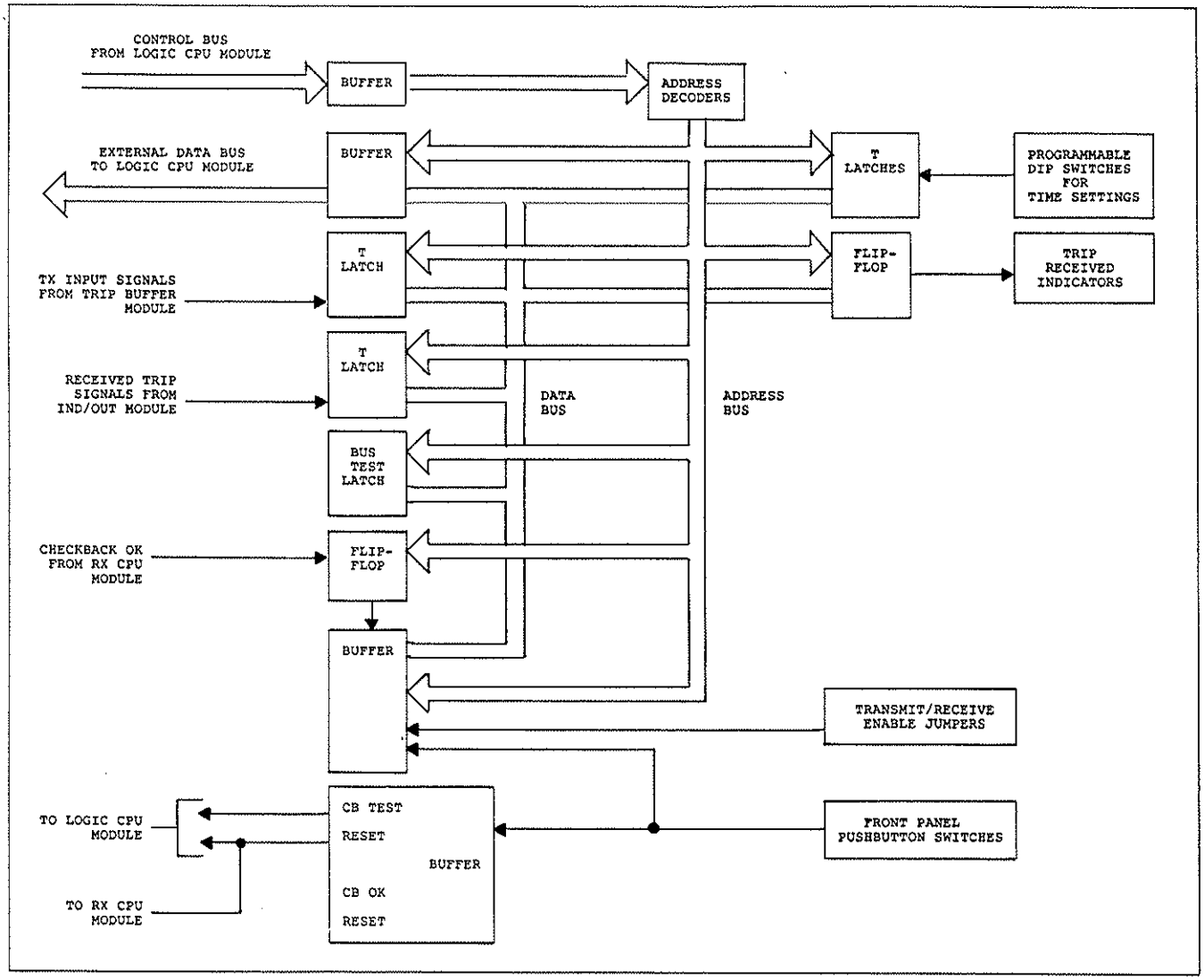


Figure 7-2. Block diagram, RFL 97 TX INTER Transmitter Interface Module

Table 7-1. Replaceable parts, RFL 97 TX INTER Transmitter Interface Module Assembly No. 101570

Circuit Symbol (Figs. 7-3 & 7-4)	Description	Part Number
C1	Capacitor,electrolytic,47μF,20%,16V,Nichicon ULB1C470M or equiv.	1007 1629
C2-20	Capacitor,X7R ceramic,0.01μF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
CR1,2	Diode,silicon,1N914B or 1N4448	26482
DS1,2	Light-emitting diode array (four),red,right-angle PC mount,Industrial Devices 5640E1 or equiv.	30162
R1-4	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
RZ1-11	Resistor network,nine 10KΩ 2% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-103 or equiv.	32622
RZ12	Resistor network,ten 221Ω 1% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-221 or equiv.	30165
S1,2	Switch,pushbutton,SPDT,right-angle PC mount,20V ac/dc @ 0.4 VA max., C&K Components EP12-D1-A-B-E or equiv.	98488
S3,4	Switch array,four SPST switches,8-pin DIP,Grayhill 90B04S or equiv.	98492
S5-10	Switch array,eight SPST switches,16-pin DIP,Grayhill 90B08S or equiv.	98493
U1,2	MOS octal tri-state non-inverting buffer/line driver,20-pin DIP, National Semiconductor MM74HC541N or equiv.	0615 297
U3,4,7	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U5	MOS tri-state octal buffer,20-pin DIP,National Semiconductor MM74HC244N or equiv.	0615 176
U6	MOS dual D-type flip-flop w/preset and clear,14-pin DIP,National Semiconductor MM74HC74N or equiv.	0615 166
U8-10	MOS decoder,3-line to 8-line,16-pin DIP,National Semiconductor MM74HC138N or equiv.	0615 168
U11-17	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC563N or equiv.	0615 307
U18	MOS octal tri-state D-type flip-flop,20-pin DIP,Motorola MC74HC574N or equiv.	0615 298
. . .	Shorting bar,single,Molex 90059-0009 or equiv.	98306

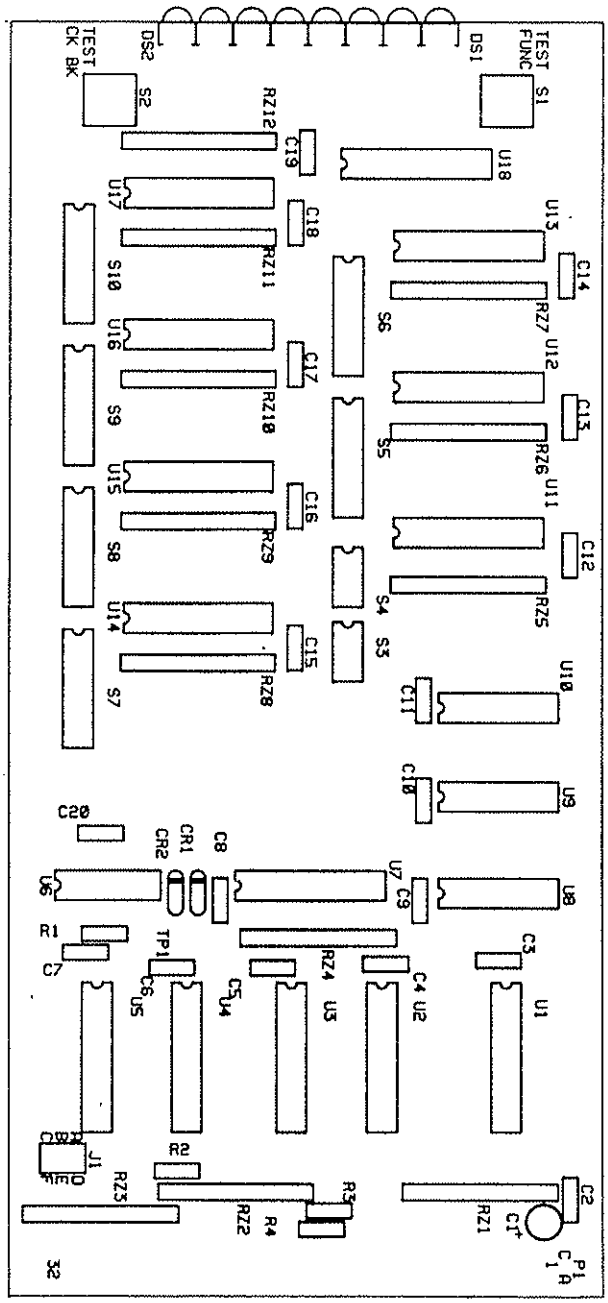


Figure 7-3. Component locator drawing, RFL 97 TX INTER Transmitter Interface Module (Assembly No. 101570; Drawing No. D-101573, Rev. A)

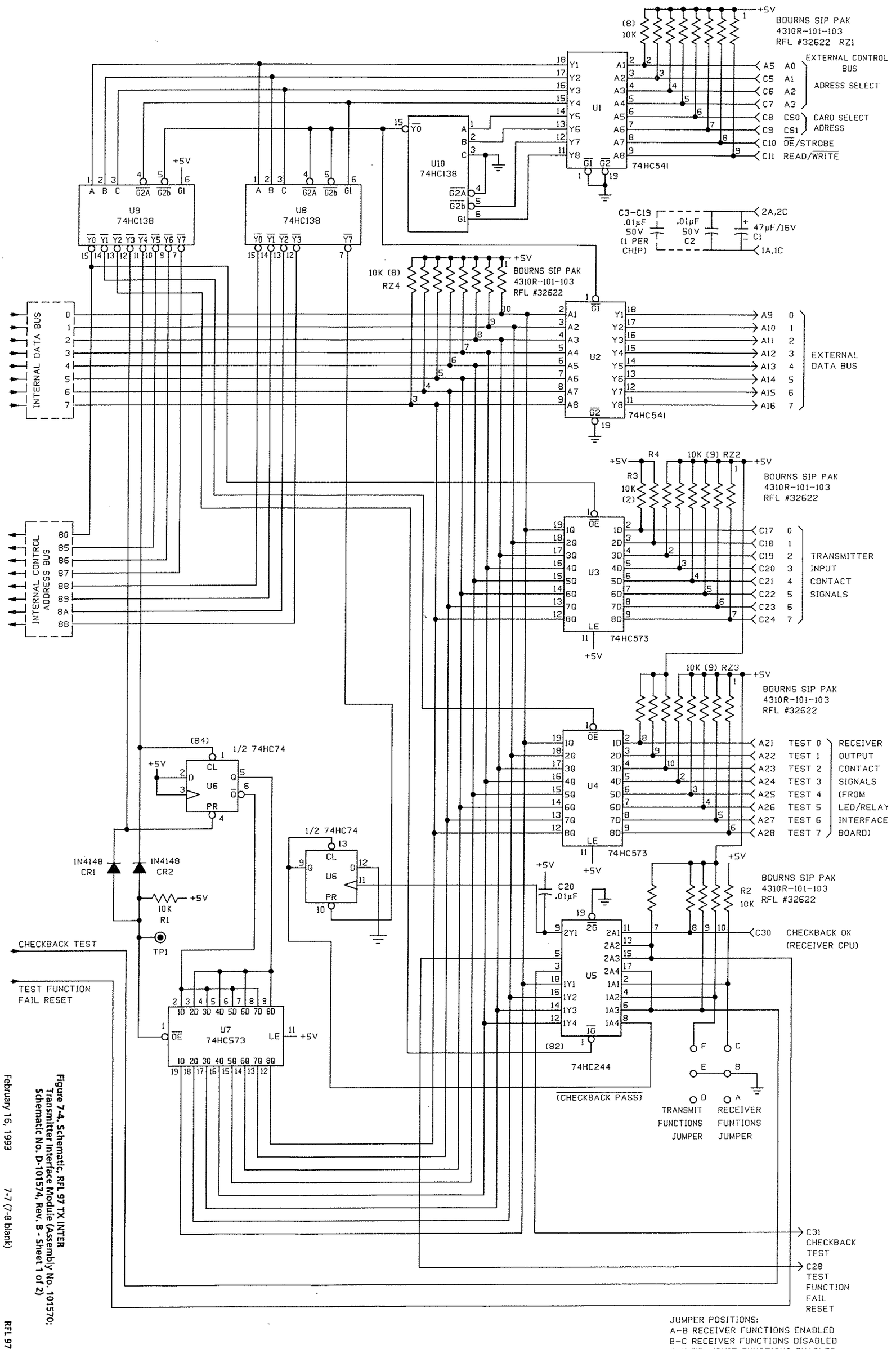


Figure 7-4. Schematic, RFL 97 TX INTER Transmitter Interface Module (Assembly No. 101570; Schematic No. D-101574, Rev. B - Sheet 1 of 2)

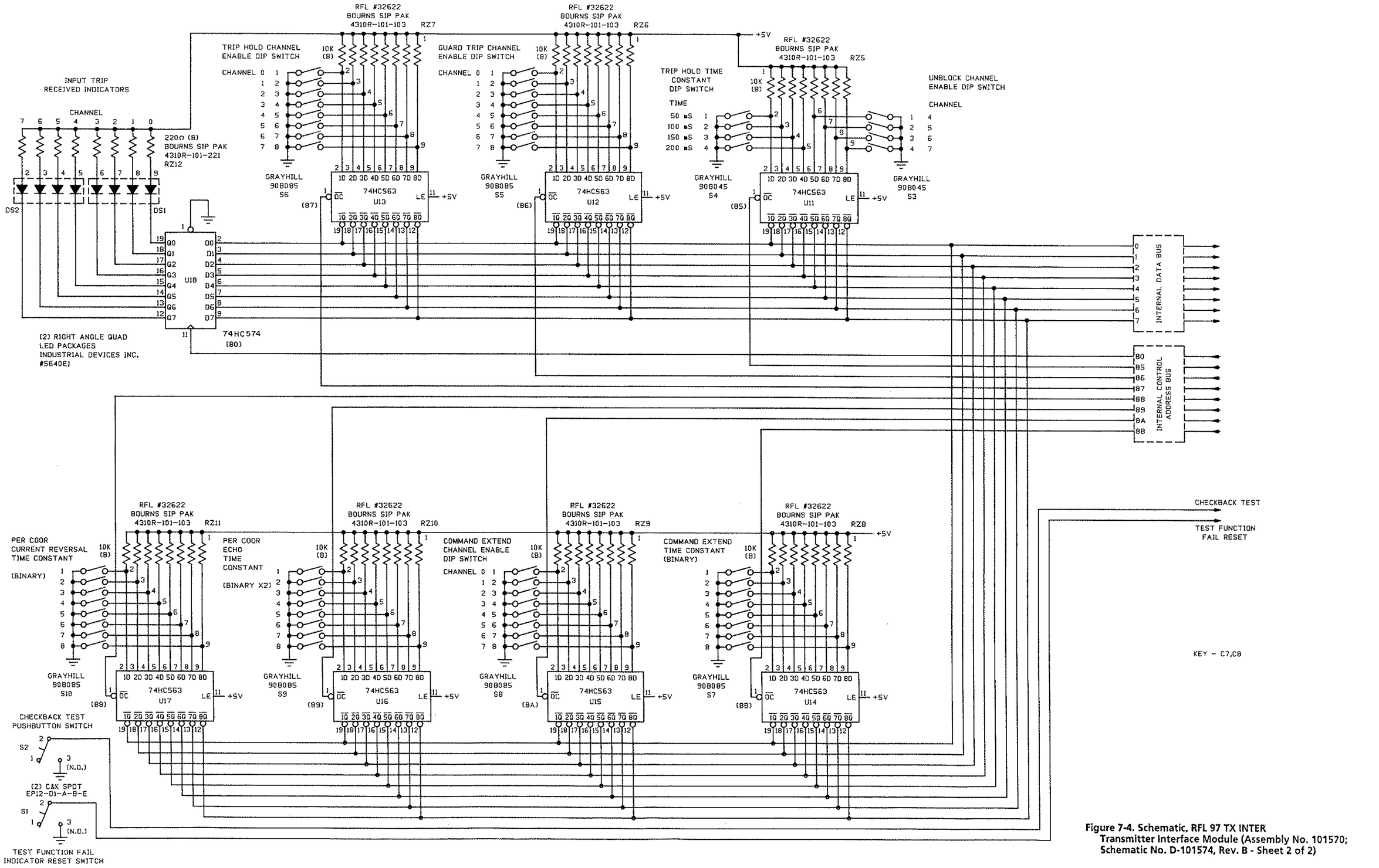


Figure 7-4. Schematic, RFL 97 TX INTER Transmitter Interface Module (Assembly No. 101570; Schematic No. D-101574, Rev. B - Sheet 2 of 2)

Section 8. DIGITAL TRANSMITTER MODULE

8.1. DESCRIPTION

RFL 9700 digital transmitter modules convert processed input trip data supplied in an eight-bit parallel format to a serial format. They also calculate the corresponding CRC code for the data, and combine them with a sync bit that alternates between one and zero. The result is a 15-bit word that is transmitted to a remote station.

There are two different digital transmitter modules available for the RFL 9700. The RFL 97A DIG TX 56 operates at 56 Kbps, meeting the requirements of EIA Specification RS-422A. The RFL 97A DIG TX 64 operates at 64 Kbps, according to the X.21 requirements in the CCITT V.11 recommendation. Either module can also transmit through the optional fiber optic transmitter module (Section 13). Each digital transmitter module occupies one dedicated module space in the RFL 97 CHAS chassis. A typical RFL 9700 digital transmitter module is shown in Figure 8-1.

8.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to both RFL 9700 digital transmitter modules, except as indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Inputs: CMOS logic level; logic high 3.15 volts minimum, logic low 0.9 volts maximum.

Outputs:
- New Message Strobe: 5-Vdc CMOS signal.
- Serial Data: Organized as 15-bit words; each word contains eight data bits, six CRC bits, and one sync bit.
- Standards Compliance:
  - RFL 97A DIG TX 56: EIA Standard RS-422A.
  - RFL 97A DIG TX 64: Meets the X.21 recommendations of CCITT Specification V.11.

Temperature:
- Storage: -40°C to +75°C (-40°F to +167°F).
- Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

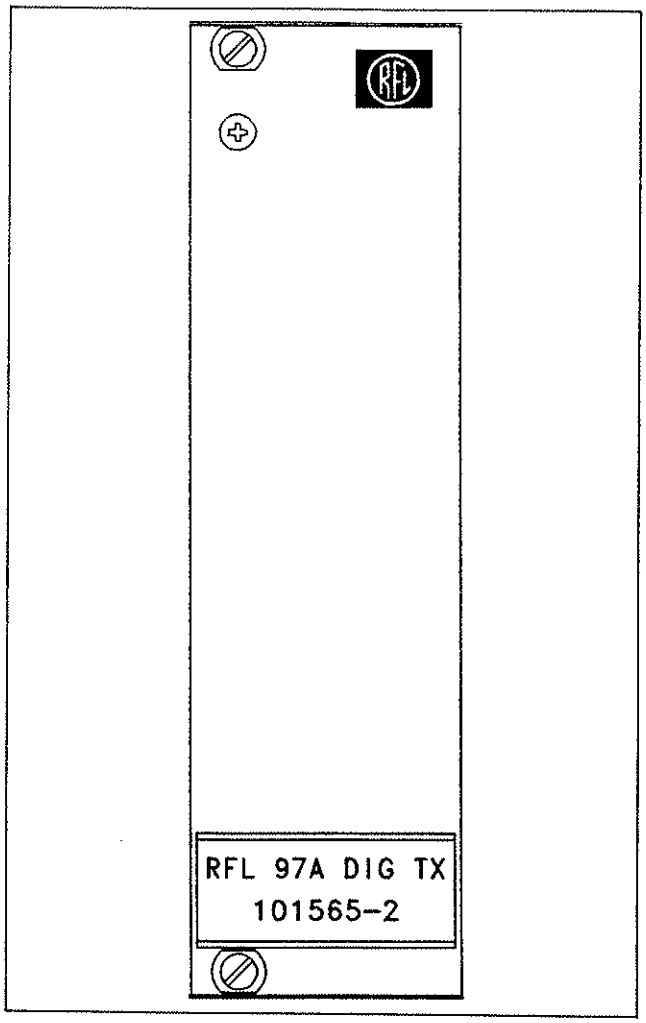


Figure 8-1. Typical RFL 9700 digital transmitter module

Input Power Requirements: 4.75 to 5.25 Vdc @ 150 mA; obtained from chassis power supply.

Dimensions:
- Panel Height: 5.1 inches (130 mm).
- Panel Width: 1.4 inches (36 mm).
- Depth (behind panel): 9.1 inches (231 mm).

8.3. THEORY OF OPERATION

RFL 9700 digital transmitter modules convert processed data supplied in an eight-bit parallel form into a 15-bit serial word. This serial word contains the original eight-bit word, plus a six-bit cyclic redundancy check (CRC) code and one alternating synchronization

bit. A block diagram for both RFL 9700 digital transmitter modules appears in Figure 8-2.

a. Input Data Processing. Processed data supplied by the logic CPU module (Section 11) is bused to the eight inputs of the RFL 97A DIG TX (edge connector terminals P1-A9 through P1-A16). Externally-generated timing signals for synchronous operation are supplied to quad line receiver U25, which converts them to CMOS logic levels. Control bus address inputs are also available to select digital transmit operations.

The control bus address is decoded by 3-line to 8-line decoder U6; the falling edge of its Y1 or Y2 outputs control the latching of data into octal latch U3. As long as the sync signal is low, the inverted data will be transferred to flip-flop U2, and the normal data will go to U4. Two NOR gates in U13 and one inverter/buffer in U15 prevent the data from being latched if the sync pulse is high (active).

If the logic CPU module initiates a watchdog alarm, edge connector terminal P1-A25 will go high, placing the outputs of U4 in a high-impedance state. The pull-up and pull-down arrangement on U4's output determines the data byte loaded into shift register U12 when the sync pulse goes high. This is the code that the receiver CPU module (Section 9) will recognize as all "no trips."

As another precaution against false data transmission, inverting latch U1, latch U2, and magnitude comparator U7 form an error check circuit that acts as a "hardware safety valve." This circuit prevents erroneous data from being transmitted by confirming what the data should be at the shift register inputs prior to transmission. When a data byte is to be transmitted, an inverted copy of the byte is first loaded into U1, then the normal data is loaded into U3. When U19-11 goes high, the data in U3 is clocked into U4; the inverted data in U1 is re-inverted and sent to U2. If the data in U2 and U3 does not match, U7's Y output will go high.

The data byte to be transmitted is loaded into U12 at the next rising edge of the LOAD signal (U12-9). This same signal latches the output of U7 into flip-flop U8. If an error has been detected, word will be transmitted that contains all zeros for data bits and all ones for CRC bits.

b. CRC Code Generation. The six-bit CRC code is calculated for each data byte. It becomes part of the 15-bit word that is transmitted, and appears after the data bits and before the sync bit. The CRC code is obtained as follows:

1. The 8-bit data word can be thought of as a seventh-order polynomial, where the data bits are simply the coefficients of the polynomial. Computing X bits of cyclic check on the given data byte requires the use of another polynomial called the "generator polynomial."

2. The data word polynomial is multiplied by (X > r), where "r" is the degree of the generator polynomial. In the RFL 9700, r is equal to 6. This multiplication results in the formation of a 14-bit polynomial, with zeroes in the lower r positions.

3. The 14-bit polynomial is then divided by the generator polynomial to produce a quotient and a remainder. The quotient is discarded, and the remainder becomes the CRC code, even if it is equal to zero.

4. At the receiving station, the entire 14-bit word it receives (after the synchronizing bit is removed) will be divided by the same generator polynomial used to generate the CRC code. This division should result in a quotient with a remainder of zero; if the remainder does not equal zero, this will be interpreted as a transmission error.

5. The polynomials used in the RFL 9700 were carefully selected to provide the highest degree of security possible without sacrificing dependability. At least four of the fourteen bits in a single transmitted word must be corrupted by noise before there is any possibility of that data being accepted as valid.

The CRC code is produced by quad Exclusive-OR gate U9, flip-flop U10, and quad AND gate U14. The code is continuously generated as the serial data is being transmitted. The generator polynomial (either normal or checkback) is determined by the Q* output of flip-flop U20A (U20-2), which works together with flip-flop U21 to ensure that the enabling level for checkback is applied for only one word time, and only when there is checkback data. U21 can be thought of as the 9th bit of latches U3 and U4. U20 is updated by the same signal that loads the data byte into shift register U12. This forces the checkback signal, which appears on the Q* output of U20, to correspond to this data byte.

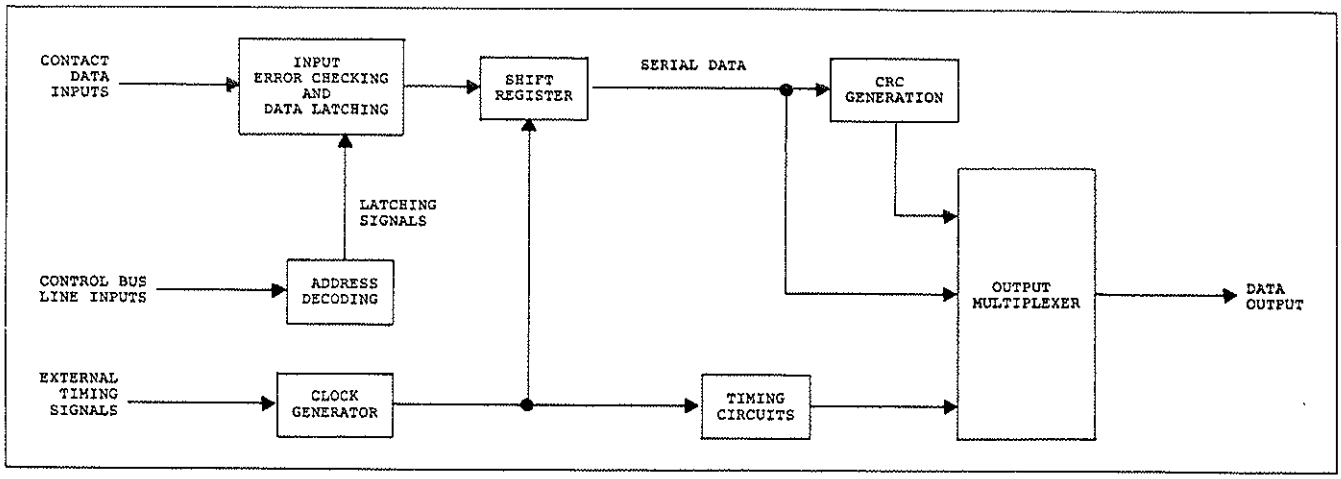


Figure 8-2. Block diagram, RFL 9700 digital transmitter modules

c. Serial Data Multiplexing. The serial data is multiplexed by quad analog switch U16. The switching action of U16 is controlled by dual binary up-counter U18 and flip-flop U11. The Q4A output of U18 (U18-6) generates a signal that is low for 8 bit-times, and high for 7 bit-times. U11 uses this signal to control the flow of data into the CRC generator and out of the multiplexer. U18's decoded outputs are used to generate the sync pulse and terminate the count cycle. The alternating sync bit is generated by the toggling of flip-flop U20. The sync bit controls when the multiplexer is enabled for transmission of the CRC code; it also controls the alternating sync bit. The output of the multiplexer is delayed for about 1 µs to remove any glitches incurred during the process. The data is then transmitted by quad line driver U23.

Table 8-1. Replaceable parts, RFL 9700 digital transmitter modules
RFL 97A DIG TX 56 (56-Kbps RS-449 operation) - Assembly No. 101565-2
RFL 97A DIG TX 64 (64-Kbps CCITT X.21 operation) - Assembly No. 101565-3

Circuit Symbol (Figs. 8-3 & 8-4)	Description	Part Number
	CAPACITORS	
C1	Capacitor,electrolytic,47µF,20%,16V,Nichicon ULB1C470M or equiv.	1007 1629
C2-8,10-12,15,17-35	Capacitor,X7R ceramic,0.01µF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C9	Capacitor,ceramic,100pF,5%,100V,AVX SA101A101JAA or equiv.	0125 11015
C13,14	Capacitor,ceramic,33pF,10%,100V,AVX SA101A330KAA or equiv.	0125 13301
	RESISTORS	
R1,2,8	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
R3,5	Resistor,metal film,68.1Ω,1%,1/4W, Type RN1/4	0410 1176
R4,10	Resistor,metal film,5.11KΩ,1%,1/4W, Type RN1/4	0410 1356
R6,7	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
RZ1,2	Resistor network,nine 10KΩ 2% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-103 or equiv.	32622
RZ3,4	Resistor network,five 100KΩ 2% resistors,0.75W total,6-pin SIP,Bourns 4306R-101-104 or equiv.	32665

Table 8-1. Replaceable parts, RFL 9700 digital transmitter modules - continued.

Circuit Symbol (Figs. 8-3 & 8-4)	Description	Part Number
	SEMICONDUCTORS	
U1	MOS octal tri-state D-type inverting latch,20-pin DIP,Texas Instruments SN74HC563N or equiv.	0615 307
U2,4	MOS octal tri-state D-type flip-flop,20-pin DIP,Motorola MC74HC574N or equiv.	0615 298
U3	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U5	MOS octal tri-state non-inverting buffer/line driver,20-pin DIP,National Semiconductor MM74HC541N or equiv.	0615 297
U6	MOS decoder,3-line to 8-line,16-pin DIP,National Semiconductor MM74HC138N or equiv.	0615 168
U7	MOS 8-bit magnitude comparator,20-pin DIP,National Semiconductor MM74HC688N or equiv.	0615 183
U8,11,20	MOS dual D-type flip-flop,14-pin DIP,RCA CD4013BE or equiv.	0615 1
U9	MOS quad Exclusive-OR gate,14-pin DIP,Motorola MC14070BCP or equiv.	0615 69
U10	MOS hex D-type flip-flop w/clear,16-pin DIP,National Semiconductor MM74HC174N or equiv.	0615 263
U12	MOS 8-stage static shift register,16-pin DIP,RCA CD4021BE or equiv.	0615 36
U13	MOS quad 2-input NOR gate,14-pin DIP,RCA CD4001BE or equiv.	0615 3
U14,19	MOS quad 2-input AND gate,14-pin DIP,RCA CD4081BE or equiv.	0615 31
U15	MOS shift register,8-bit,serial in/parallel out,16-pin DIP,National Semiconductor MM74HC164N or equiv.	0615 173
U16	MOS quad analog switch,14-pin DIP,Motorola MC14066BCP or equiv.	0615 246
U17	Not used.	
U18	MOS dual binary up-counter,16-pin DIP,RCA CD4520BE or equiv.	0615 28
U21,29-31	MOS dual D-type flip-flop w/preset and clear,14-pin DIP,National Semiconductor MM74HC74N or equiv.	0615 166
U22	MOS hex inverter,14-pin DIP,National Semiconductor MM74HC04N or equiv.	0615 185
U23	Quad line driver,RS-485,16-pin DIP,Texas Instruments SN75174N or equiv.	0680 15
U24	MOS hex inverter,unbuffered,high-speed,14-pin DIP,RCA CD74HCU04E or equiv.	0615 304
U25	Quad line receiver,RS-485,16-pin DIP,Texas Instruments SN75175N or equiv.	0680 16
U26	TTL retriggerable monostable multivibrator,14-pin ceramic DIP,Texas Instruments SN54LS123J or equiv.	0610 147
U27	MOS dual 4-bit binary counter,14-pin DIP,National Semiconductor MM74HC393N or equiv.	0615 192
U28	MOS quad 2-input NAND gate,14-pin DIP,National Semiconductor MM74HC00N or equiv.	0615 159
	MISCELLANEOUS COMPONENTS	
Y1	Crystal,quartz,frequency dependent upon model: RFL 97A DIG TX 56: 8.000 MHz RFL 97A DIG TX 64: 9.142857 MHz	 30161 101101
. . .	Shorting bar,single,Molex 90059-0009 or equiv.	98306

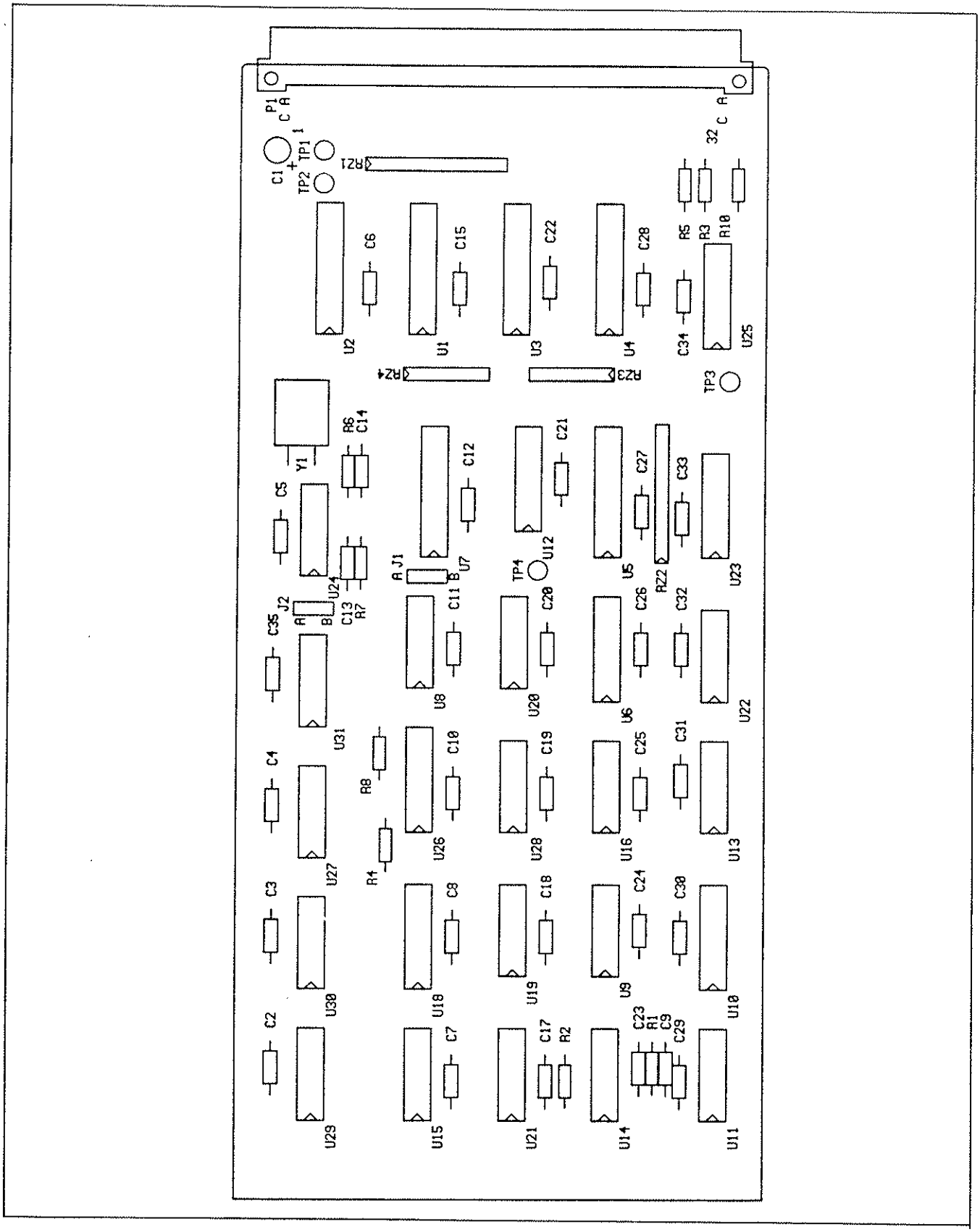


Figure 8-3. Component locator drawing, RFL 9700 digital transmitter modules (Assembly No. 101565-X; Drawing No. D-101568-1, Rev. A)

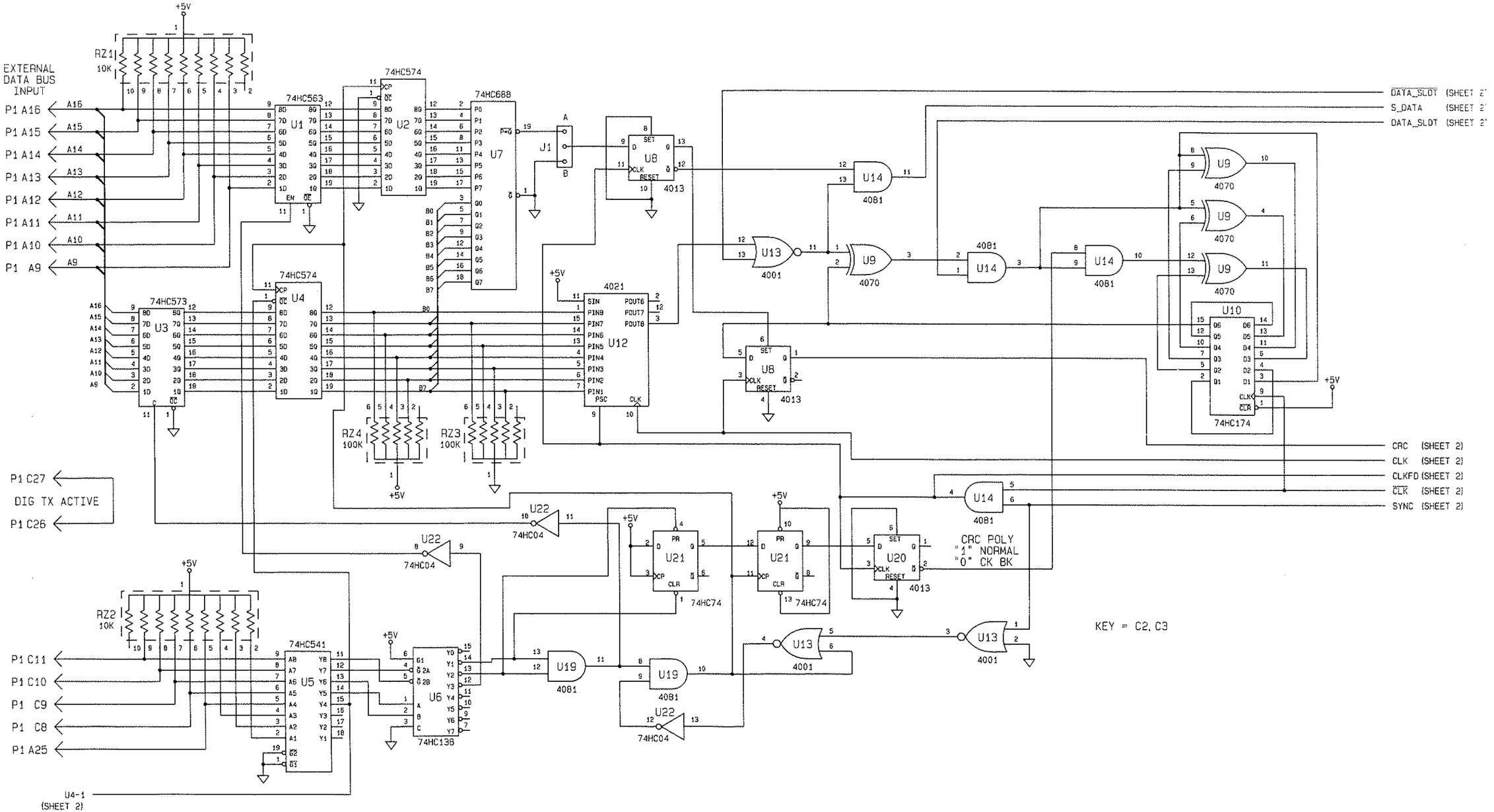
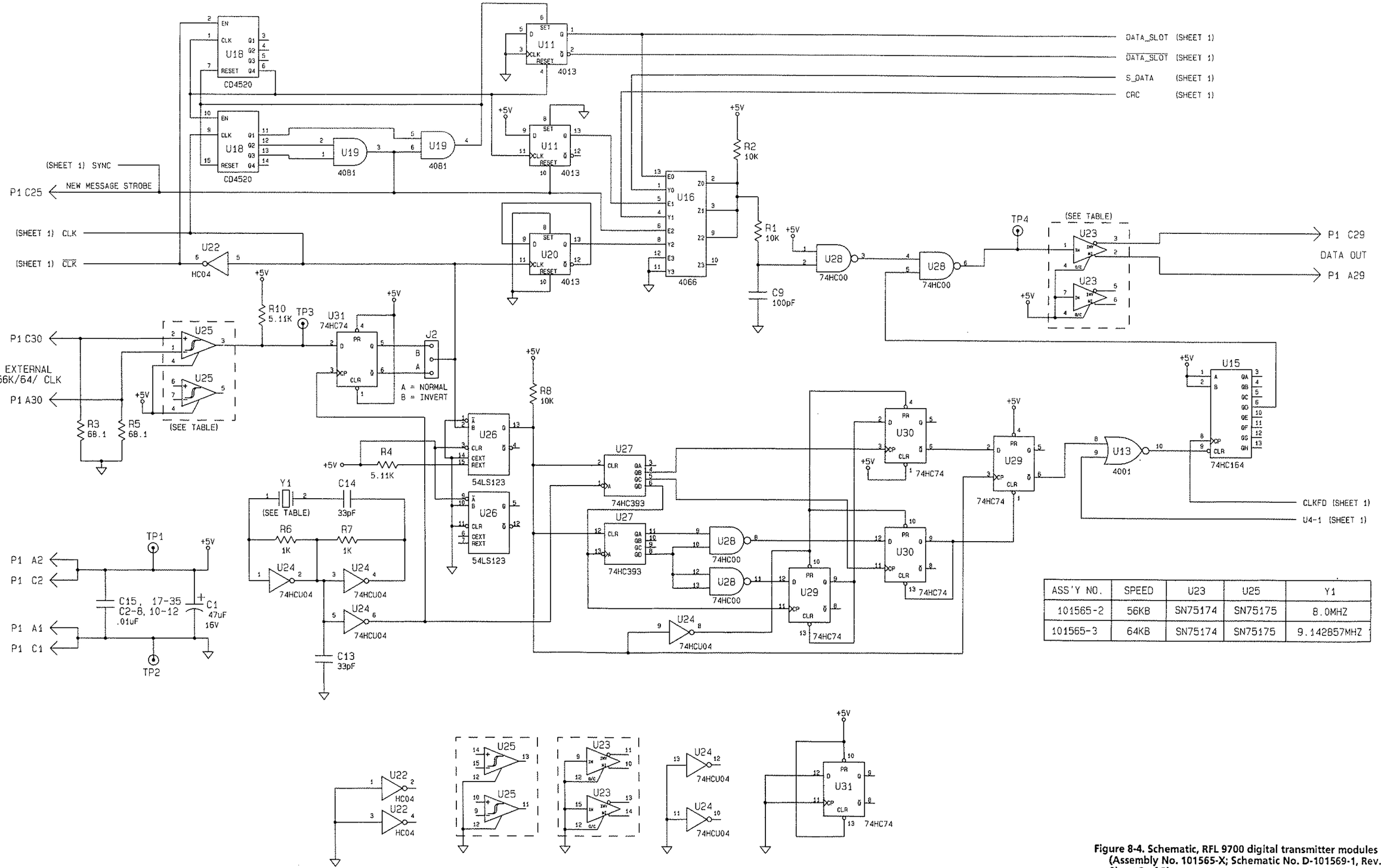


Figure 8-4. Schematic, RFL 9700 digital transmitter modules (Assembly No. 101565-X; Schematic No. D-101569-1, Rev. A - Sheet 1 of 2)



ASS'Y NO.	SPEED	U23	U25	Y1
101565-2	56KB	SN75174	SN75175	8.0MHZ
101565-3	64KB	SN75174	SN75175	9.142857MHZ

Figure 8-4. Schematic, RFL 9700 digital transmitter modules (Assembly No. 101565-X; Schematic No. D-101569-1, Rev. A - Sheet 2 of 2)

Section 9. DIGITAL RECEIVER MODULE

9.1. DESCRIPTION

RFL 9700 digital receiver modules are synchronous serial data receivers that separate the incoming data stream into its basic components (eight data bits and six CRC bits). They then check the CRC bits to be sure the incoming data is valid, and constantly monitor the incoming clock frequency. The CRC output status bits are used to notify the receiver CPU module (Section 10) that the received data and input clock are valid.

Two different digital receiver modules are available for the RFL 9700. The RFL 97A DIG RX 56 processes for 56-Kbps RS-422A data; the RFL 97A DIG RX 64 accepts 64-Kbps CCITT V.11 data. Both modules are self-contained, and do not require the receiver CPU or logic CPU modules to operate. Each digital receiver module occupies one dedicated module space in the RFL 97 CHAS chassis. A typical RFL 9700 digital receiver module is shown in Figure 9-1.

9.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to both RFL 9700 digital receiver modules, except as indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

External Clock Signals:

Signal Level:
- RFL 97A DIG RX 56: Meets the requirements of EIA Standard RS-422A.
- RFL 97A DIG RX 64: Meets the X.21 requirements of CCITT V.11.

Nominal Frequency:
- RFL 97A DIG RX 56: 55.72 to 56.28 kHz (56 kHz ±0.5 percent).
- RFL 97A DIG RX 64: 63.68 to 64.32 kHz (64 kHz ±0.5 percent).

Duty Cycle: 45 to 55 percent.

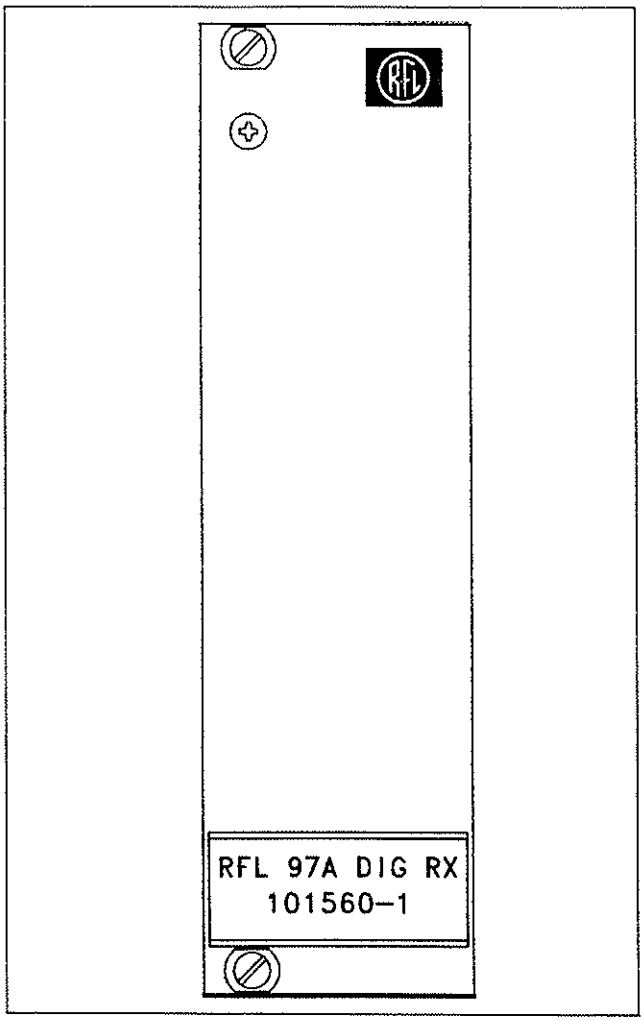


Figure 9-1. Typical RFL 9700 digital receiver module

Serial Data:

Signal Level:
- RFL 97A DIG RX 56: Meets the requirements of EIA Standard RS-422A.
- RFL 97A DIG RX 64: Meets the X.21 requirements specified in CCITT V.11.

Nominal Data Rate:
- RFL 97A DIG RX 56: 56 Kbps.
- RFL 97A DIG RX 64: 64 Kbps.

Data Format: 8 data bits, 6 CRC bits, 1 sync bit; most-significant data bit received first, sync bit must alternate with each word.

Output Signal Level: CMOS logic levels (logic high 3.15 Vdc minimum, logic low 0.9 Vdc maximum).

Output Load Resistance: 10,000Ω pull-up to +5-volt supply.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements: 4.75 to 5.25 Vdc @ 175 mA; obtained from chassis power supply.

Dimensions:
Panel Height: 5.1 inches (130 mm).
Panel Width: 1.4 inches (36 mm).
Depth (behind panel): 9.1 inches (231 mm).

9.3. THEORY OF OPERATION

RFL 9700 digital receiver modules are synchronous serial data receiver that synchronize themselves to the incoming data stream. Once synchronized, they separate the eight-bit data word from the six-bit CRC code, and translates them into outputs that are passed on to the receiver CPU module (Section 10). A block diagram for both RFL 9700 digital receiver modules appears in Figure 9-2.

a. Input Signal Processing. The serial data and the external 56-kHz clock signal are accepted by line receiver U29, and converted to CMOS logic levels. Changes in data state will occur at the falling edge of the clock signal. The data is then strobed into shift registers U27 and U28, on the rising edge of the clock signal. U27 and U28 are connected in series, to form a single 16-bit register.

After the entire 15-bit word has been received and if synchronization has been achieved, the eight data bits will be present at outputs Q_A through Q_G of U27, and Q_H of U28. Q_H of U27 will hold the previously-received sync bit, and Q_A of U28 will hold the current sync bit.

b. Sync Detector. If the digital receiver module is synchronized to the incoming data stream, one sync bit will be high, and the next sync bit will be low. The sync bits are the only ones that can change from one message interval to the next, so they are easily detected. Pin 3 of Exclusive-OR gate U9 will set the D input of shift register U12 (U12-12) to a logic zero when they detect the alternating sync bit. The rising edge of four-bit counter U33's CARRY output will then strobe the data into latch U10; the sync status will be strobed into U12. As long as the sync pulses are alternating properly, the Q output of U12 will be low and U10's outputs will be enabled. This allows the data to flow into transparent inverting latch U41.

The outputs of U41 drive edge connector pins P1-C17 through P1-C24; these are passed over the backplane to the receiver CPU module, where they are fed into its contact input latch. (The signal on P1-C17 corresponds to the status of Channel 8, and the signal on P1-C24 to Channel 1.) If the sync signals are incorrect, the Q output of U12 will be high; U10's outputs will be forced to the high-impedance state and disabled. The pull-up and pull-down resistors in resistor networks RZ1 and RZ2 will then control U41's input; they are arranged to produce an all no-trip code.

As described above, U12-9 will be low as long as synchronization is maintained. This signal is applied to the CLEAR input of binary counter U32, disabling it and preventing its CARRY output from going high. This maintains the feedback path through inverter U30 that provides the ENABLE input (E_P). The low CARRY signal and the sync signal from U12 are applied to a 3-input NAND gate in U34, forcing the A input of four-bit binary counter U33 (U33-3) high. This will force U33 to reload its data inputs following a 15-count cycle. U33's CARRY output will reload its own inputs through inverter U30 and strobe the latest data and status bits into the output latches.

To prevent a loss of sync in the event of an occasional sync bit being lost in transmission, binary counter U32 is clocked on the falling edge of the incoming clock signal, as long as it is enabled by U33's CARRY output. If synchronization is lost, U12-9 will go high, removing the CLEAR signal from U32. If the sync loss persists for sixteen message intervals, the CARRY output of U32 will go high, and it will be disabled by the feedback to its E_P input. Once this occurs all three inputs to NAND gate U34 will be high every time the CARRY output of U33 goes high, and the load count for U33 will change to zero. U33 will now go through a 16-count cycle before strobing the data and status latches.

Since the input message consists of 15 clock cycles, the receiver will "slip sync" by one clock cycle for every 16 received, until it gets back into sync with the incoming data stream. As soon as sync is re-established, the CLEAR signal is applied to U32 through U12, and U33 resumes its 15-count cycle.

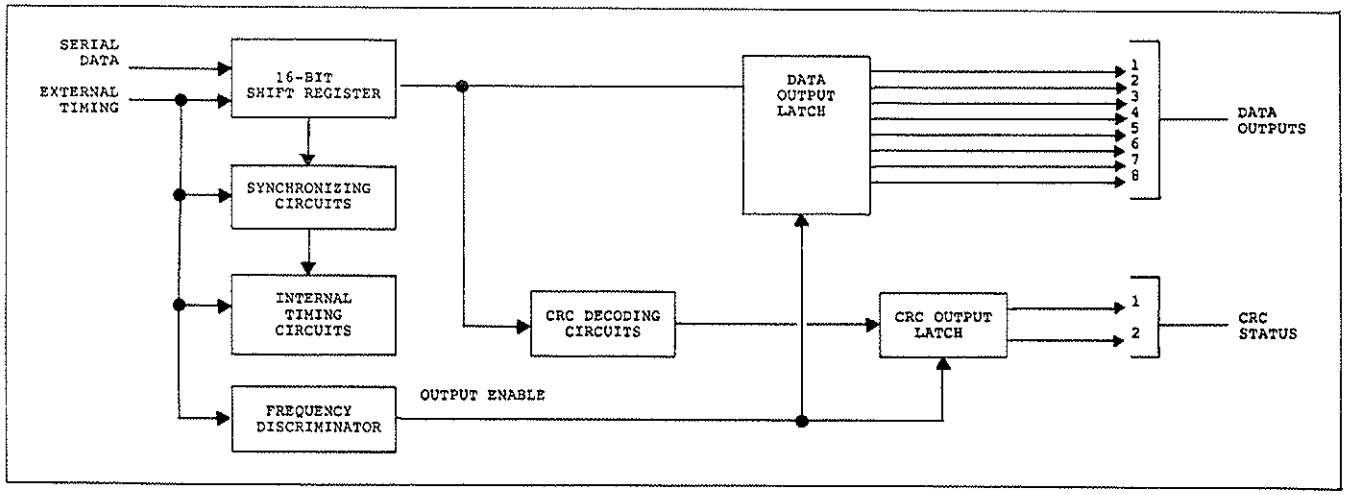


Figure 9-2. Block diagram, RFL 9700 digital receiver modules

c. Output Strobing. The rising edge of the new message strobe at U9-11 will occur at the same time as the falling edge of the clock signal at pin 5 of line receiver U29, and the rising edge of the U33 CARRY output signal (U33-15). With these three events occurring at the same time, the data will be strobed into U10 and the CRC status will be strobed into U12 and U13.

The new message strobe originating on the digital receiver module is only used in receive-only terminals, where it provides the interrupt pulse for the receiver CPU and logic CPU modules. In these terminals, jumper J1 is placed in the IN position; this jumper is placed in the OUT position in transmit-receive terminals, because the interrupt pulse will be provided by the digital transmitter module (Section 8).

d. CRC Code Detection And Calculation. The CRC bits included with the received message represent the remainder that resulted when the data byte was divided by the generator polynomial on the digital transmitter module. In order to verify that the received data is correct, the received 14-bit string (the eight data bits plus the six CRC bits) must be divided by the same polynomial, using a process called "modulo-2 arithmetic." This is done by a circuit formed from Exclusive-OR gates U7 and U8, NOR/OR gates U22 and U23, hex flip-flops U25 and U26, and flip-flops U12 and U13. At the same time, the 14-bit string is passed through the checkback divider formed from U8 and U25, and the normal data divider formed from U7 and U26. If all the inputs to U23 are low when the CRC output clock goes high, CRC1 (edge connector P1-C31) will be low, indicating that the data was normal and error-free. If all the inputs to U22 are low when the CRC output clock goes high, CRC2 (edge connector P1-C30) will be low, indicating that error-free checkback data was received.

e. Timing Signal Verification. Both digital receiver modules rely heavily on the integrity of the clock signals supplied by external equipment. A frequency discriminator is used to insure that these signals are correct; it is formed from multivibrator U35, inverter U36, binary counter U37, NAND gate U38, and flip-flops U39 and U40. This circuit measures the elapsed time between falling edges of the input clock signal, making sure the clock frequency is within limits (55.72 to 56.28 kHz for the RFL 97A DIG RX 56, or 63.68 to 64.32 kHz for the RFL 97A DIG RX 64). If the frequency exceeds these limits, U13-9 will go low for at least one bit time (about 18 µs), and both latches in U40 will clear. This will cause U12-9 to go high, just as it does when the module goes out of sync. Since U40 is clocked at the same rate as the new message strobe, the digital receiver module's outputs will be disabled for two message intervals, plus whatever time it takes for sync to be re-established. While this condition persists, both CRC outputs will be high, indicating a communications error.

U41 is a programmable logic device (PLD). It is programmed at the factory to invert the input signals on alternate channels. Data is transmitted from the remote station with alternate bits inverted. A no-trip code is transmitted as AAH. This code must be converted back to the proper format on the digital receiver module to produce the no-trip output code FFH. U41 performs this conversion by effectively combining the received data with 55H in an Exclusive-OR gate. This must be done because the receiver CPU module has pull-up resistors on its data inputs, and they are connected to U41's outputs. Without this for-

mat change, the receiver CPU module could read a trip on alternate channels if the digital receiver module was removed from the chassis with the power on.

f. Summary Of Operation. In summary, the following conditions apply to the digital receiver module's operation:

1. Once the received data has been latched into output data latch U41, the latch outputs will remain unchanged unless there is a change in data or a loss of sync.

2. The new message strobe and the CRC output status will only change state on the rising edge of the CRC output clock signal.

3. The CRC status outputs will remain constant (CRC1 low and CRC2 high) as long as normal data is being received.

4. When checkback data is received, CRC1 goes high and CRC2 goes low. If the system is functioning properly, this condition will only persist for one message interval (about 267 μs in 56-Kbps terminals, and 234 μs in 64-Kbps terminals).

5. If the digital receiver module loses sync with the incoming serial data, CRC1 and CRC2 will both go high, and the data output code at pins P1-C17 through P1-C24 will equal AAH, with the most-significant bit on P1-C17.

6. If the external clock frequency is less than 54 kHz or more than 57.5 kHz for the RFL 97A DIG RX 56 (or less than 62.8 kHz or more than 64.3 kHz for the RFL 97A DIG RX 64), CRC1 and CRC2 will both go high, and the data output code at pins P1-C17 through P1-C24 will equal AAH, with the most-significant bit on P1-C17.

7. If the received serial data byte equals ØØH, 4ØH, 81H, or C1H and the corresponding CRC code is correct, CRC1 and CRC2 will both go low, whether normal data or checkback data is being received.

Table 9-1. Replaceable parts, RFL 9700 digital receiver modules
RFL 97A DIG RX 56 (56-Kbps RS-449 operation) - Assembly No. 101560-1
RFL 97A DIG RX 64 (64-Kbps CCITT X.21 operation) - Assembly No. 103545-1

Circuit Symbol (Figs. 9-3 & 9-4)	Description	Part Number
	CAPACITORS	
C1,2,4-6,26	Not used.	
C3,9-22,25,27-29, 42,47	Capacitor,X7R ceramic,0.01μF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C7	Capacitor,tantalum,1μF,20%,35V,Kemet T322B105M035AS or equiv.	1007 496
C8	Capacitor,ceramic,0.001μF,5%,100V,AVX SA201A102JAA or equiv.	0125 11025
C23,24	Capacitor,ceramic,33pF,5%,100V,AVX SA101A330JAA or equiv.	0125 13305
	RESISTORS	
R1-4	Resistor,metal film,68.1Ω,1%,1/4W, Type RN1/4	0410 1176
R5-7	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R8,14-19	Resistor,metal film,5.11KΩ,1%,1/4W, Type RN1/4	0410 1356
R9-13	Not used.	
RZ1,2	Resistor network,five 100KΩ 2% resistors,0.75W total,6-pin SIP,Bourns 4306R-101-104 or equiv.	32665

Table 9-1. Replaceable parts, RFL 9700 digital receiver modules - continued.

Circuit Symbol (Figs. 9-3 & 9-4)	Description	Part Number
	SEMICONDUCTORS	
U1-6,11,14-21,24,31	Not used.	
U7-9	MOS quad 2-input Exclusive-OR gate,14-pin DIP,National Semiconductor MM74HC86N or equiv.	0615 268
U10	MOS octal tri-state D-type flip-flop,20-pin DIP,Motorola MC74HC574N or equiv.	0615 298
U12,13,39,40,42	MOS dual D-type flip-flop w/preset and clear,14-pin DIP, National Semiconductor MM74HC74N or equiv.	0615 166
U22,23	MOS 8-input NOR/OR gate,14-pin DIP,National Semiconductor MM74HC4078N or equiv.	0615 184
U25,26	MOS hex D-type flip-flop w/clear,16-pin DIP,National Semiconductor MM74HC174N or equiv.	0615 263
U27,28	MOS shift register,8-bit,serial in/parallel out,16-pin DIP, National Semiconductor MM74HC164N or equiv.	0615 173
U29	Quad line receiver,16-pin DIP,standard compliance and type dependent upon model: RFL 97A DIG RX 56: RS-422; Motorola MC3486P or equiv. RFL 97A DIG RX 64: RS-485; Texas Instruments SN75175N or equiv.	0680 9
U30	MOS hex inverter,14-pin DIP,National Semiconductor MM74HC04N or equiv.	0615 185
U32,33	MOS synchronous binary counter,16-pin DIP,National Semiconductor MM74HC163N or equiv.	0615 154
U34	MOS triple 3-input NAND gate,14-pin DIP,National Semiconductor MM74HC10N or equiv.	0615 162
U35	Retriggerable monostable multivibrator,14-pin ceramic DIP,Texas Instruments SN54LS123J or equiv.	0610 147
U36	MOS hex inverter,unbuffered,high-speed,14-pin DIP,RCA CD74HCU04E or equiv.	0615 304
U37	MOS dual 4-bit binary counter,14-pin DIP,National Semiconductor MM74HC393N or equiv.	0615 192
U38	MOS quad 2-input NAND gate,14-pin DIP,National Semiconductor MM74HC00N or equiv.	0615 159
U39	MOS dual D-type flip-flop,14-pin DIP,Samsung KS74AHCT74N or equiv.	0615 314
U41	Programmable logic aray (PAL), programmed at factory	Contact factory
	MISCELLANEOUS COMPONENTS	
Y1	Crystal,quartz,frequency dependent upon model: RFL 97A DIG RX 56: 8.0 MHz RFL 97A DIG RX 64: 9.142857 MHz	 30161 101101
. . .	Shorting bar,single,Molex 90059-0009 or equiv.	98306

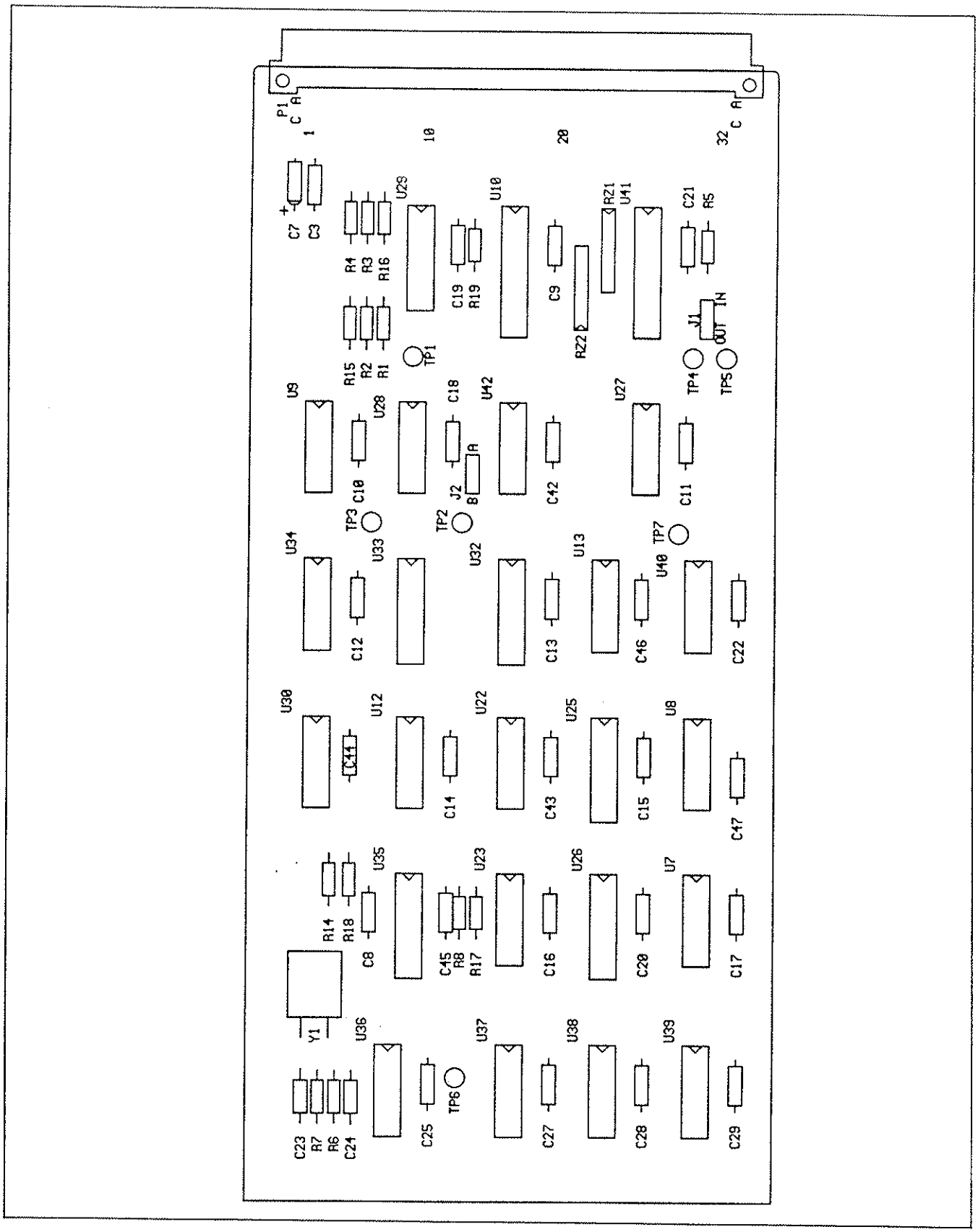
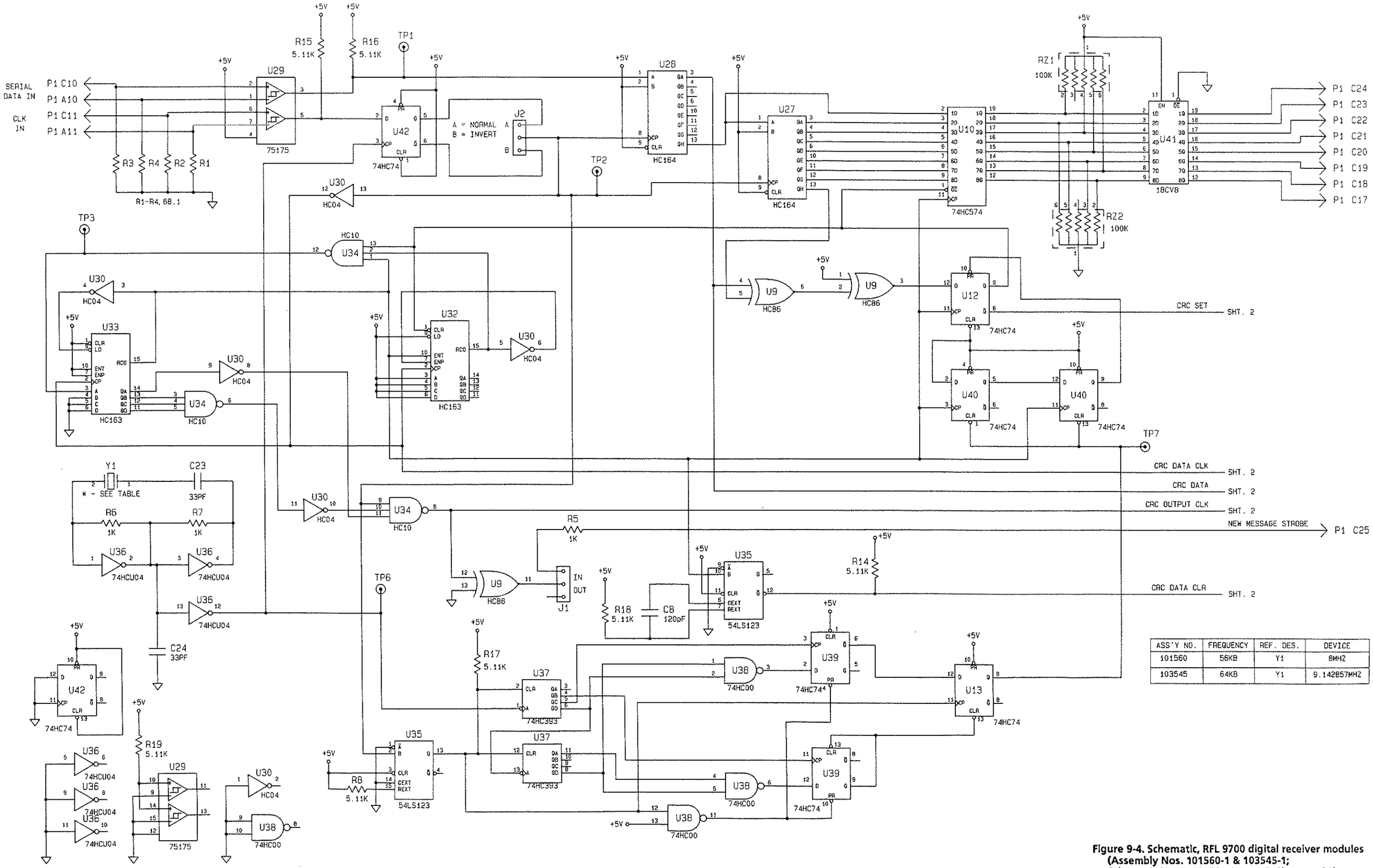


Figure 9-3. Component locator drawing, RFL 9700 digital receiver modules (Assembly Nos. 101560-1 & 103545-1; Drawing No. D-101563-1, Rev. A)



ASS'Y NO.	FREQUENCY	REF. DES.	DEVICE
101560	56KB	Y1	8MHZ
103545	64KB	Y1	9.142857MHZ

Figure 9-4. Schematic, RFL 9700 digital receiver modules (Assembly Nos. 101560-1 & 103545-1; Schematic No. D-101564-1, Rev. E, Sheet 1 of 2)

IC POWER CONNECTIONS

IC	+5V	GND
U7	14	7
U8	14	7
U9	14	7
U10	20	10
U12	14	7
U13	14	7
U22	14	7
U23	14	7
U25	16	8
U26	16	8
U27	14	7
U28	14	7
U29	16	8
U30	14	7
U32	16	8
U33	16	8
U34	14	7
U35	16	8
U36	14	7
U37	14	7
U38	14	7
U39	14	7
U40	14	7
U41	20	10
U42	14	7

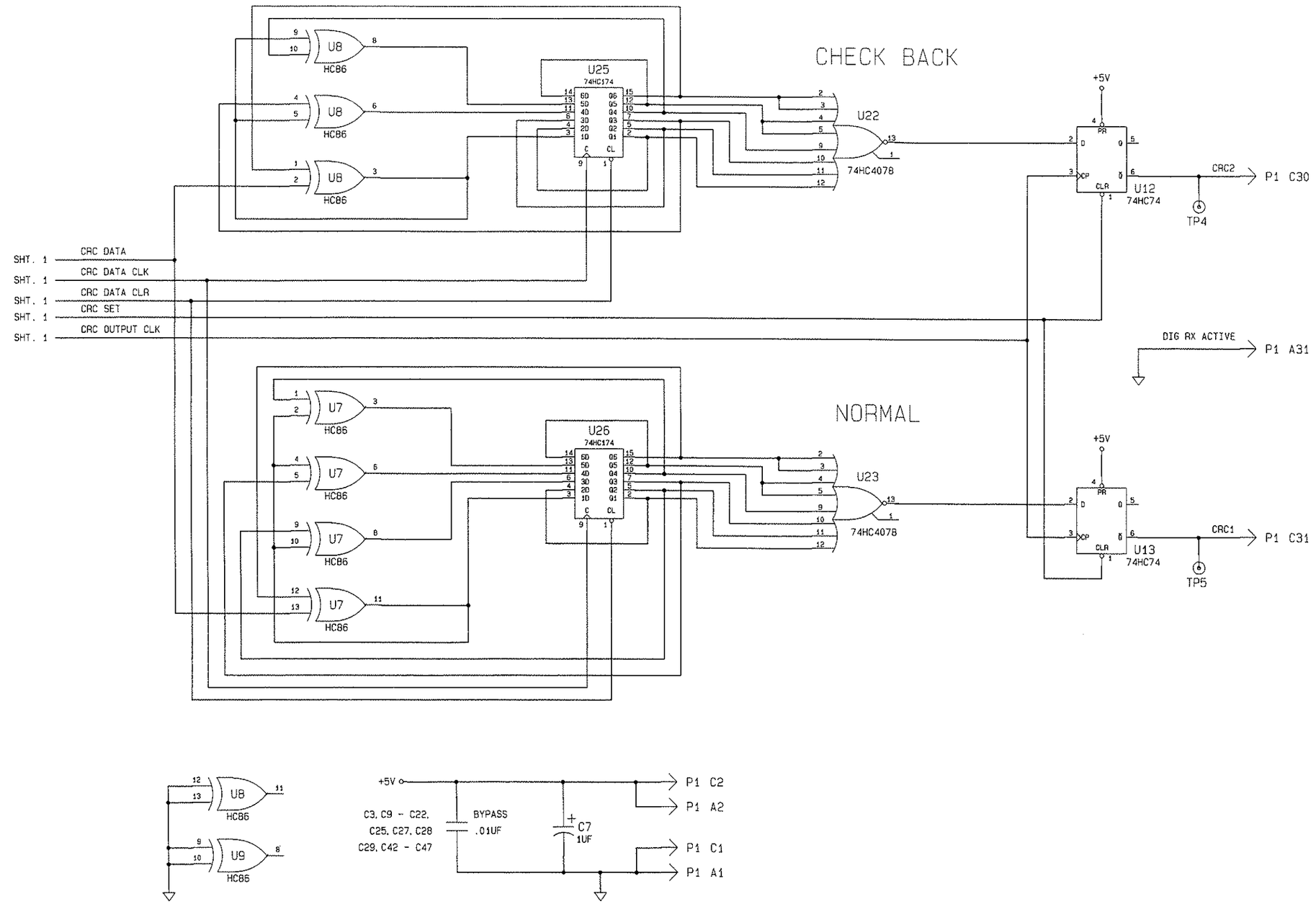


Figure 9-4. Schematic, RFL 9700 digital receiver modules (Assembly Nos. 101560-1 & 103545-1; Schematic No. D-101564-1, Rev. E, Sheet 2 of 2)

Section 10. RECEIVER CPU MODULE

10.1. DESCRIPTION

The RFL 97A RX CPU Receiver CPU Module (Fig. 10-1) accepts the decoded information from the digital receiver module (Section 9), and decides the acceptance criteria for the incoming message. Once this is done, it converts the message into eight-bit parallel data, which is passed to the logic CPU module (Section 11). Checkback testing is performed by the RFL 97A RX CPU, and an array of sealed-in LED indicators on its front panel provide a visual indication of checkback failures. The RFL 97A RX CPU occupies one dedicated module space in the RFL 97 CHAS chassis.

10.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to the RFL 97A RX CPU module. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Signal Level: CMOS logic levels (logic high 3.15 Vdc minimum, logic low 0.9 Vdc maximum).

Input Load Resistance: 10,000Ω pull-up to +5-volt supply.

Output Signal Level: CMOS logic levels (logic high 3.15 Vdc minimum, logic low 0.9 Vdc maximum).

Output Load Resistance:
Outputs Driven By 74HC-Type Devices: 10,000Ω pull-up to +5-volt supply.
Outputs Driven By KS74AHCT-Type Devices: 2,000Ω pull-up to +5-volt supply.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements: 4.75 to 5.25 Vdc @ 275 mA; obtained from chassis power supply.

Dimensions:
Panel Height: 5.1 inches (130 mm).
Panel Width: 1.4 inches (36 mm).
Depth (behind panel): 9.1 inches (231 mm).

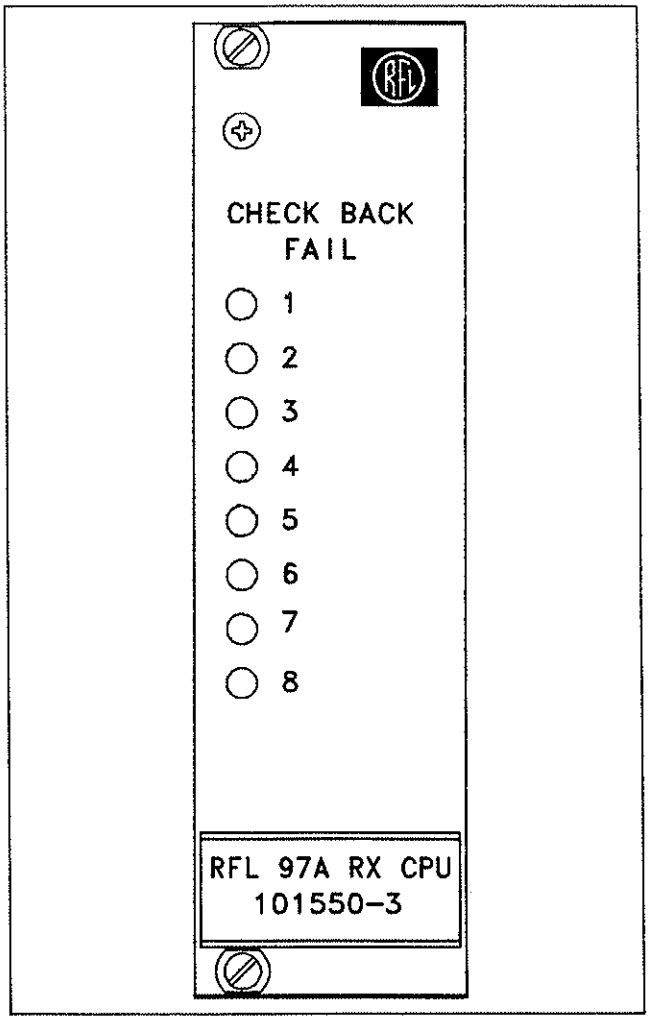


Figure 10-1. RFL 97A RX CPU Receiver CPU Module

10.3. HARDWARE DESCRIPTION

The RFL 97A RX CPU is an 8-MHz microcomputer, based on the Z-80 microprocessor. It is designed to handle the system communication tasks. Data received from the digital receiver module is checked for errors, processed, and passed on to the logic CPU module. The RFL 97A RX CPU module also conducts all checkback tests and reports the test results to the logic CPU module (Section 11). Four DIP switches on the RFL 97A RX CPU module configure it for the desired security and dependability levels, addressing, and data rate. A block diagram of the RFL 97A RX CPU module can be found in Figure 10-2.

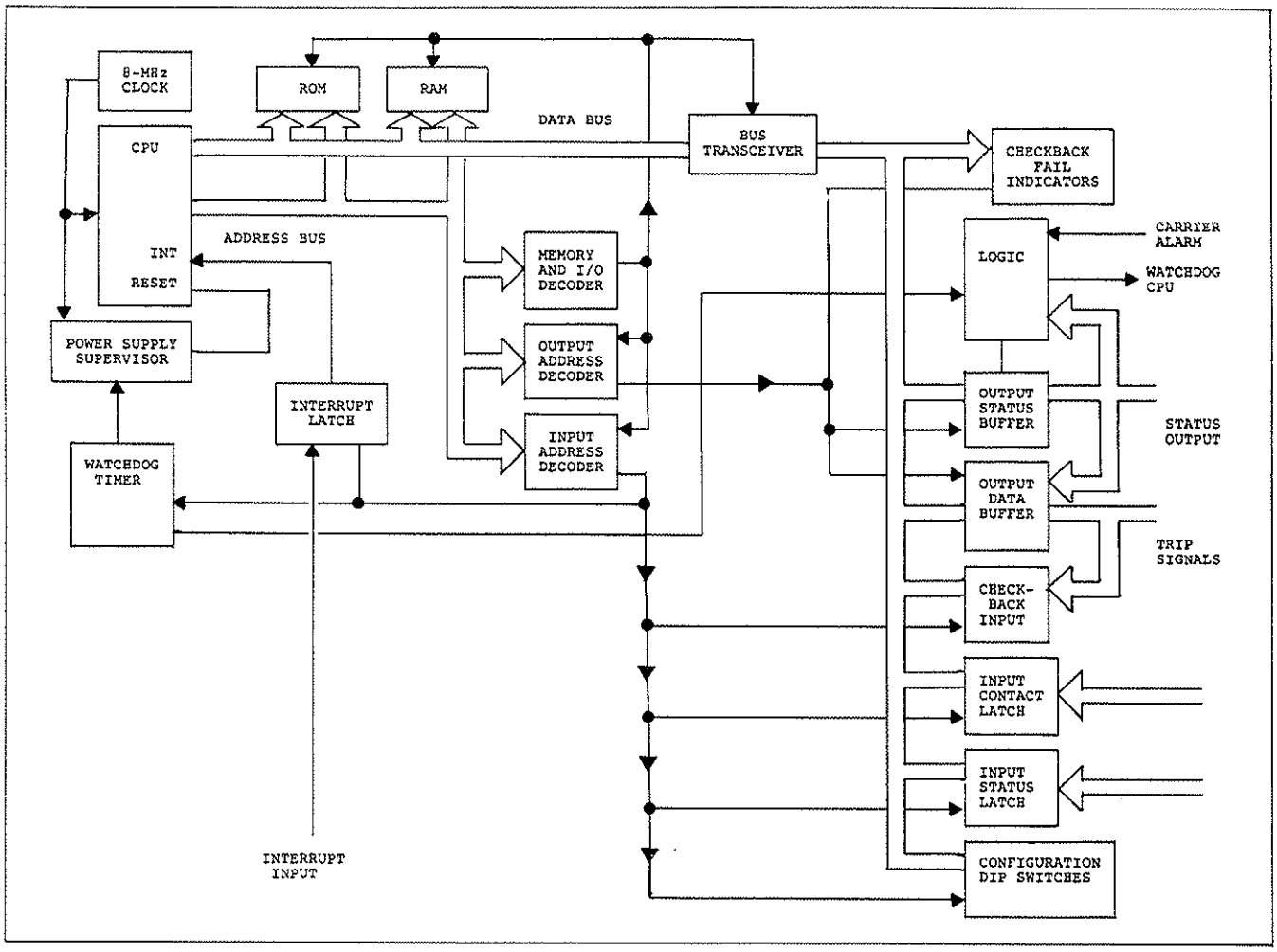


Figure 10-2. Block diagram, RFL 97A RX CPU Receiver CPU Module

10.3.1. Program Storage EPROM

The RFL 97A RX CPU module's operating program is stored in EPROM U2. Jumper ABC allows several EPROM types to be used for U2; 8K x 8 or 16K x 8 devices can be used when the jumper is in the A-B position, and 32K x 8 devices can be used when it is in the B-C position. The EPROM used must be capable of operating over the specified temperature range for the module (para 10.2). Address decoder U17 is only capable of decoding memory address locations from 0000 through 3FFFH, so the upper 16K of memory in 32K x 8 EPROM devices will not be accessible. Jumper DEF must be placed in the D-E position, or this chip will be disabled.

10.3.2. Static RAM

U3 is a CMOS static RAM, used as a "scratchpad" memory to store temporary system parameters as the RFL 97A RX CPU performs its functions. The decoded address range for U3 is 4000H to 47FFH. Three different device types can be installed for U3: 2K x 8, 8K x 8, or 32K x 8. Two sets of holes are provided on the circuit board to accommodate devices with 0.300-inch pin spacings or 0.600-inch spacings. Jumper RS sets the module for the device type being used; position S for 2K x 8 devices, and position R for the others. The device used must be CMOS, must operate over the module's entire operating temperature range (para 10.2), and must have an address access time of 150 ns or less.

10.3.3. Microprocessor

Z-80 microprocessor U1 is responsible for executing the control program. It features a non-multiplexed address/data bus configuration, with 16 address lines and 8 data lines. U1 requires an 8-MHz clock signal, which is produced by the oscillator circuit formed from

inverter U19, capacitors C21, resistors R5 and R6, and crystal Y1. Resistors R1 through R3 and capacitor C18 form a high-speed, low-loss driver circuit; it is required to provide a fast rise time for the clock while insuring that the signal's high limit is no more than 0.6 volts below V_{CC}, and no more than 0.3 volts above V_{CC}. Jumper JKL determines whether the oscillator circuit's output is used to clock U1 (position J-K), or if an external clock source is used (position K-L). For normal operation, the jumper should be placed in the J-K position.

The RESET signal for U1 is supplied by U18-5 (the Q output of D-type flip-flop U18). This active-low signal is produced as a result of either a CLEAR signal produced by microprocessor supervisor U22 or a logic low applied to U18-2 by the watchdog timer circuit (para 10.3.8).

10.3.4. Address Decoding

3-line to 8-line decoder/demultiplexer U17 decodes the EPROM and static RAM memory addresses. It also decodes the memory-mapped addresses of the I/O devices, and controls the G1* output enable and DIR direction signals for bus transceiver U4. When the RD* (read) signal on U1-21 goes low and the Y4 output of U17 is selected, U15-11 goes low. This sets U4 to allow data to flow from the I/O ports to U1 along the internal data bus. At all other times, data flows from U1 to the I/O ports. The output buffers in U4 will be in the high-impedance state unless an I/O address is decoded and the Y4 output of U17 goes low to enable them.

10.3.5. Input Ports

Octal D-type latches U7 through U11, U23, and U24 provide the RFL 97A RX CPU with seven input ports. They are all equipped with pull-up resistors, which guarantee a logical one when no driving source is present.

U7 and U8 interface with the digital receiver module (Section 9); the received trip signals are loaded into U7, while the CRC status bits are loaded into U8. U8 also receives the active-high CARRIER ALARM signal from the optional fiber optic receiver module (Section 13), and the CHECKBACK FAILURE RESET* signal from the transmitter interface module (Section 7). U9 provides a means for microprocessor U1 to read back the output latch contents during checkback testing.

U10 and U11 interface with DIP switches S1 and S2, which are used to program system security and dependability. S1 and S2 are read at program start-up, and any time the RFL 9700 is recovering from an interval of noise on the communications line. (See paragraph 3.3.4h in Section 3 for more information on setting S1 and S2.)

U23 and U24 interface with DIP switches S4 and S5, which control the addressing configuration and data rate. S4 and S5 are read every time a new message arrives. (See paragraphs 3.3.4i through 3.3.4k in Section 3 for more information on setting S4 and S5.)

10.3.6. Latches

During normal operation, the digital transmitter module (Section 8) will provide an interrupt pulse at the start of each new message interval. If the RFL 9700 is set up for receive-only operation, the interrupt pulse will be provided by the digital receiver module. In either case, the pulse will clock U21-6 (the Q* output) low on its rising edge; this provides the interrupt signal for microprocessor U1. At the start of the interrupt routine, U1 will use address decoder U13 to clear the interrupt by addressing output Y5 (port address 8085H). This will result in an active-low CLEAR signal being applied to U21-1, which can be monitored at test point TP2. The pulses at TP2 should be spaced at 268-µs intervals.

Once the interrupt latch is cleared, the processor inputs the status byte from U8 and the received trip byte from U7. These latches are accessed through U13, which decodes the port address supplied by U1 and then delivers an active low signal to the output enable input of the desired latch (OE*, pin 1).

10.3.7. Microprocessor Supervisor

U22 is a microprocessor supervisor, which provides the power-up reset signal. It also resets U1 if the 5-volt supply line falls below U1's reset voltage threshold, which is normally 4.5 to 4.75 Vdc.

A reset will also occur if the internal watchdog timer's input is not strobed at least once every 1.6 seconds. During normal operation, a READ from Address 8080 will reset the timer input well within the 1.6-second interval. This adds a great deal of power brown-out immunity to the system. U22 will hold the RESET signal low for at least 50 ms after the supply voltage returns to a value above the reset voltage threshold.

10.3.8. Watchdog Timer

The OE* signal supplied to latch U8 is also fed to U20-2, which is the positive-going B trigger input of one of the retriggerable multivibrators in U20. These multivibrators serve as the "watchdog timer" for microprocessor U1. Each time U8 is read, the first multivibrator is triggered and its 1500-µs time-out period is restarted. When the RFL 9700 is functioning normally, this multivibrator will be retriggered before it has a chance to time out, so its output will never change state.

If for any reason the input trigger signal is not received, the first multivibrator will time out and the ALARM signal (which can be monitored at test point TP3) will go high. This is a fatal alarm, since the watchdog CPU signal will become active through OR gate U15. At the same time, the second multivibrator in U20 will be triggered (on the rising edge of the ALARM signal, through U20-10). When the second multivibrator is clocked, a 60-µs low-going strobe is applied to U18-2, forcing U18 to reset the microprocessor.

10.3.9. Output Ports

Octal tri-state flip-flops U5, U6, and U12 provide the RFL 97A RX CPU with three output ports, which are controlled by decoder U16. When U16 decodes one of the output ports' address codes, one of its outputs will go low. These lows are inverted by hex inverter U14 to supply a clock signal to the target latch's CLK input (pin 11). U12 is clocked by U16's Y0 output (U16-15), U5 by the Y1 output (U16-14), and U6 by Y2 (U16-13).

U12 provides the drive current necessary to light CHECKBACK FAILURE indicator arrays DS1 and DS2 on the RFL 97A RX CPU's front panel. Each indicator requires about 11 mA to light; resistor network RZ7 limits the current through the indicators.

System status signals are output to U5. These signals indicate the results of processing the input signals supplied by the digital receiver module. The MEMORY FAIL* and TRANSMISSION FAIL* signals are supplied to the indicator/output module (Section 12). The CHECKBACK OK signal is a low-going strobe sent to the transmitter interface module (Section 7), where it strobes the CHECKBACK PASSED latch. This signal is the result of a successful checkback test; if the test fails, no indication is given.

The CARRIER ALARM signal supplied by the fiber optic receiver module (Section 13), along with the watchdog timer ALARM signal, is applied directly to the READY* output (edge connector terminal P1-C11), through two OR gates in U15 and jumper M-N. The READY* signal is passed over to the logic CPU module's status input latch; it signals that the RFL 97A RX CPU module has detected a serious problem. This high-going signal is also applied to U6's OUTPUT ENABLE input (OE*, U6-1).

Jumper TU controls the RFL 9700's addressing feature. This jumper is placed in position T to enable the addressing feature, or position U to disable it.

U6 controls the contact outputs. If U6-1 goes high, all the contact output signals are immediately de-energized.

U16's Y5 output (U16-10) becomes the CPU ACTIVE* signal at edge connector terminal P1-C16. This signal is passed over to the logic CPU module and applied directly to its input status latch. When this constantly-low signal is detected, it means that the RFL 97A RX CPU module is present. If jumper ABC on the transmitter interface module is set to enable receiver software functions and CPU ACTIVE* is not low, a fatal alarm will result and the RFL 9700 will go off-line. The RFL 9700 will also go off-line if receiver functions are not enabled and this signal is detected.

When jumper TU is placed in position T, the signal at U5-19 becomes the ADDR TX signal. This enables the RFL 97A RX CPU to notify the logic CPU module that an address has been received from the remote station.

10.4. SOFTWARE DESCRIPTION

Paragraphs 10.4.1 through 10.4.6 provide a basic description of the assembly-language program used to control operations on the RFL 97A RX CPU module. An overall flow chart for the control program appears in Figure 10-3.

10.4.1. Program Structure

The program executive structure is a ring composed of the following program blocks:

1. Initialization Block
2. Primary Input Data Block
3. Primary Input Data Processing Block
4. Secondary Input Data Block
5. Output Data Block

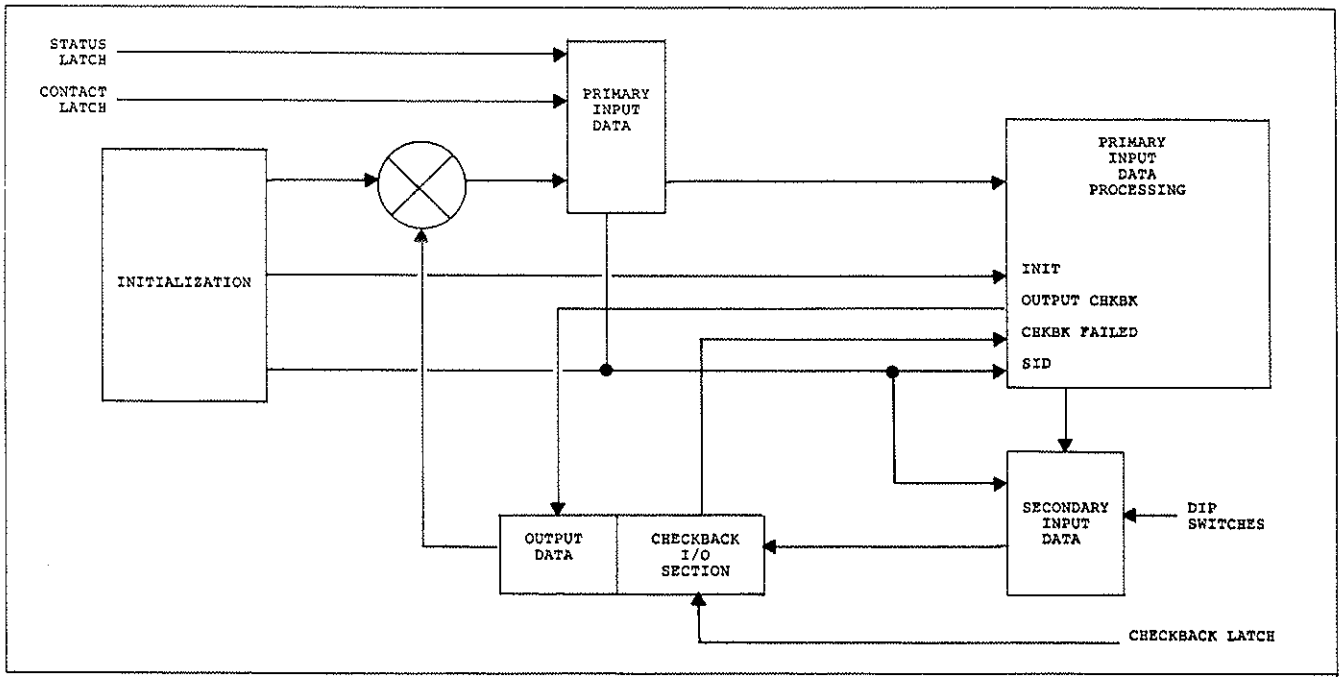


Figure 10-3. Flow chart, RFL 97A RX CPU Receiver CPU Module

On start-up, the program enters the Initialization Block. Once the Initialization Block is completed, a HALT instruction is issued and the program waits for an interrupt to occur. When is does, control passes to the Primary Input Data Block (para 10.4.3).

When control is passed to a block, the first action taken is a check of the Block Enable Register. Each block is assigned an enable bit in this register. If the bit is set, the block program will proceed. When the block has been executed, it resets its own enable bit and sets the enable bit of the program block it wants to activate next. Control will then be pass to the newly-activated program block.

There are two exceptions to the above process. The Primary Input Data Block is enabled by the initialization routine at the start of the program, and this block always remains enabled. The Primary Input Data Processing Block is also enabled at all times. There is no need for these blocks to take the time to check the Block Enable Register; computing time is critical.

10.4.2. Initialization Block

The Initialization Block is entered when the RFL 97A RX CPU module is powered up, or any time the watchdog timer times out. All output latches will be set up so that all outputs, alarms, and error indicators are turned off. The READY signal will be held high, automatically holding the contact latch outputs high; updating the latches through software adds extra insurance to the system. The contents of the EPROM will be used to initialize the latches, so the system RAM will not be used until it is tested. Once all the latches are set, the Initialization Block will continue.

When initialization resumes, a memory test will be performed. First, the stack area is tested with a ROM-based routine. Once the stack area is verified as good, the remaining read/write memory can be tested. A "walking ones" test is performed first, and then the values 55H, AAH, 00H and FFH are loaded and read back, in that order. If the test fails, the READY line will be kept high and the MEMORY ALARM and GENERAL ALARM signals will be activated. The program will then go into a loop, continuously testing the memory. (This is a fatal condition; if the memory does not pass the test, one of the memory chips is bad and must be replaced.)

At the end of the memory test, all RAM locations will be initialized to FFH, which is the code for an RST 38 instruction. At the conclusion on the Initialization Block, only the RAM locations that are used will be different, so RST 38 instructions will be executed in case the program counter goes into an unused portion of system RAM.

If the memory test is passed, initialization continues. The memory stack will be initialized, and all allocated

memory locations will be cleared. The output registers will be initialized, and their contents will be used to update the output latches. When this is done, all failure indicators will be off and all contact outputs will be held high. The READY line will remain inactive (high) until sync is established with the hardware.

Next, interrupts are enabled and a HALT instruction will be issued. This will cause the processor to execute NOP instructions until either an interrupt arrives or a reset signal is received from the watchdog timer. The program will not enter this block again during normal program operation.

The RFL 97A RX CPU will then wait for interrupt signals to be received; in transmit/receive terminals, interrupts are produced by the digital transmitter module; in receive-only terminals, they come from the digital receiver module. When an interrupt is received, the program will vector to Location 38H and execute the code found there. This code will force a jump into the Primary Input Data Block.

10.4.3. Primary Input Data Block

During execution of this block, the input contact and status latches are read, accepting new messages from the remote station. It is primarily a hardware interface control block; once enabled by the Initialization Block, it stays enabled until the RFL 9700 is turned off or reset.

The first part of this block is actually the end of the executive loop program (para 10.4.1). The program always returns here to adjust the stack, enable interrupts and issue a HALT instruction. When the interrupt occurs, the program vectors to Location ISTART, where the input status and contact latches will be read. Throughout the executive loop routines, the interrupts will remain disabled; if the program does not follow the correct path to the Primary Input Data Block, the interrupts will never be enabled. If this happens, the watchdog timer will reset the processor, because the input status latch will never be read. (The watchdog timer input is tied to the Output Enable pin of the input status latch; this causes the watchdog timer to be reset every time the latch is read.)

The RFL 9700's SYNC signal is generated by the digital transmitter module in transmit/receive and transmit-only terminals; in receive-only terminals, it is produced by the digital receiver module. It is used to strobe U21, which is the new message flip-flop. Once U21 is strobed, its Q* output (U21-21) will go low, applying an interrupt signal to microprocessor U1. This same latch signal is used as the INTERRUPT signal on the logic CPU module, so the programs on both CPU modules are synchronized.

The INTERRUPT strobe starts the program. The digital receiver module loads the latest data it received into the RFL 97A RX CPU's input latch. These strobe signals are not synchronized, so it is possible that the receiver could update its output latches after the status latch is read but before the contact latch is read. If this happens, the status byte would not correspond to the contact byte; a false trip may result. To prevent this, the data read from the latches is stored in a set of local registers. The bytes are read a second time, and compared to the first readings. If the readings do not match, readings are taken until a matched set of readings of both latches is obtained during a single pass. The code is structured so that the data from these latches is read and stored in just 5 μs.

Back at the transmitting terminal, the transmitted data byte was combined with the number 55H in a series of Exclusive-OR gates to invert alternate bits. This was done to prevent long strings of ones or zeroes from being transmitted; such strings could bias some transmission mediums. Another series of Exclusive-OR gates at the receiving end is used to combine the received data byte with the number 55H to restore it to its original form.

The first instruction executed by this routine after an interrupt occurs is to clear the interrupt latch. This latch must function properly, to prevent erratic system operation. Its status is checked by looking at Bit 7 in the status byte, which should be low at this stage of the program; if it is high, either the latch is defective or false interrupts are occurring. Either situation will result in the microprocessor being reset, and a fatal alarm signal will be issued.

Every time the input status latch is accessed, the watchdog timer is reset in hardware. Any time more than 1.67 ms passes between latch accesses, the watchdog timer will reset the module.

10.4.4. Primary Input Data Processing Block

The Primary Input Data Processing Block interprets the data read by the Primary Input Data Block (para 10.4.3). The program will not enter this block unless a new message has arrived.

a. CRC Bit Check. The CRC bits in the status byte are examined first. If a communications error or a check-

back request is detected, flags will be set in the System Flag Register.

b. Communications Medium Verification. Once the data has been identified, it must be established that the communications medium is intact. This is done at the following points in the program:

1. At program start-up.

2. Any time the RFL 9700 is recovering from an out-of-lock alarm.

3. Any time excessive noise has been detected on the communications channel.

4. Any time an incorrect address is received while the addressing feature is enabled.

If an out-of-lock alarm is received (or if excessive noise is detected on the communications channel), "good" channel status will be lost. It will not be re-established until six consecutive messages are received without a CRC error. While good status is lost, the error subroutine will force the READY line high and the TRANSMISSION FAIL* line low. This will automatically pull all contact outputs high; all data received during the restoration process is considered valid, but no trips will be generated until the channel status returns to good. If a bad CRC message is detected during the restoration period, the restoration process is restarted.

If the RFL 9700's addressing feature has been enabled (S4-7 in the ON position), the TRANSMISSION FAIL* line will be set high (inactive) as soon as the channel status returns to good. However, the READY line will be held high until both good channel status is achieved and a correct address is received. The READY line controls the state of the trip outputs. If an incorrect address is received while the channel status is considered good, the READY line will be set high. The TRANSMISSION FAIL* line will not change state and the channel status will remain good.

c. DIP Switch Reading. During the INIT interval, DIP switches S1 and S2 are read. Their settings are used to determine the security and dependability of each channel. DIP switches S4 and S5 are read every time a new message arrives.

If the FAILURE RESET switch on the transmitter interface module is pressed, all the failure indicators will turn off.

d. Carrier Loss Response. The fiber optic receiver module (Section 13) will produce an alarm signal if it detects a loss of carrier signal; an alarm will also be produced if the fiber optic receiver module is removed from the chassis. This signal will pass across the backplane to the RFL 97A RX CPU module, where it will set the appropriate System Status Register bit low. Since the alarm indicates that the RFL 9700 has gone out of lock, the ERROR subroutine must be called to force the RFL 9700 to re-synchronize. All data received during an out-of-lock alarm is ignored. The output contact latch will be placed in the high-impedance state and the READY line will be pulled high. When the READY line goes high, the OUT OF LOCK alarm indicator will light and a fatal alarm will be activated. In this case, the software acts as a back-up to the much-faster hardware. When the alarm condition is detected by the software, the BAD DATA indicator will light. The channel recovery process will not start until the RFL 9700 re-establishes sync and the alarm is removed.

If a communications error is indicated, the contact data byte received during this message interval is ignored.

e. Checkback and Address Testing. The RFL 9700's addressing feature is controlled by DIP switch S4-7. Its setting will determine which checkback scheme is employed. If the switch is in the ON position, addressing is enabled. If the switch is in the OFF position (or is not installed), addressing is disabled.

DIP switch S4-8 must be set according to the RFL 9700's communications data rate. If the switch is set to the ON position, the checkback code will take the data rate to be 64 Kbps. If the switch is in the OFF position (or not installed), the checkback code will take the data rate to be 56 Kbps.

(1) Non-Addressing Checkback. Checkback tests are initiated on request. A checkback request consists of three messages: two deliberate errors followed by an inverted copy of the data encoded with the second CRC polynomial. Between each message, two (at 56 Kbps) or three (at 64 Kbps) good data messages are received.

If the test request is valid, the input contact data should be the complement of the previously-received contact data; if the input data is inverted, it should equal the previous data. When it does, the input contact data will be inverted back to its true state and passed through the contact algorithm routines as normal data.

If the checkback test is not passed on the first try, it could be an indication that a contact changed state at the same time the test was made. The next contact

data message must be analyzed to determine if the checkback test was failed. Since the data received during the first message interval of the test is ignored, a delay of one message interval will result.

(2) Addressing Messages. With addressing enabled, the RFL 97A RX CPU module can receive three types of non-data (CRC2 encoded) messages:

ADDRESS REQUEST
Equal to 80H.

ADDRESS REPLY
Two six-bit address bytes.

CHECKBACK REQUEST
Equal to 40H followed by two six-bit address bytes.

Between each message, two good data messages are received in 56-Kbps terminals. In 64-Kbps terminals, three good data messages are received.

In order to provide maximum security, all non-data message bytes are translated before transmission. By using a look-up table, they are translated into one of 72 bytes. When these bytes are encoded with the second CRC polynomial, they have up to 11 of 14 bits in common with any byte encoded with the first CRC polynomial. This means that three or more bit errors would be needed to transform one of these bytes into a valid data message. Another lookup table in the RFL 97A RX CPU module translates all bytes received encoded with the second CRC polynomial back to their original value.

The RFL 97A RX CPU module informs the logic CPU module that an address request has been received by raising the ADDR TX line for one message period. It takes no other action.

The control program compares the received address bytes to the address bytes that it reads from S4 and S5. If the addresses match, the checkback request is honored. If outputs are disabled as a result of loss of good channel status, they cannot be re-enabled until a valid Address Reply or Checkback Request is received.

If an incorrect address is received, either in a Checkback Request or an Address Reply message, the RFL 97A RX CPU module immediately blocks its outputs. It does this by raising the READY line but not lowering the TRANSMISSION fail line.

The cause of failure can be determines by reading the lit indicators on the front of the RFL 97A RX CPU module:

BAD DATA And OUT OF LOCK
The RX CPU is waiting to receive six good data messages in a row and an address from the remote station.

OUT OF LOCK
The RX CPU is waiting to receive an address from the remote station.

CHECKBACK FAIL
The CHECKBACK FAIL indicators will light if the received address does not match the address read from the DIP switches. The first six indicators will reflect the difference between the two addresses:

Lit Indicator	Address Bits That Do Not Match
1	Either bits 1 or 7
2	Either bits 2 or 8
3	Either bits 3 or 9
4	Either bits 4 or 10
5	Either bits 5 or 11
6	Either bits 6 or 12
7	Not used
8	Not used.

(3) Checkback Success. When a checkback test is successfully completed, the CHANNEL FAIL indicators will flash in sequence, starting with Channel 0 and ending with Channel 7. Any channel that fails the test will have its indicator remain lit.

The only time that the output data block will actually produce a data output is when a change is required. This will help prevent system noise problems and output data bus errors.

f. Sub-Routines. The following sub-routines are part of the Primary Input Data Processing Block. They can only be accessed from that block, and they return the program to the Primary Input Data Processing Block when they are completed.

(1) Communications Check. The COMCHK subroutine keeps track of communication errors. If three or more bad messages are received in a group of ten, the ERROR subroutine is called. The system will be forced to re-establish a good channel before normal operation can resume.

(2) Chechback Test Conclusion. The PASS2 sub-routine is run if a change of state is detected during a non-addressing checkback test. If any channel changes state during the same period that a checkback test is requested, it would appear to be a checkback error. To verify the change of state, the next data byte must be tested. The results of both tests are compared. If the channel in question still shows the change during the second message period, then a change of state has indeed occurred and the test has been passed. If the data is different for both message intervals, there is a bad channel and the CHECKBACK FAILURE indicators will show which channel failed.

(3) Security/Dependability Algorithm. The ALGOR sub-routine performs logical operations on the newest contact byte and the previously-received contact bytes to determine the contents of the output contact latch. This is done to satisfy the security and dependability requirements that have been programmed for each channel. For example, consider a channel that has been programmed for Very Secure operation; a change of state must be present in at least three of the last four message intervals to be interpreted as a valid change.

(4) Error Sub-Routine. The ERROR sub-routine forces the system to re-establish a good communications channel when an error condition exists. The READY line is forced high, disabling the output contact latch.

10.4.5. Secondary Input Data Block

The Secondary Input Data Block reads DIP switches S1 and S2, and interprets their settings. This information is used to determine the security and dependability ratings of each contact channel.

If the program tried to read all the DIP switch settings and calculate the shadow mask values for all eight channels during each message interval, this operation alone would take longer than the allotted message interval time (267.86 µs for 56-Kbps operation, or 234.38 µs for 64-Kbps operation). To allow these calculations to be made on a timely basis, they are spread over two message intervals, with four channels being processed at a time. The shadow mask values for Channels 0 through 3 are calculated and updated during the first message interval, and the values for Channels 4 through 7 are processed during the second.

Security and dependability status is updated after the RFL 9700 is initialized, and whenever noise disrupts communications. Whenever the program has to restore communications after carrier loss or a period of high bit error rates, six consecutive error-free messages must be received from the remote RFL 9700 before normal operation will continue. (Non-data messages are not counted for this purpose.) The six messages are formed into two modes: a two-message INIT mode (during which all data is ignored), and a four-message RESTORE mode. During the INIT mode, DIP switches S1 and S2 are read and security and dependability are rechecked. During the RESTORE mode, data is accepted and processed through the security/dependability algorithms. The resulting output contact data is then loaded into the output contact latch. Its output lines are not enabled until the end of the RESTORE mode, because it takes up to four message intervals to calculate the algorithm for a Very Secure channel. Since the other algorithms are calculated faster, this guarantees that all calculations will be made before the RFL 97A RX CPU module returns to normal operation.

The DIP switch settings are checked during program execution in case a noise glitch was to change their stored value. If they were only read once during initialization, the RFL 9700 could never recover from the noise glitch. When the Secondary Input Data Block is finished, it always passes control to the Primary Input Data Block (para 10.4.3).

10.4.6. Output Data Block

The Output Data Block handles all of the output operations for the main program. The output data is held in three registers: the Output Contact Register, the Output Status Register, and the Checkback Failure Register. The contents of these registers will only be loaded into the output latches if an update is required; this reduces system noise and reduces the chance of error.

Whenever a checkback test is performed, the CHECKBACK FAIL indicators on the front of the RFL 97A RX CPU module are flashed in sequence, lowest to highest. If a channel passes the checkback test, its indicator will light for about 4/10 of a second, and then go out. If a channel fails the checkback test, its indicator will stay lit.

If the Output Data Block is enabled, the output latches will be updated and the flash routine will be bypassed during that particular message interval. The checkback test is actually done in two parts: first, the Primary Input Data Processing Block checks for "stuck" communications channels, and the the Output Data Block tests the output contact latch. In order to prevent the checkback test from taking too much computing time during any particular message interval, the code has been arranged so that the two parts of the checkback test are never performed during the same message interval.

Because the checkback test routine performed by the TLATCH sub-routine is essentially an I/O routine, it is included within this block. This portion of the test must be performed as quickly as possible, and includes these steps:

1. The contents of the Output Contact Latch are read through the Input Checkback Latch.

2. The data is inverted and loaded back into the Output Contact Latch.

3. The new latch contacts are then read through the Input Checkback Latch.

4. The Output Contact Latch is reloaded with its original contents.

The inverted data will appear at the output of the Output Contact Latch for about 1.75 μs. While the inverted data is on the latch's outputs, it is ignored. Once the original data has been reloaded, the original data and the inverted data are combined in a series of Exclusive-OR gates; they should complement each other.

At the end of the test, the program initializes the Checkback Flash Routine Registers and updates the Output Status Latch. If the checkback test was passed, Bit 1 of the Output Status Latch is pulsed; this is the CHECKBACK OK signal, that is passed over to the transmitter interface module to serve as the clock signal for the CHECKBACK PASSED indicator latch. This allows the programmable logic software to detect the passed checkback test.

If the programmable logic software does not sense a CHECKBACK PASSED strobe within a set amount of time, it assumes that the checkback test has failed. It does this because there are times that the local RFL 9700 signals for a test, but the signal is corrupted and the test is never performed. In this case, there would be neither a passed nor a failed indication.

If the first pass through the TLATCH sub-routine indicates that the Output Contact Latch is not functioning properly, the test is repeated. Since the chances of the latch being defective are rather slim, this provides a degree of assurance that there is an actual failure, and not just a glitch.

If the local RFL 9700 initiates a checkback test and does not receive a checkback request from the remote RFL 9700 within 400 ms, the test has been failed. The local RFL 9700 will wait one second, and then try again. If the remote RFL 9700 does not respond to the second request, the FUNCTION FAIL indicator will light and another checkback test will be initiated 15 seconds later.

The checkback test itself, along with the flash sequence, requires a lot of computing time. In order to fit the entire test sequence into the RFL 9700's message interval, the test and flash sequences are broken up into seven "time-sliced" routines. Each of these routines takes less than 30 μs to run:

TEST1 and TEST2 - These routines perform the actual checkback test on the output contact latch.

CBLATCH - Strobes the Checkback Passed Latch when the checkback test is passed.

IFLASH - Initializes the timer/counters used by the flash sequence routines.

DOFLASH, RELOAD, and CBMODIFY - The actual flash routines.

Table 10-1. Replaceable parts, RFL 97A RX CPU Receiver CPU Module
Assembly No. 101550-3

Circuit Symbol (Figs. 10-4 & 10-5)	Description	Part Number
	CAPACITORS	
C1	Capacitor,electrolytic,47µF,20%,16V,Nichicon ULB1C470M or equiv.	1007 1629
C2-17,19,22-26,31	Capacitor,X7R ceramic,0.01µF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C18,21	Capacitor,ceramic,33pF,5%,100V,AVX SA101A330JAA or equiv.	0125 13305
C19	Capacitor,X7R ceramic,0.1µF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C20	Not used; wire jumper or zero-ohm resistor installed in its place.	
C27,28	Capacitor,X7R ceramic,0.033µF,10%,50V,AVX SA205C333KAA or equiv.	0130 53331
	RESISTORS	
R1	Resistor,metal film,200Ω,1%,1/4W, Type RN1/4	0410 1221
R2	Resistor,metal film,1.21KΩ,1%,1/4W, Type RN1/4	0410 1296
R3	Resistor,metal film,24.3Ω,1%,1/4W,Mepco/Electra 5053YD24R30F or equiv.	1510 2235
R4	Resistor,metal film,100KΩ,1%,1/4W, Type RN1/4	0410 1480
R5,6	Resistor,metal film,499Ω,1%,1/4W, Type RN1/4	0410 1259
R7	Resistor,metal film,143KΩ,1%,1/4W, Type RN1/4	0410 1495
R8	Resistor,metal film,5.62KΩ,1%,1/4W, Type RN1/4	0410 1360
RZ1-6,8	Resistor network,nine 10KΩ 2% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-103 or equiv.	32622
RZ7	Resistor network,ten 221Ω 1% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-221 or equiv.	30165
	SEMICONDUCTORS	
DS1,2	Light-emitting diode array (four),red,right-angle PC mount,Industrial Devices 5640E1 or equiv.	30162
Q1	Transistor,PNP;2N4121	98486
U1	Microprocessor CPU,8-bit,8-MHz,Zilog Z84C0008PEC or equiv.	0640 18
U2	EPROM,8K x 8,UV-erasable,factory-programmed	Contact factory
U3	MOS static RAM,2K x 8,24-pin DIP,Matra-Harris HM3-6116-9 or equiv.	0615 333
U4	MOS octal tri-state bus transceiver,20-pin DIP,Samsung KS74AHCT245N or equiv.	0615 316
U5,6,12	MOS octal tri-state D-type flip-flop,20-pin DIP,Motorola MC74HC574N or equiv.	0615 298
U7-11,23,24	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U13,16	MOS 3-to-8 line decoder/demultiplexer,16-pin DIP,Texas Instruments SN74HCT138N or equiv.	0615 309
U14	MOS hex inverter,14-pin DIP,National Semiconductor MM74HC04N or equiv.	0615 185
U15	MOS quad 2-input OR gate,14-pin DIP,Motorola MC74ACT32N or equiv.	0615 386
U17	MOS 1-of-8 line decoder,16-pin DIP,Motorola MC74ACT138N or equiv.	0615 388
U18	MOS dual D-type flip-flop,14-pin DIP,Motorola MC74ACT74N or equiv.	0615 387

Table 10-1. Replaceable parts, RFL 97A RX CPU Receiver CPU Module - continued.

Circuit Symbol (Figs. 10-4 & 10-5)	Description	Part Number
	SEMICONDUCTORS - continued.	
U19	MOS hex inverter,unbuffered,high-speed,14-pin DIP,RCA CD74HCU04E or equiv.	0615 304
U20	Retriggerable monostable multivibrator,14-pin ceramic DIP,Texas Instruments SN54LS123J or equiv.	0610 147
U21	MOS dual D-type flip-flop w/preset and clear,14-pin DIP,National Semiconductor MM74HC74N or equiv.	0615 166
U22	Microprocessor supervisor,8-pin DIP,Maxim MAX690EPA or equiv.	0635 27
	MISCELLANEOUS COMPONENTS	
L1	Inductor,rf,molded,100µH,10%,Gowanda 10/103 or equiv.	32505 1
S1,2,4,5	Switch array,eight SPST switches,16-pin DIP,Grayhill 90B08S or equiv.	98493
S3	Not used.	
Y1	Crystal,quartz,16.000 MHz	30297
. . .	Shorting bar,single,Molex 90059-0009 or equiv.	98306

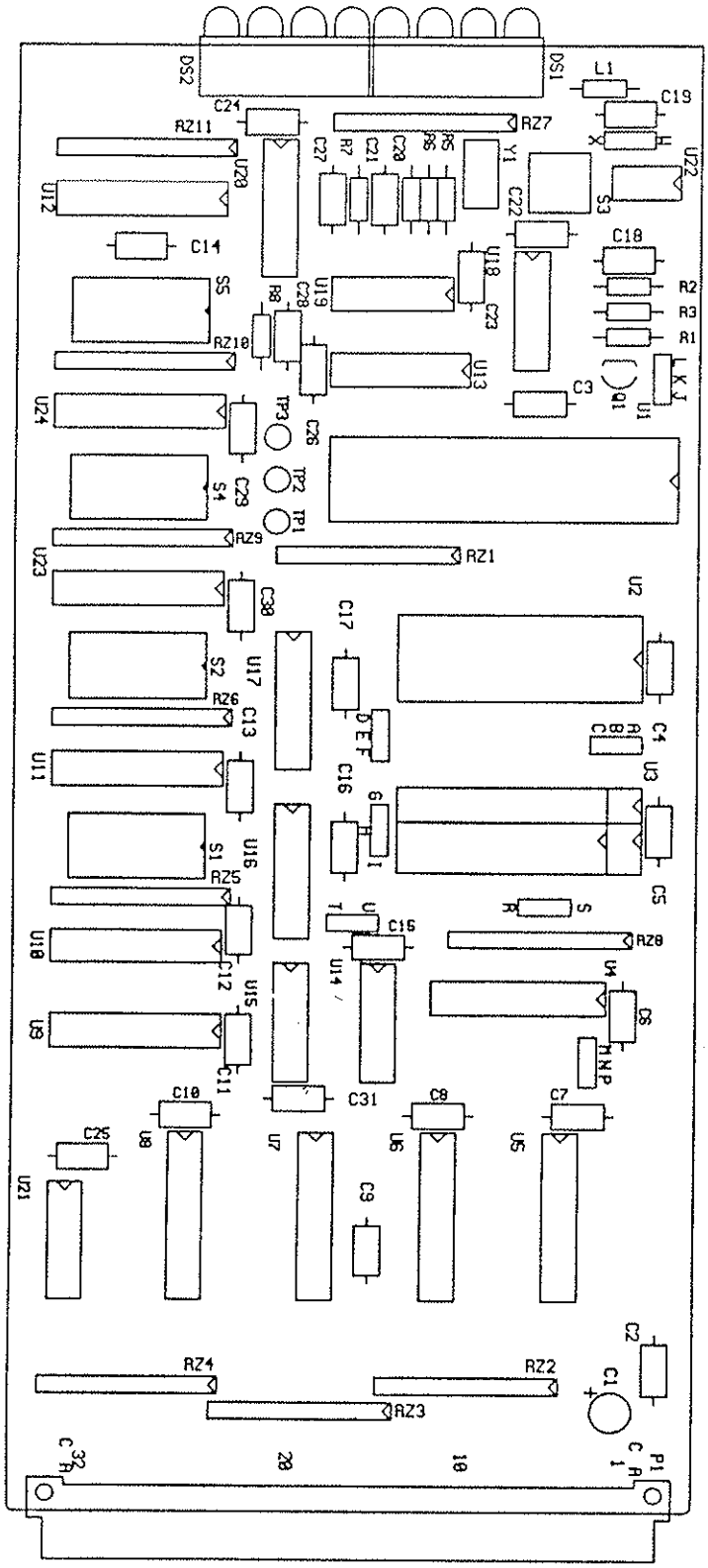


Figure 10-4. Component locator drawing, RFL 97A RX CPU Receiver CPU Module (Assembly No. 101550-3; Drawing No. D-101553-2, Rev. A)

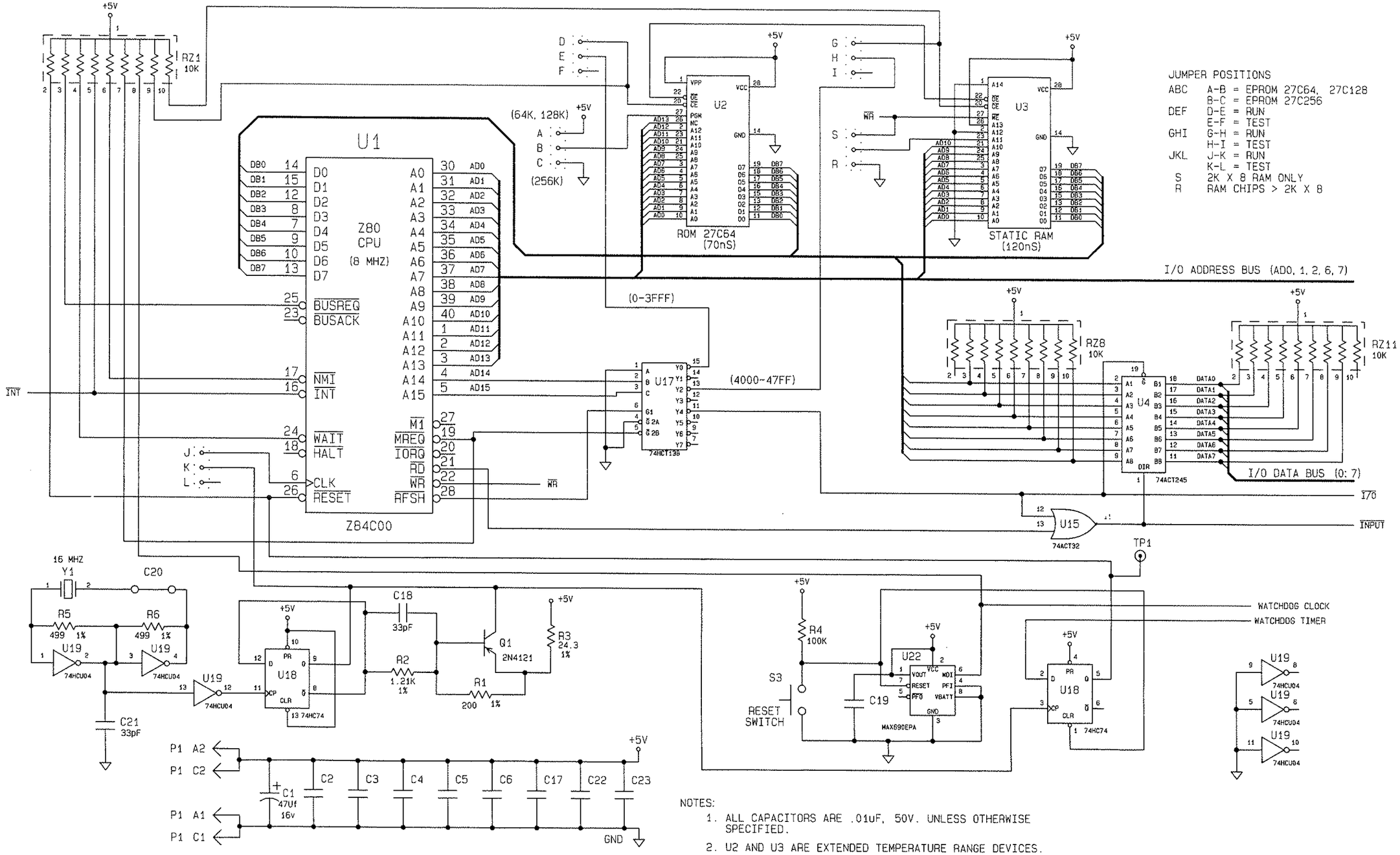


Figure 10-5. Schematic, RFL 97A RX CPU Receiver CPU Module (Assembly No. 101550-3; Drawing No. D-101554-2, Rev. A - Sheet 1 of 3)

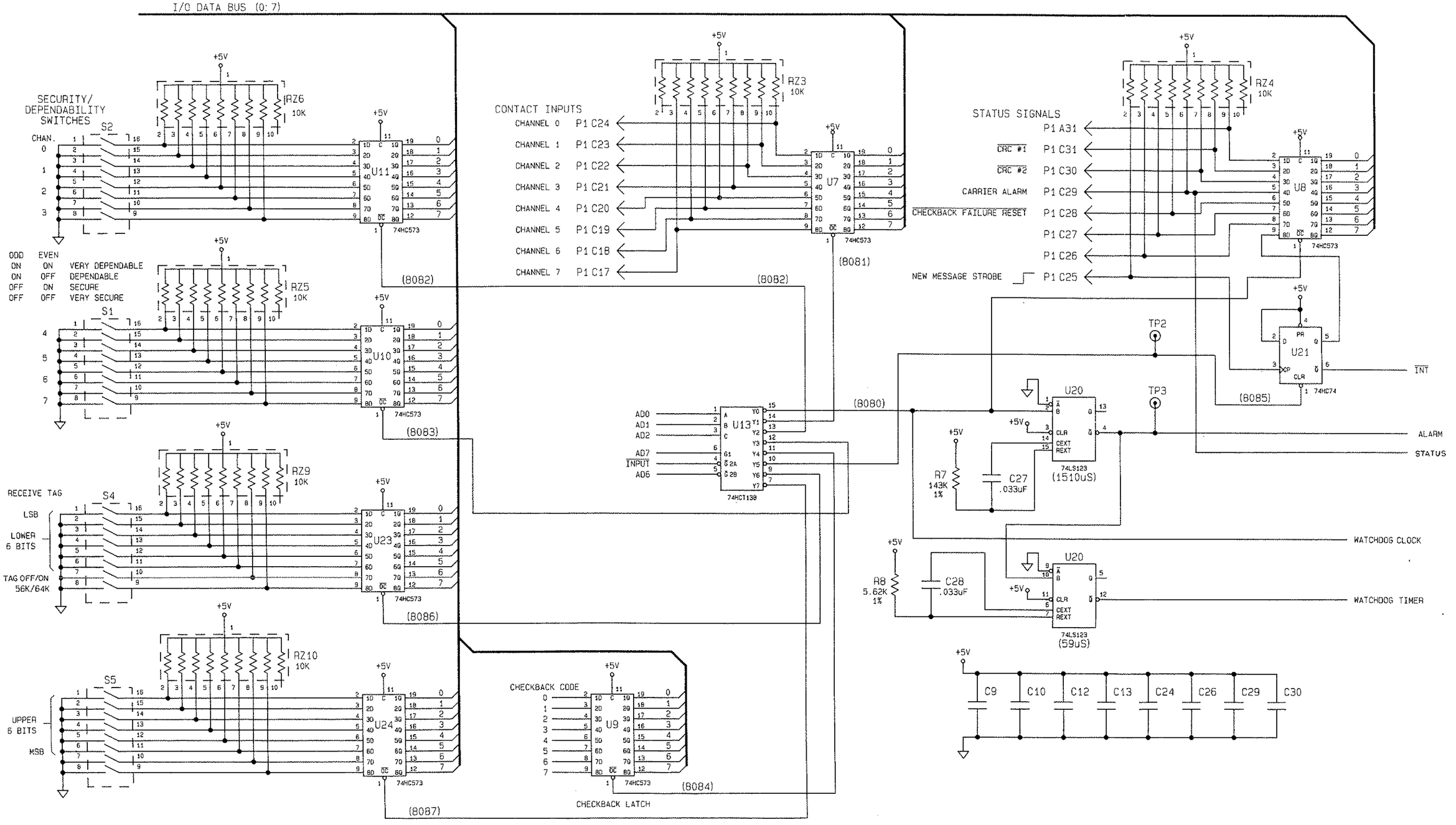


Figure 10-5. Schematic, RFL 97A RX CPU Receiver CPU Module (Assembly No. 101550-3; Drawing No. D-101554-2, Rev. A - Sheet 2 of 3)

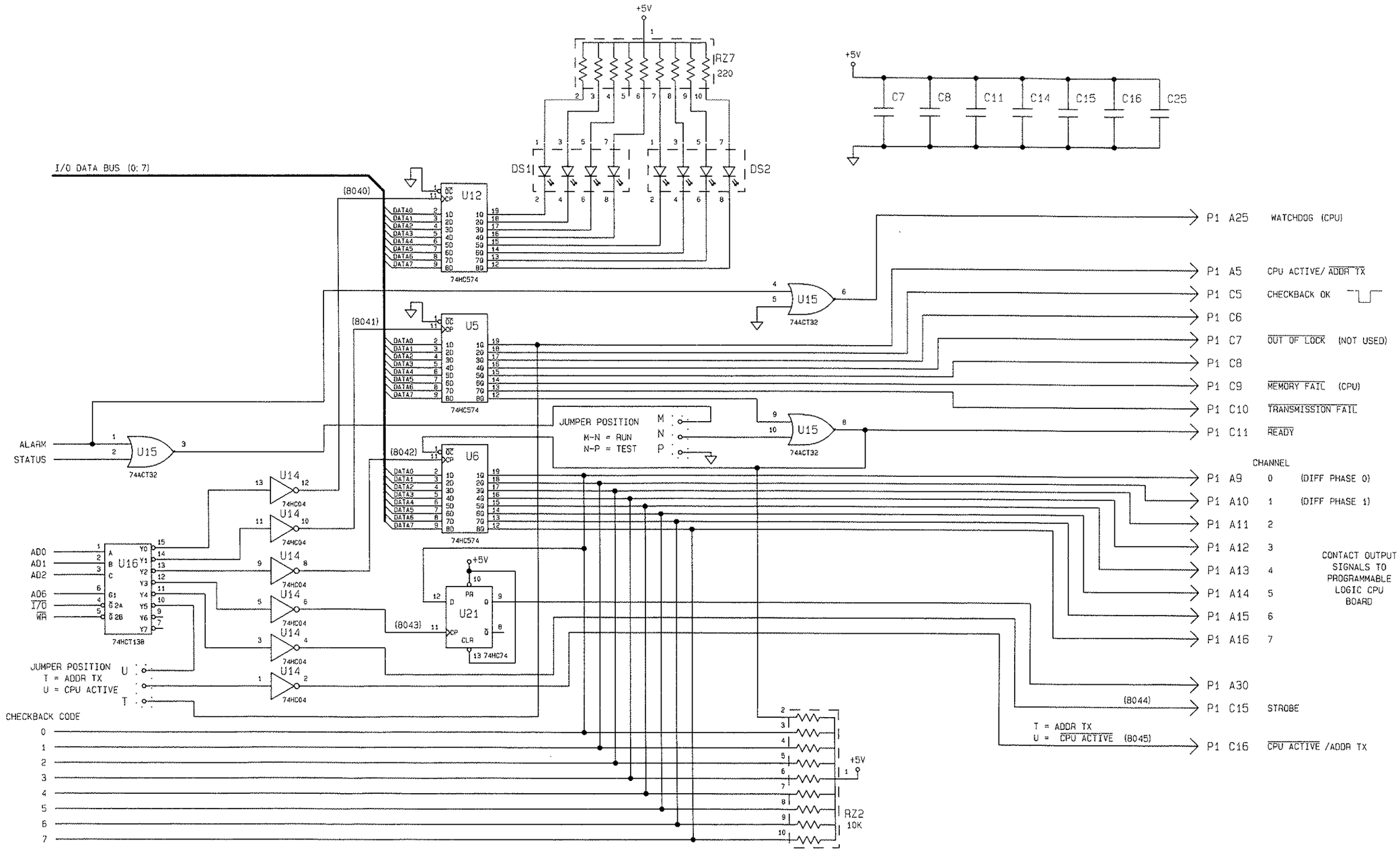


Figure 10-5. Schematic, RFL 97A RX CPU Receiver CPU Module (Assembly No. 101550-3; Drawing No. D-101554-2, Rev. A - Sheet 3 of 3)

Section 11. LOGIC CPU MODULE

11.1. DESCRIPTION

The RFL 97A LOGIC CPU Logic CPU Module (Fig. 11-1) accepts the parallel data from the receiver CPU module (Section 10), and conditions the data as determined by the switch settings on the transmitter interface module (Section 7). The RFL 97A LOGIC CPU module's standard software enables various functions, such as trip hold, command extend, guard-before-trip, and unblocking. Other functions can be accommodated through the use of customized software, developed by RFL for specific applications. The RFL 97A LOGIC CPU occupies one dedicated module space in the RFL 97 CHAS chassis.

11.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to the RFL 97A LOGIC CPU module. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Signal Level: CMOS logic levels (logic high 3.15 Vdc minimum, logic low 0.9 Vdc maximum).

Input Load Resistance: 10,000Ω pull-up to +5-volt supply.

Output Signal Level: CMOS logic levels (logic high 3.15 Vdc minimum, logic low 0.9 Vdc maximum).

Output Load Resistance:
Outputs Driven By 74HC-Type Devices: 10,000Ω pull-up to +5-volt supply.
Outputs Driven By KS74AHCT-Type Devices: 2,000Ω pull-up to +5-volt supply.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements: 4.75 to 5.25 Vdc @ 275 mA; obtained from chassis power supply.

Dimensions:
Panel Height: 5.1 inches (130 mm).
Panel Width: 1.4 inches (36 mm).
Depth (behind panel): 9.1 inches (231 mm).

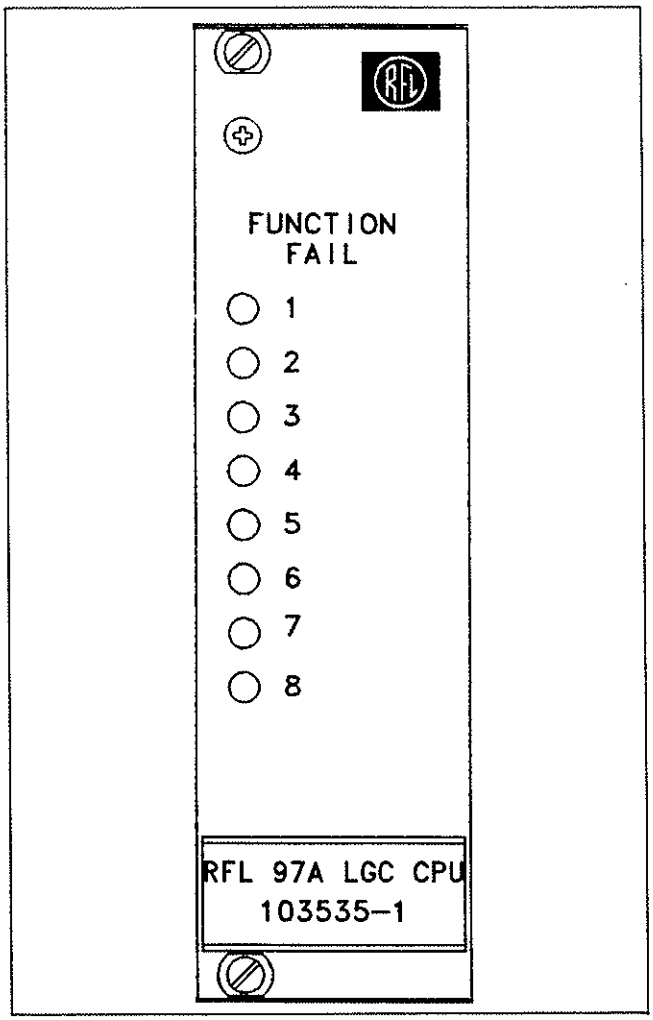


Figure 11-1. RFL 97A LOGIC CPU Logic CPU Module

11.3. HARDWARE DESCRIPTION

The RFL 97A LOGIC CPU is an 8-MHz microcomputer, based on the Z-80 microprocessor. It is designed to handle the RFL 9700's programmable logic function tasks, run diagnostic programs, and send signals to the indicator/output module (Section 12) to update the output relays. Data received from the receiver CPU module is processed through the logic function software and passed to the indicator/output module. System integrity is constantly monitored, and alarms are triggered if faults are detected. Two DIP switches on the RFL 97A LOGIC CPU module configure it for the desired security and dependability levels, addressing, and data rate. A block diagram can be found in Figure 11-2.

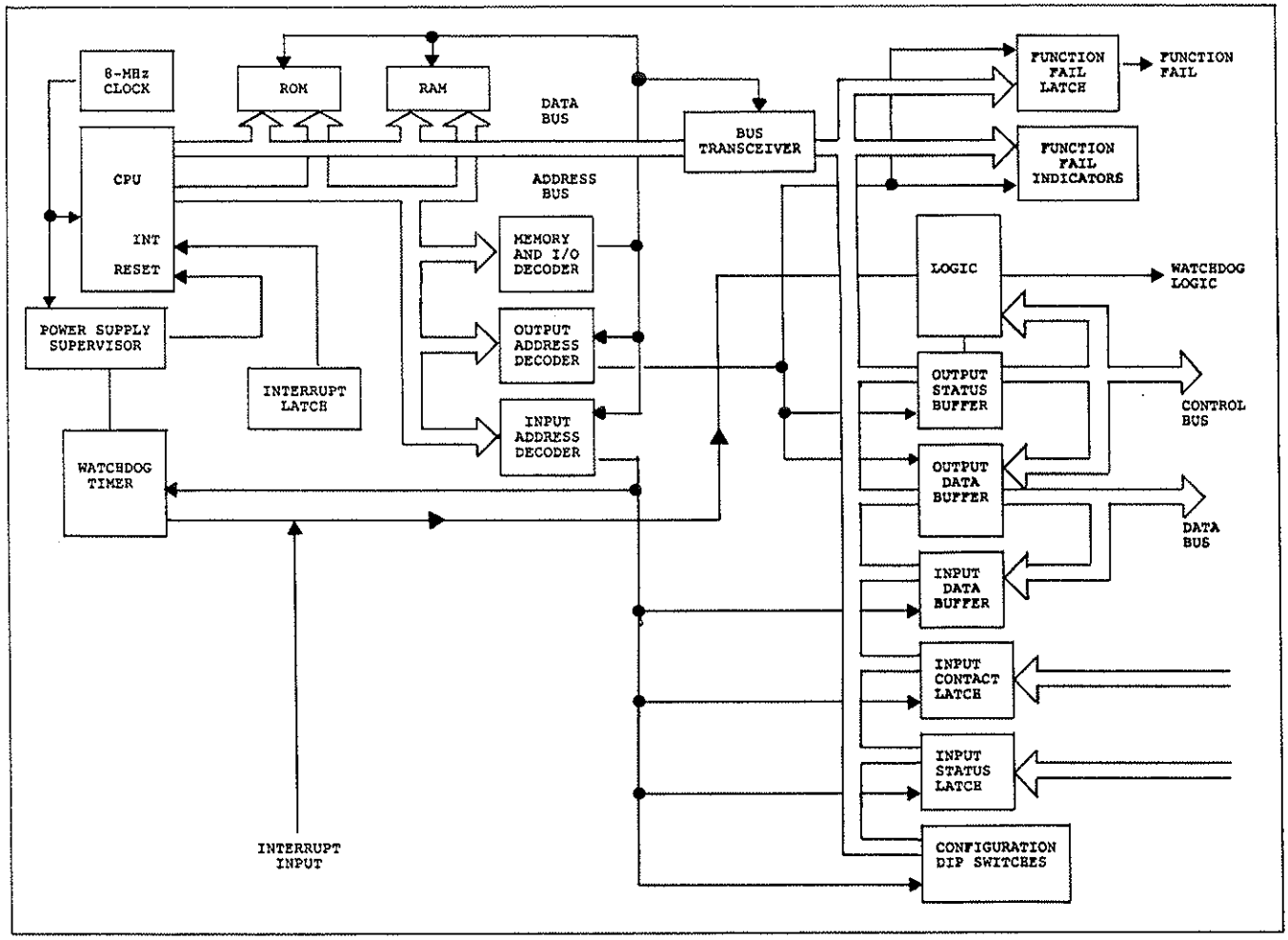


Figure 11-2. Block diagram, RFL 97A LOGIC CPU Logic CPU Module

11.3.1. Program Storage EPROM

The RFL 97A LOGIC CPU's operating program is stored in EPROM U2. Jumper ABC allows several EPROM types to be used for U2; 8K x 8 or 16K x 8 devices can be used when the jumper is in the A-B position, and 32K x 8 devices can be used when it is in the B-C position. The EPROM used must be capable of operating over the specified temperature range for the module (para 11.2). Address decoder U17 is only capable of decoding memory address locations from 0000 through 3FFFH, so the upper 16K of memory in 32K x 8 EPROM's will not be accessible. Jumper DEF must be placed in the D-E position, or this chip will be disabled.

11.3.2. Static RAM

U3 is a CMOS static RAM, used as a "scratchpad" memory to store temporary system parameters as the RFL 97A LOGIC CPU performs its functions. The decoded address range for U3 is 4000H to 47FFH.

Three different device types can be installed for U3: 2K x 8, 8K x 8, or 32K x 8. Two sets of holes are provided on the circuit board to accommodate devices with 0.300-inch or 0.600-inch pin spacings. Jumper RS sets the module for the device type being used; position S for 2K x 8 devices, and position R for the others. The device used must be CMOS, must operate over the module's entire operating temperature range (para 11.2), and must have an address access time of 150 ns or less.

11.3.3. Microprocessor

Z-80 microprocessor U1 is responsible for executing the control program. It features a non-multiplexed address/data bus configuration, with 16 address lines and 8 data lines. U1 requires an 8-MHz clock signal,

which is produced by the oscillator circuit formed from inverter U19, capacitors C21, resistors R5 and R6, and crystal Y1. Resistors R1 through R3 and capacitor C18 form a high-speed, low-loss driver circuit; it is required to provide a fast rise time for the clock while insuring that the signal's high limit is no more than 0.3 volts above V_{CC}, and no more than 0.6 volts below V_{CC}. Jumper JKL determines whether the oscillator circuit's output is used to clock U1 (position J-K), or if an external clock source is used (position K-L). For normal operation, the jumper should be placed in the J-K position.

The RESET signal at U1-26 is supplied by U18-5 (the Q output of D-type flip-flop U18). This active-low signal is produced as a result either a CLEAR signal produced by microprocessor supervisor U22 or a logic low applied to U18-2 by the watchdog timer circuit (para 11.3.8).

11.3.4. Address Decoding

3-line to 8-line decoder/demultiplexer U17 decodes the EPROM and static RAM memory addresses. It also decodes the memory-mapped addresses of the I/O devices, and controls the G1* output enable and DIR direction signals for bus transceiver U4. When the RD* (read) signal on U1-21 goes low and the Y4 output of U17 is selected, the output of OR gate U15 (U15-11) goes low. This sets U4 to allow data to flow from the I/O ports to U1 along the internal data bus. At all other times, data flows from U1 to the I/O ports. The output buffers in U4 will be in the high-impedance state unless an I/O address is decoded and the Y4 output of U17 goes low to enable them.

11.3.5. Input Ports

Octal D-type latches U7, U8, U9, U23, and U24 provide the RFL 97A LOGIC CPU with five input ports. They are all equipped with pull-up resistors, which guarantee a logical one when no driving source is present.

The HAS TRIPPED output signals from the receiver CPU module are loaded into U7. U8 serves as the status input latch, and receives the following signals:

CPU ACTIVE*
The receiver CPU module is present.

DIGITAL RECEIVER ACTIVE*
The digital receiver module is present.

CHECKBACK TEST*
The CBI (checkback initiate) switch on the transmitter interface module has been pressed.

CARRIER ALARM
Received but not used by the RFL 97A LOGIC CPU program.

TEST FUNCTION FAIL RESET*
The FAILURE RESET switch on the transmitter interface module has been pressed.

DIGITAL XMIT ACTIVE*
The digital transmitter module is present.

READY*
Received but not used by the RFL 97A LOGIC CPU program.

U9 is the external data bus input data buffer. It passes all the data on the motherboard's data bus to microprocessor U1.

U23 and U24 interface with DIP switches S4 and S5, which control the addressing configuration and data rate. S4 and S5 are read every time a new message is being sent. (See paragraphs 3.3.4i through 3.3.4k in Section 3 for more information on setting S4 and S5.)

11.3.6. Latches

During normal operation, the digital transmitter module will provide an interrupt pulse at the start of each new message interval. If the RFL 9700 is set up for receive-only operation, the interrupt pulse will be provided by the digital receiver module. In either case, the pulse will clock U21-6 low on its rising edge; this is the Q* output, which provides the interrupt signal for microprocessor U1. At the start of the interrupt routine, U1 will use address decoder U13 to clear the interrupt by addressing output Y5 (port address 8085H). This will result in an active-low CLEAR signal being applied to U21-1, which can be monitored at test point TP2. The pulses at TP2 should be spaced at 268-µs intervals.

Once the interrupt latch is cleared, the processor inputs the status byte from U8 and the TRIP byte from U7. These latches are accessed through U13, which decodes the port address supplied by U1 and then delivers an active low signal to the output enable input of the desired latch (OE*, pin 1).

11.3.7. Microprocessor Supervisor

U22 is a microprocessor supervisor, which provides the power-up reset signal to U18-1, which results in a reset signal being sent to U1-26. A RESET pulse will also be sent to U1 if the 5-volt supply line falls below U1's reset voltage threshold, which is normally 4.5 to 4.75 volts.

A reset will also occur if the internal watchdog timer's input is not strobed at least once every 1.6 seconds. During normal operation, a READ from Address 8080 will reset the timer input well within the 1.6-second interval. This adds a great deal of power brown-out immunity to the system. U22 will hold the RESET signal low for at least 50 ms after the supply voltage returns to a value above the reset voltage threshold.

11.3.8. Watchdog Timer

The OE* signal supplied to latch U8 is also fed to U20-2, which is the positive-going B trigger input of one of the retriggerable multivibrators in U20. These multivibrators serve as the "watchdog timer" for microprocessor U1. Each time U8 is read, the first multivibrator is triggered and its 1500-µs time-out period is restarted. When the RFL 9700 is functioning normally, this multivibrator will be retriggered before it has a chance to time out, so its output will never change state.

If for any reason the input trigger signal is not received, the first multivibrator will time out and the ALARM signal (which can be monitored at test point TP3) will go high. This is a fatal alarm, since the watchdog CPU signal will become active through OR gate U15. At the same time, the second multivibrator in U20 will be triggered (on the rising edge of the ALARM signal, through U20-10). When the second multivibrator is clocked, a 60-µs low-going strobe is applied to U18-2, forcing U18 to reset the microprocessor.

11.3.9. Output Ports

Octal tri-state flip-flops U5, U6, and U12 provide the RFL 97A LOGIC CPU with three output ports, which are controlled by decoder U16. When U16 decodes one of the output ports' address codes, one of its outputs will go low. These lows are inverted by hex inverter U14 to supply a clock signal to the target latch's CLK input (pin 11). U12 is clocked by U16's Y0 output (U16-15), U5 by the Y1 output (U16-14), and U6 by Y2 (U16-13).

U12 provides the drive current necessary to light FUNCTION FAIL indicator arrays DS1 and DS2 on the RFL 97A LOGIC CPU's front panel. Each indicator requires about 11 mA to light; resistor network RZ7 limits the current through the indicators.

The eight output lines of U5 form the source of the eight-bit external control bus on the backplane motherboard. The lowest six outputs (Q0 at U5-19 through Q5 at U5-14) serve as the ADDRESS SELECT and CARD SELECT outputs; they are used to address specific RFL 9700 modules, and specific I/O ports on the addressed module.

The Q6 output (U5-13) serves two functions. When it is low, it serves as the OE* (output enable) signal that allows the addressed module to place data on the external data bus. When it is high, it becomes the STROBE signal that allows the addressed module to latch the data that is on the external data bus.

The Q7 output (U5-12) determines the direction of data flow. Microprocessor U1 will set this bit high when it wants to read data from the external bus, and low when it wants to write data to the bus.

U6 acts as the output data buffer latch for the RFL 97A LOGIC CPU module. All data being written to the other modules in the RFL 9700 is first loaded into U6, where it waits until it is released by the WRITE* signal produced by U5-12. When U5-12 is producing the READ signal, U6 is disabled. This avoids bus contention problems that would result if two active sources were competing for control of the bus at the same time. U6 and input data buffer U9 give the RFL 97A LOGIC CPU module the bi-directional bus capability required to communicate with the other modules in the RFL 9700.

U21-9 provides the FUNCTION FAIL* signal for the indicator/output module. U1 uses this signal to control the FUNCTION FAIL indicator. This signal will become active if the processor detects a failed checkback test, or if it finds that the output contact byte being sent back by the indicator/output module over the test bus does not match the output byte it transmitted to that module. U1 controls this signal by strobing U21B's CLK input, through decoder U16 and inverter U4, after establishing a high/low signal on Bit 0 of the external data bus (U6-19, output Q0).

The CARRIER ALARM signal generated by the fiber optic receiver module (Section 14) has no effect on the RFL 97A LOGIC CPU. This signal is disabled by keeping the MNP jumper in the NP position. This signal cannot be allowed to disable the outputs of U6, because

several programmable logic functions are still active, even after a carrier alarm is detected. The ADDR TX signal set by jumper TU has no effect on the RFL 97A LOGIC CPU. This jumper is placed in position U at the factory.

11.4. SOFTWARE DESCRIPTION

Paragraphs 11.4.1 through 11.4.12 describe the assembly-language control program used on the RFL 97A LOGIC CPU module. An overall logic diagram for the RFL 97A LOGIC CPU module can be found in Figure 11-3.

11.4.1. Program Structure

The RFL 97A LOGIC CPU's operating program is interrupt driven. The description that follows is based on a logic CPU module installed in a typical 56-Kbps synchronous system. A synchronous communications link exists between the local receiver and the remote transmitter.

Each word contains one synchronizing bit, eight data bits, and six CRC bits. Each word takes 267.86 µs to transmit. The local digital receiver module receives the transmission, calculates the CRC, and then strobes a new message into its output latch. Each new message strobe will cause an interrupt on the logic CPU module.

In the descriptions that follow, the time required to transmit one word is referred to as a "message interval." In 56-Kbps systems, a message interval is 267.86 µs long; it is 234.38 µs long in a 64-Kbps system.

11.4.2. The Background Program

The background program executive structure is a ring comprising the following program blocks:

Input/Output Data
Input Data Processing
Guard-Before-Trip
Unblock
Command Extend
Combinational Logic
Permissive Coordinating (optional)
Trip Hold

Not all of the above program blocks will be active at the same time, but their position within the background program loop will not vary. In 56-Kbps systems, the background program loop requires three message intervals (803 µs) to execute; it requires four message intervals (937.5 µs) in 64-Kbps systems.

a. Timers. The background program uses a large number of software timers; there are no hardware timers used on the RFL 97A LOGIC CPU module. Timing is derived from the new message strobes that are generated each time the background program starts (every three message intervals).

The interrupt routines handle the interface between the RFL 9700 and all external equipment. The background program maintains the timers, calculates the function block active flags, and passes this information to the interrupt routines. The interrupt routines use this information to modify the output signals.

b. Initialization. On start-up, the program enters the Initialization Program Block. Once the Initialization Program Block is completed, the program will be synchronized to the new message strobe. Depending on the terminal configuration, the new message strobe will originate on either the digital transmitter module or the digital receiver module. Once synchronized, the program will switch from a polling mode to an interrupt-driven mode. Interrupt Mode 1 will be selected for the processor. The new message latch, which will now serve as the interrupt source, will be reset, interrupts will be enabled, and a HALT instruction issued.

11.4.3. Interrupt Routines

The background program uses three interrupt routines: INTERRUPT Ø, INTERRUPT 1, and INTERRUPT 2. If DIP switch S4-8 is in the ON position, a fourth interrupt routine is added: INTERRUPT 3. If the switch is in the OFF position (or is not installed), the three interrupt routine sequence is used. On 64-Kbps systems this switch must be set to the ON position.

Interrupt Mode 1 has been selected for the processor. When a new message is available, the digital transmitter module will issue the new message strobe. This strobe is used to clock flip-flop U21; its Q* output (U21-6) will go low and cause an interrupt. When the microprocessor detects the interrupt, the program will execute the interrupt routine that is addressed by the schedule register.

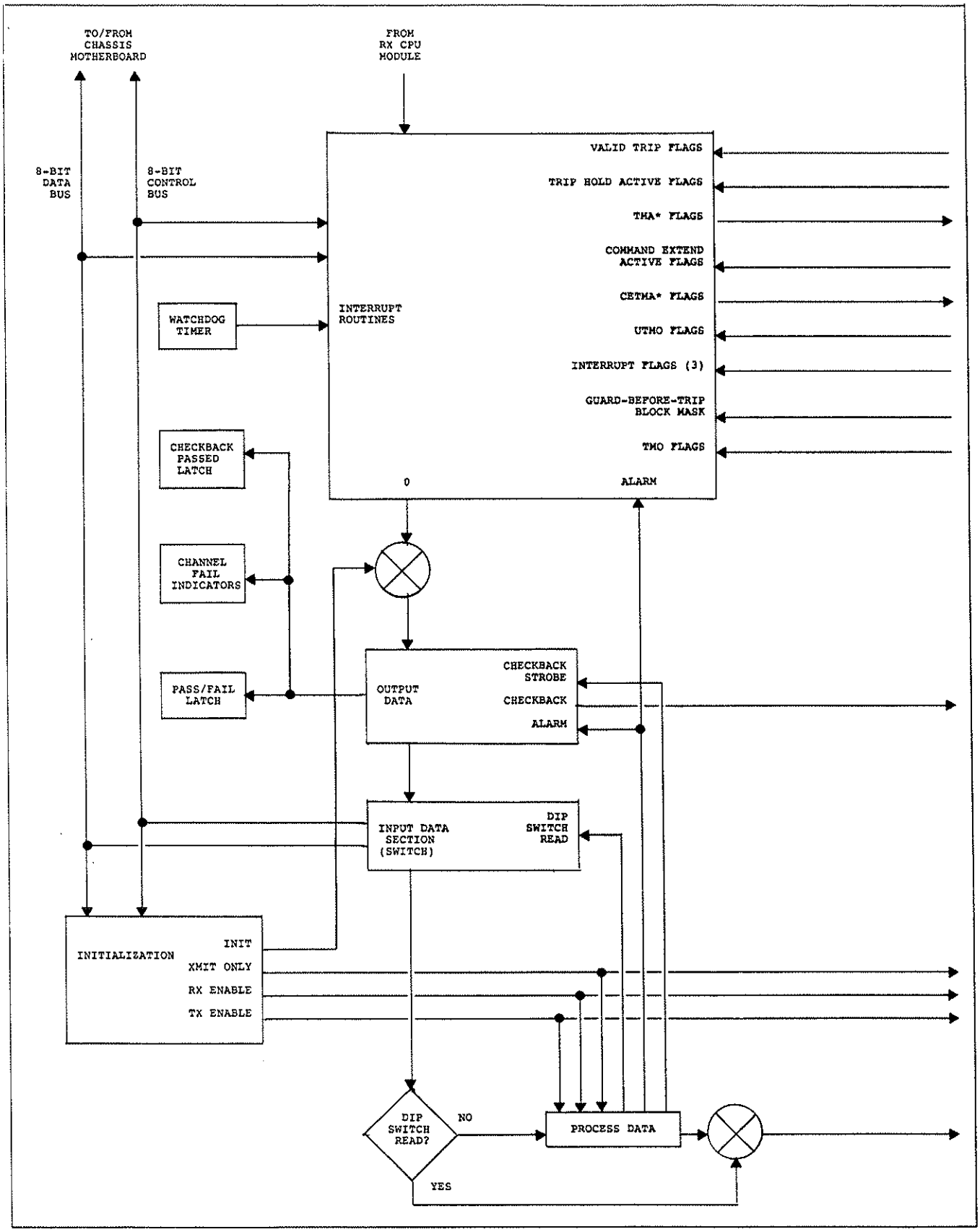


Figure 11-3. Logic diagram, RFL 97A LOGIC CPU Programmable Logic CPU Module (Sheet 1 of 2)

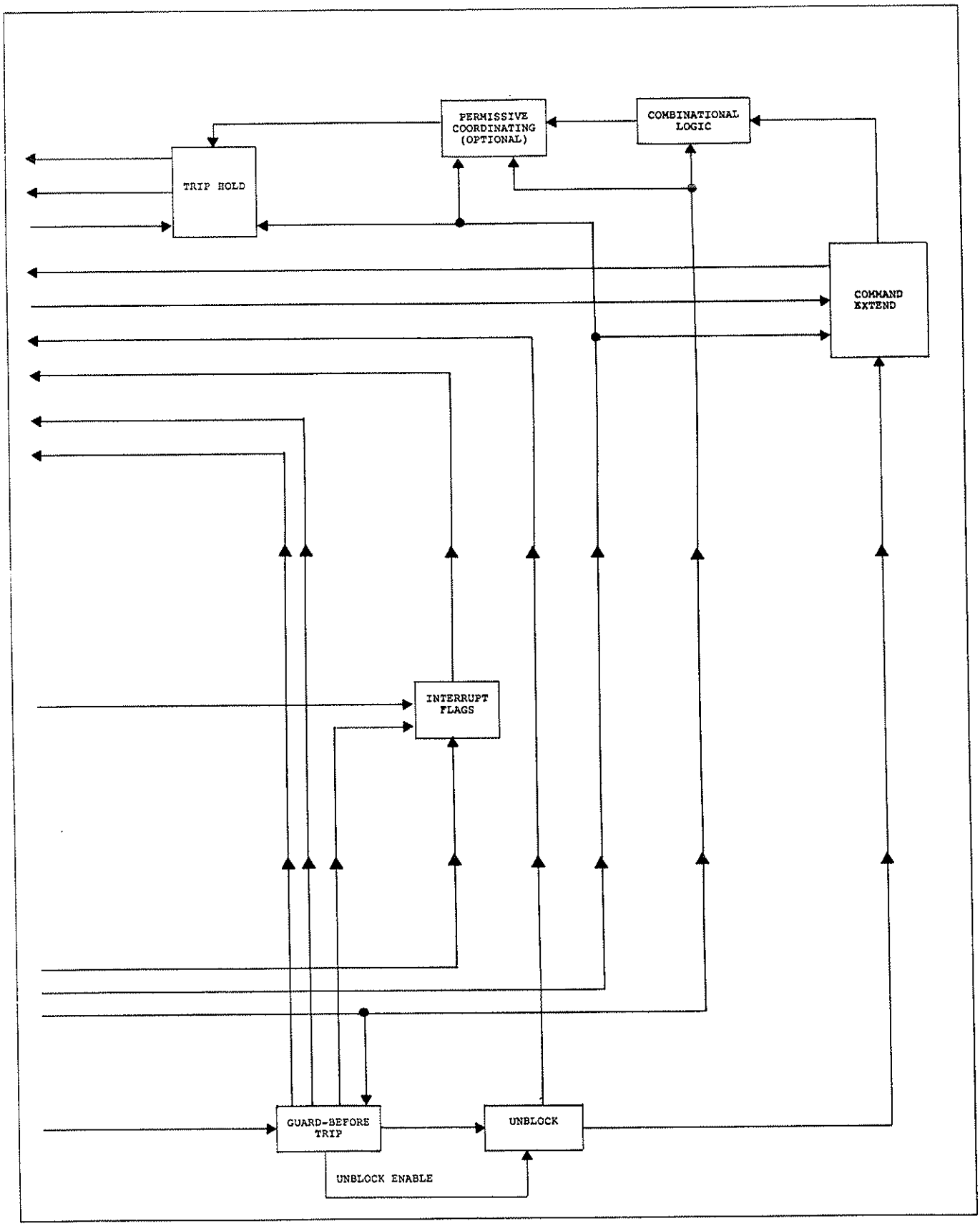


Figure 11-3. Logic diagram, RFL 97A LOGIC CPU Programmable Logic CPU Module (Sheet 2 of 2)

a. INTERRUPT Ø. Upon completion, this routine always returns to the background program at the start of the Input/Output Program Block. The ALARM flag will be set by the Guard-Before-Trip Program Block if one of the process data block routines has detected a fatal alarm condition. If an alarm condition is present, the OUTALARM subroutine is called. This subroutine will disable the output relays in a controlled manner. At the conclusion of this subroutine, the program will jump to the Input/Output Data Program Block. This block will detect that the ALARM flag is set and will loop until the watchdog timer expires, resetting the program.

Each function block in the program has been assigned a flag bit in the program path register. As each function block executes, its flag bit is reset. When the program returns to INTERRUPT Ø, the program path register should read ØØH. If it does, the proper flag pattern is reloaded into the register, the watchdog timer is pulsed, and the routine continues. If any of the flags was not reset, it means that the proper path was not followed; this is a fatal alarm condition. The ALARM flag is set in the background program's FLAGS1 register, and the OUTALARM subroutine initiates an orderly shutdown.

The background program always starts its executive loop at the conclusion of INTERRUPT Ø. The data input during this interrupt routine is used as the reference input data for the background program. Various flag bytes are passed back and forth between INTERRUPT Ø and the background program at the start of the INTERRUPT Ø routine; this is the only time that data is exchanged between foreground and background programs.

If a channel has guard-before-trip and trip hold both enabled, the trip hold function will dominate when a valid trip signal (one that lasts for 4 ms or more) changes to no-trip. The guard-before-trip function will be blocked from seeing the change. If the trip signal was not valid (did not last at least 4 ms), the trip hold function will be blocked from seeing the change and the guard-before-trip function will dominate.

If the guard-before-trip function is active and the signal changes from valid trip to no-trip and back to trip before guard has been established for at least 5 ms, both trip and guard will be lost. This condition will exist until the trip signal is removed and the channel can establish guard for at least 5 milliseconds.

Anytime the RFL 97A LOGIC CPU is powered up or reset, the guard-before-trip function will supersede the trip hold function, because it will prevent a valid trip from being established until guard has been established for 5 ms. This prevents the RFL 9700 from generating a trip as it is turned on.

When the TX INPUT contact byte is read, it cannot be accepted until two consecutive readings match. This is done because the TX INPUT contact input changes are not synchronous with the contact byte readings, and there is a possibility of catching the latch input in a transient state, which is undesirable.

A similar technique is used when the RX INPUT contact byte is read, but for different reasons. First, when the receiver CPU module performs a checkback test, the data input to the RX INPUT contact latch changes for up to 2 µs. Since successive readings of this latch by the RFL 97A LOGIC CPU are spaced much further apart, it is impossible to accept wrong data. Second, we must be sure that the STATUS latch reading corresponds to the contact byte being read. (See below.) The STATUS latch is read along with the contact byte, and then the contact byte reading is compared to the previous one; if two successive contact bytes match, it can be assumed that the STATUS byte is correct.

If the communications channel is lost or bad data is received, Bit 6 of the STATUS byte will be a logic one. This will cause the guard relays on all channels to be de-energized.

When the RXCPU READY line (STATUS byte Bit 6) goes high, the CONTACT OUTPUT latch (U6) is put in the high-impedance state. This will cause the RFL 97A LOGIC CPU to read all NO TRIP's. Normally, every channel would have guard active at this point. Since a problem exists with the communications channel, guard should be turned off. This is done by Bit 6 in the STATUS byte. Because of this, the STATUS byte must correspond to the CONTACT byte.

If the RFL 9700's addressing feature has been enabled (S4-7 in the ON position) and the RFL 97A RX CPU receives an address request it sets the ADDRESS REQUEST line high. This causes STATUS byte Bit 0 to be logic one. A flag will be set directing the INTERRUPT 0 TX CONTACT DATA routine to send an ADDRESS REPLY in place of the normal data.

INTERRUPT Ø is the only interrupt routine that handles checkback and address output requests.

The Guard Output and Trip Output routines are straightforward. The address of the destination latch is loaded into the output control latch. The data is loaded into the output data latch and then strobed

into the destination latch. The strobe line is Bit 6 of the CONTROL LATCH address.

The TX CONTACT DATA routine is quite different:

1. The data is loaded into the HAS TRIPPED latch on the indicator/output module. A light-emitting diode on the front of this module will indicate if a trip has been sent to the remote RFL 9700.

2. The data is passed to an Exclusive-OR gate, where it is combined with the number 55H, resulting in alternate bits being inverted. This is done to avoid the transmission of long strings of ones or zeroes.

3. An inverted copy of the resulting byte is loaded into the ERROR CHECK latch on the digital transmitter module.

4. The non-inverted byte is loaded into the TX OUTPUT contact latch on the digital transmitter module.

Hardware on the digital transmitter module inverts the ERROR CHECK latch contents back to normal and compares them with the TX OUTPUT contact latch outputs. If they match, the contact byte is transmitted; if they don't match, the data byte is still transmitted, but the CRC byte is garbled. This causes the remote receiver to discard the data byte when it is received, while maintaining communications synchronization.

Two different checkback schemes are implemented, depending on whether the addressing feature is enabled by S4-7. If S4-7 is in the ON position, the addressing checkback scheme is used. Otherwise, the non-addressing checkback scheme is used.

(1) Non-addressing Checkback. A checkback request transmission is composed of three bytes transmitted on consecutive executions of the INTERRUPT 0 TX CONTACT DATA routine. The first two transmissions are deliberate errors. These are sent by not inverting the data sent to the ERROR CHECK latch. On the third pass through the INTERRUPT 0 routine, inverted data is transmitted to the remote RFL 9700 and CRC Generating Polynomial #2 is used. This will require the local RFL 9700 to combine the outgoing data with the number 55H in an Exclusive-OR gate to invert alternate bits, and then load a non-inverted copy of the resulting byte into the ERROR CHECK latch. An inverted copy of the byte will be loaded into the TX OUTPUT contact latch.

(2) Addressing Checkback. When it is using this scheme, the RFL 97A LOGIC CPU can send three types of non-data messages:

ADDRESS REQUEST
Equal to 80H.

ADDRESS REPLY
Two six-bit address bytes.

CHECKBACK REQUEST
Equal to 40H followed by two six-bit address bytes.

The two most significant bits of both address bytes are logic zero. The six least significant bits of the first address byte are read from DIP switches S4-1 through S4-6, those of the second from DIP switches S5-1 through S5-6.

In order to provide maximum security, all non-data message bytes are translated before transmission. By using a look-up table, they are translated into one of 72 bytes. When these bytes are encoded with the second CRC polynomial, they have up to 11 of 14 bits in common with any byte encoded with the first CRC polynomial. This means that three or more bit errors would be needed to transform one of these bytes into a valid data message. Another lookup table translates all bytes received encoded with the second CRC polynomial back to their original value.

The ADDRESS REQUEST byte is sent when the receiver CPU module raises the READY line. The OUT OF LOCK indicator on the indicator/output module will light, and the RFL 97A LOGIC CPU will be informed that it is no longer receiving good data. As long as the READY line stays high, the RFL 97A LOGIC CPU will send this byte once every five times the INTERRUPT 0 routine executes (or once every 4 or 5 ms). The receiver CPU module will not lower the READY line until it has received six good data messages and the proper address from the remote RFL 9700.

An ADDRESS REPLY is sent when the receiver CPU module requests one. The two bytes are sent in consecutive executions of the INTERRUPT 0 TX CONTACT DATA routine. Thus they will be separated by three or four message periods.

A CHECKBACK REQUEST is sent upon request of the checkback routines. The three bytes are sent in consecutive executions of the INTERRUPT 0 TX CONTACT DATA routine.

b. INTERRUPT 1 And INTERRUPT 2. These interrupt routines are identical, with one exception. At the start of INTERRUPT 1, the address of INTERRUPT 2 is loaded into the schedule register; in INTERRUPT 2, the address of either INTERRUPT Ø (56-Kbps systems) or INTERRUPT 3 (64-Kbps systems) is loaded into the schedule register.

INTERRUPT 1 and INTERRUPT 2 differ from INTERRUPT Ø in the following ways:

1. CHECKBACK OUTPUT requests are ignored.

2. ALARM status is not checked.

3. Input data is not passed to the background program.

4. Flag data is not passed to the background program.

5. Flag data is not accepted from the background program.

In all other respects, the routines are similar.

11.4.4. Initialization Program Block

The Initialization Program Block disables all RFL 9700 outputs, tests its memory, and then verifies the jumper settings and module complement. If the RFL 9700 passes all the tests in the Initialization Program Block, the outputs will be enabled and the RFL 9700 will be allowed to come on line.

a. Output Latch Initialization. The first action of the Initialization Program Block is to initialize all contact, guard, and transmitter output contact latches to NO TRIP and NO GUARD status. These outputs will remain in this condition until initialization is completed.

b. Memory Test. The memory test routine uses subroutine calls, so the integrity of the stack area must be assured. This area is tested by a routine that does not use any RAM locations. The MEM FAIL (memory failure) indicator is driven by a latch on the indicator/output module. The program always comes on in the fatal alarm condition, and will remain in this condition until initialization is completed. If the memory test fails, the MEM FAIL and CPU FAIL indicators on the indicator/output module will remain lit. The program will repeat the memory test until either the test is passed or the operator intervenes.

During the memory test, a "walking ones" test is performed, where all memory locations are alternated between logic one and logic zero. After this, each memory location is loaded with a byte which is then read. The bytes used are AAH, ØØH, 55H, and FFH.

If the memory passes the test, the MEMORY FAIL flip-flop is preset and all working RAM locations are cleared. The multifunction latch is read, and the receiver and transmitter FUNCTION ENABLE flags are initialized, as controlled by the jumpers on the transmitter interface module.

If the permissive coordinating function is active, the FUNCTION ENABLE flags must indicate that the RFL 9700 is full-duplex (both receiver and transmitter functions enabled). If not, the program will remain in an endless loop until the operator intervenes. This is done to make sure that the operator is aware that the RFL 9700 is not properly set up.

Next, the TEST latch is read to make sure that the two fixed codes (55H and AAH) match what is expected. This indicates that the transmitter interface module is present and that its OUTPUT CONTROL latch, INPUT DATA latch, DATA bus, CONTROL bus, and all interface latches are functioning properly. If any portion of the RFL transmitter interface module is defective, the test will run in an endless loop until the operator intervenes.

c. Module Complement And Jumper Setting Verification. The following tests checks all the jumper settings, and make sure that the required modules are present and properly seated in the chassis.

If receiver functions are enabled by the switches, the digital receiver and receiver CPU modules must be present. Conversely, if transmitter functions are enabled, the digital transmitter module must be present. This establishes a basis for determining if a module is missing or if the jumper settings are correct.

All conditions that can cause a fatal alarm condition in the main executive loop (except for program path errors) are tested during the Initialization Program Block. This will insure that if an error is detected and the program re-initializes, the RFL 9700 will not return to the main loop or reset the alarms until the problem is corrected.

The ALARM flag can be set as a result of only three other conditions:

1. Failure to read the correct codes from the TEST latch.

2. Failure to receive a new message within a given interval.

3. The modules detected as present or not present in the RFL 9700 do not agree with the settings of the FUNCTION ENABLE jumpers.

After the configuration has been verified, all the programmable DIP switches are read, and their settings are used to initialize the FUNCTION BLOCK, CHANNEL ENABLE, and TIMER registers. Two consecutive switch readings that match must be obtained before the data is considered to be valid. After this, the remaining software latches are initialized. The new message strobe is then polled to establish sync with the digital receiver module. If sync is not established, the alarm will be activated and the RFL 9700 will go through the entire initialization process (with the exception of the memory test).

11.4.5. Input/Output Program Block

The Input/Output Program Block does not require an enable flag; it is enabled on every pass through the executive loop. When the RFL 9700 first enters the Input/Output Program Block, it checks for an alarm condition; if one is detected, the program loops until the watchdog timer expires and resets the microprocessor.

The TRIPCK Data Processing Routine compares the contents of the RX OUTPUT contact register with the data read back from the RECEIVER OUTPUT contact latch. If any of the channel bit positions don't match, an indicator on the front of the RFL 97A LOGIC CPU module will light.

The second task performed by the Input/Output Program Block is to update these indicators. Once this is done, the FCTN FAIL function fail indicator on the indicator/output module is updated. This indicator is accessed through the Q output (pin 9) of D-type latch U21. If the TRIPCK Data Processing Routine detected a channel failure or a checkback failure has occurred, the D input to U21 (DATA BUS Bit Ø) is set to zero an strobed into the latch. If no failure is detected, a logic one is strobed into the latch.

When the receiver CPU module passes a checkback test, the output of CHECKBACK PASSED latch U6 on the transmitter interface module is strobed low. The status of this latch is tested by the checkback routines. If the checkback routines have determined that a checkback test is required, INTERRUPT Ø will execute the test.

About every 200 ms, the MULTIFUNCTION, TEST, and TRIP CHECK latches are read; these are the alarm checks. Since these checks are made so frequently, it is impossible for someone to remove a module and change a switch setting without setting off an alarm and re-initializing the program. This makes the switch settings tamper-proof once power is turned on.

The FUNCTION BLOCK ENABLE and PROGRAMMABLE TIME CONSTANT switches are read about once an hour. This is done to help prevent soft memory errors from corrupting the data. Before a new reading can be accepted as valid, it must be read twice in succession; it will take two hours for a new setting to be accepted, unless the processor is reset.

At the conclusion of all READ sequences, the CONTROL latch is left with Bit 7 (READ/WRITE) and Bit 6 (STROBE/OUTPUT ENABLE) high. This will leave all latches with outputs facing the data bus in the high-impedance condition, and eliminate any chance of bus contention when READ or WRITE operation commences.

Communications with other boards in the RFL 9700 takes place over two 8-bit parallel buses: one for data, and one for control. The control bus is organized as follows:

Bit Ø - Address AØ
Bit 1 - Address A1
Bit 2 - Address A2
Bit 3 - Address A3
Bit 4 - CARD SELECT ADDRESS CSØ
Bit 5 - CARD SELECT ADDRESS CS1
Bit 6 - OUTPUT ENABLE (OE*) or STROBE
Bit 7 - READ or WRITE

If Bit 7 is high, a READ operation is indicated. This will automatically put the PLC CARD output buffer latch in the high-impedance condition. Bit 6 must be low for the READ operation to take place; this bit enables the output latch on the selected board to place its data on the data bus. Two bits are used to control read operations to avoid any chance of bus contention problems. During normal operation Bit 6 and Bit 7 are both high (READ mode with output enabled), so the output latches on all modules (including the PLC) will be in the

high-impedance state. At the start of a READ operation, Bit 6 is forced low; it is forced high at the end of the READ operation. If a WRITE operation is to take place, Bit 7 is brought low while Bit 6 remains high. Bit 6 is now used to strobe data into the destination latches after it has been loaded into the output data latch and placed on the data bus.

Bit 7 works in conjunction with the CARD SELECT ADDRESS bits (Bit 4 and Bit 5) to select the module to be read from or written to. Bit 6 controls when the transfer will take place. The ADDRESS bite (Bit Ø through Bit 3) selects the desired location on the selected module.

The eight-bit control bus format allows the logic module to read from four modules and write to four modules. Sixteen different locations can be addressed on each module (except the digital transmitter module; it uses some of the addresses for signal processing).

11.4.6. Input Data Processing Program Block

The Input Data Processing Program Block works closely with the Input/Output Program Block. Basically, a DIP switch is read and then data is processed. These two events will be spread out over up to 19 message intervals, to prevent them from taking up too much time during any given message period.

During the initialization routine, the address of the CPUSTATUS processing routine will be loaded into HL'. After 200 milliseconds, a software timer will time out, and the program will branch to the primary processing routines.

a. Primary Processing Routines. The sixteen primary processing routines are accessed by the Input Data Processing Program Block. Each routine is broken up into time slices, and each time slice takes 30 to 40 µs to execute. One time slice is executed during each pass through the background routine, until all time slices are executed.

The checkback routines will only allow a manual checkback test to start after the CBI switch has been released for at least ten seconds. This prevents an operator from continually initiating checkback tests by holding down the CBI switch.

Local checkback requests are automatically generated once every hour. The remote RFL 9700 also generates checkback requests once an hour, but timers in both RFL 9700's these tests so that a checkback test is performed every 30 minutes. These timers are reset whenever a manual checkback test is initiated.

The RCVRCPU routine insures that the presence or absence of the digital receiver and receiver CPU modules agrees with the setting of the RECEIVER FUNCTIONS ENABLED jumper. If an error is detected during two successive passes through this routine, the ALARM flag is set.

The XMITCPU routine loads the address of the RESET process routine into HL' and insures that the presence or absence of the digital transmitter module agrees with the setting of the TRANSMITTER FUNCTIONS ENABLED jumper. If an error is detected during two successive passes through this routine, the ALARM flag is set.

The RESET routine checks the status of the FAILURE RESET switch. If the FAILURE RESET switch is pressed, the TEST FUNCTION FAILURE flag is reset and number FFH is loaded into the CHANNEL FAIL indicator register. This will cause the FCTN FAIL indicator and all the CHANNEL FAIL indicators to go out.

The TEST55 input data routine loads a code of 55H into the test latch in the transmitter interface module, reads the latch output, and stores the reading in memory. The PROC55 routine will then check to see if the 55H code was read. If an error is detected during two successive passes through this routine, the ALARM flag is set.

The TEST55 input data routine will also load a code of AAH into the test latch in the transmitter interface module, read the latch output, and store the reading in memory. The PROC55 routine will then check to see if the AAH code was read. If an error is detected during two successive passes through this routine, the ALARM flag is set.

The output signals from the output contact latch on the indicator/output module are run through the backplane and connected to the inputs of the TRIP CHECK latch on the transmitter interface module. The TRIP READ routine reads the TRIP CHECK latch, and stores the data in memory. The contents of the receiver output contact register are stored in the CONTACT COMPARE register; these should match the contents of the TRIP CHECK latch. The TRIPCK routine compares the contents of the TRIP CHECK latch to the CONTACT COMPARE register. If an error is detected on two successive passes, the CHANNEL FAIL register is updated to reflect the error. This is not considered a fatal alarm; it is on a par with a checkback failure.

b. Secondary Processing Routines. The data set by the programmable DIP switches will be processed over a time period spanning many message intervals. The exact amount of time it will take will depend on whether permissive coordinating or receiver functions have been enabled. The processing time during any given pass through the background routine has been limited to about 15 μs. This limitation has been placed on the software to increase system operation speed.

The DIP SWITCH READ timer is reset to one hour and enables the Input Data Program Block to read the programmable DIP switches.

The PROC1, PROC2, and PROC3 routines calculate the channel enable bytes for the UNBLOCK, GUARD<TRIP, and TRIP HOLD function blocks when permissive coordinating is disabled.

The PROC4 routine calculates the channel enable bytes for the UNBLOCK, GUARD<TRIP, and TRIP HOLD function blocks when permissive coordinating is enabled.

The PROC5, PROC6, PROC7, and PROC8 routines calculate the time constant for the trip hold programmable timer. A four-position switch is used to program this timer in 50-ms increments. Only four switch settings are allowed: 0001, 0010, 0100, and 1000. If any other settings are detected, a default value of 100 ms will be used.

The PROC9, PROC10, PROC11, PROC12, and PROC13 routines calculate the time constant for the permissive coordinating current reversal timer. The time constant can vary between 5 ms and 50 ms; values less than 5 ms will default to 5 ms, and values greater than 50 ms will default to 25 ms. An eight-position DIP switch is used to program this timer in straight binary fashion.

The PROC14, PROC15, PROC16, PROC17, PROC18, and PROC19 routines calculate the time constant for the permissive coordinating echo timer. The time constant can vary between 30 ms and 300 ms. An eight-position DIP switch is used to program this timer in straight binary fashion; because an eight-position switch using binary code has a maximum value of 255, the range is limited to 30 ms minimum, 285 ms maximum. Since the entire range is programmable, there are no default values.

The PROC20 routine calculates the channel enable byte for the command extend function block.

The PROC21, PROC22, PROC23, PROC24, PROC25, and PROC26 routines calculate the time constant for the command extend timer. The time constant can vary between zero and 100 ms. An eight-position DIP switch is used to program this timer in straight binary fashion; values greater than 100 ms will default to 50 ms.

The PROC27 routine shifts the values calculated by the other routines from their temporary storage buffer to an active buffer. This makes all values active at the same time.

During the READ/COMPARE and process routines, the DIP SWITCH READ timer is bypassed. The PROC28 routine updates the DIP SWITCH READ timer with the number of missing counts.

11.4.7. Guard-Before-Trip Program Block

When a channel has guard-before-trip enabled, guard must be established for at least 5 ms before a trip will be allowed. The Guard-Before-Trip Program Block makes sure that this requirement has been met.

If trip returns before the guard-before-trip timer expires, the guard-before-trip timer will be reset to 5 ms and the trip signal will be blocked from the RX INPUT contact register. The Trip Hold Program Block will never see the trip, and if a trip to no-trip change should occur, it won't see that either.

First, the alarm condition is checked. If the data processing routines have detected an alarm condition, an orderly output turn-off will be executed.

If receiver functions are not enabled, the RFL 9700 is unidirectional (transmit only). The UNBLOCK function is disabled and control is passed to the Unblock Program Block (para 11.4.8).

If receiver functions are enabled, the program directs the RFL 97A LOGIC CPU module to check for a "good" channel, based on the status of the CPU READY line. If the communications channel has been disrupted, the registers used by this function block must be re-initialized so they are ready as soon as communications are re-established.

If the communications channel is good, the GOOD CHANNEL flag is set. This will signal the unblock function block that communications have been established since the last time the unblock function block was entered. The unblock function becomes active when good communications are lost; the GOOD CHANNEL flag will be monitored by the unblock function, and it will terminate when it detects that good communications have been re-established with the transmitter.

At the completion of the Guard-Before-Trip Program Block, the RX INPUT contact register will indicate a trip for each channel that has received a trip signal from the receiver CPU module after a valid guard has been established for at least 5 ms. (This condition only applies if the guard-before-trip function was enabled.)

11.4.8. Unblock Program Block

The Unblock Program Block generates a 150-ms unblock trip on all enabled channels if a communications failure lasting more than 20 ms is detected. The unblock function is enabled by the Guard-Before-Trip Program Block, and the following conditions must be met before it can be enabled:

1. Receiver functions must be enabled (required to execute the Guard-Before-Trip Program Block).

2. A good channel must have been established and then lost. (The GOOD CHANNEL flag must have been set).

3. The READY line output from the receiver CPU module must be high; this means that the receiver CPU module has failed, a good channel has not been established, or the communications channel has failed. Once enabled, this block will remain in effect as long as communications are down, or until the 150-ms trip period expires, whichever happens first.

4. If the guard-before-trip and unblock functions are both enabled on a channel, that channel will default to the guard-before-trip function. The unblock function for that channel will be disabled.

5. If the trip hold and unblock functions are both enabled on a channel, they will cancel each other out; both functions will become disabled.

6. The unblock function can only be active on Channels 4, 5, 6, and 7; it cannot be enabled on Channels Ø, 1, 2, or 3.

The unblock function will be disabled for 200 ms after it completes executing, so another execution cannot be performed for at least 200 ms.

Once the program established that the unblock function is enabled, it will check the status of the GOOD CHANNEL flag. If this flag is set, the communications channel was restored sometime since the last pass through the background program. If this is the case, the unblock function will be terminated and control is passed to the Command Extend Program Block.

Any time the unblock routine terminates (either because the 150-ms trip time expires or because communications has been re-established), the program will leave by way of the exit routine. The Unblock Program Block cannot be re-enabled until a good channel is re-established, another communications failure is detected, and the 200-ms interval timer has timed out.

The unblock function can have no effect on guard; guard is defined as a good channel with no trip. The only time that the unblock function is active is when the channel is not good. Therefore, as far as the unblock function is concerned, the system is never in guard.

11.4.9. Command Extend Program Block

The Command Extend Program Block has the ability to prolong a trip signal for a programmable interval of time - anywhere from zero to 100 ms. Command extend is enabled or disabled for each individual channel, and the same programmed interval applies to all enabled channels. An eight-position DIP switch on the transmitter interface module is used to program the timer, using true binary code. If a code greater that 100 ms is programmed, the time constant will default to 50 ms. The command extend function becomes active when a trip signal terminates, and remains active until the command extend timer expires.

This function remains active any time a failure is indicated on the receiver CPU module. Any trip state changes that occur while the command extend timer is active are ignored.

Once all the channels have been tested, the COMMAND EXTEND ACTIVE flags must be stored in memory. If the permissive coordinating function is active, the bit positions for Channels 2 through 7 will never have their COMMAND EXTEND ACTIVE flags set.

11.4.10. Combinational Logic Program Block

The combinational logic program block will remain active in the event of a failure indicated on the receiver CPU module. This function and all other transmitter functions are completely independent of the receiver CPU module, so that the program blocks are useful in unidirectional RFL 9700.

In the standard RFL 97A LOGIC CPU software, this function is not used; the only action taken is to reset the flag in the program path register to indicate that the program accessed this program block. This program block will only be used by customized software developed for specific applications. The contents of the TX INPUT contact register can be altered by this program block, according to the requirements of the specific application. The exact location of this program block in the main executive loop is also dependent upon the specific application that uses it.

11.4.11. Trip Hold Program Block

The trip hold function extends the trip signals in all enabled channels by a programmable amount. Valid trip signals (those lasting at least 4 ms) can be extended by up to 200 ms. A four-position DIP switch on the transmitter interface module sets the programming code. Only four codes are recognized as valid:

ØØØ1 = 50-ms extension
ØØ1Ø = 100-ms extension
Ø1ØØ = 150-ms extension
1ØØØ = 200-ms extension

If any other code is detected, the time constant defaults to a 100-ms extension. If a channel has both the unblock and trip hold functions enabled, they will cancel each other out (both functions will become disabled). If the permissive coordinating function is active, trip hold can only be used on Channels 1 and 2.

The final step in the Trip Hold Program Block is to reset the TRIP HOLD FUNCTION BLOCK flag in the program path register. This is done at the end of program to assure that the program has followed the correct path to completion and that the the entire program has executed.

The program will then enter an endless WAIT loop, where it will remain until the next interrupt occurs; this will be INTERRUPT Ø. When INTERRUPT Ø is completed, the program will return to the beginning of the background program (at the start of the Input/Output Program Block (para 11.4.5). If an interrupt does not occur, the watchdog timer will expire and reset the processor.

11.4.12. Permissive Coordinating Software Option

The permissive coordinating software option allows the RFL 9700 to be used in a permissive coordinating scheme. The program emulates in software the timers and logic gates normally associated with analog-type permissive coordinating controllers, such as the RFL 67 PER COOR. The required permissive coordinating signals are simultaneously generated for two independent channels. The block diagram of a typical permissive coordinating scheme is shown in Figure 11-4.

a. Permissive Coordinating Principles. The permissive coordinating function comprises two semi-independent parts: receiver functions and transmitter functions. The current reversal input signal is used in both algorithms. The RX TRIP signal affects the transmitter echo keying function. The functions can be broken down even further as the program is molded to fit within the interrupt-driven framework of the RFL 9700's programmable logic.

The channel signal assignments for permissive coordinating are shown in Table 11-1.

Table 11-1. Permissive coordinating signal assignments

Signal Name	Receiver Channel	Transmitter Channel
CH1 RX TRIP	5 (INPUT)	. . .
CH1 CURRENT REVERSAL	. . .	5 (INPUT)
CH1 ECHO	. . .	6 (INPUT)
CH1 RECEIVED TRIP *	5 & 6 (OUTPUT)	. . .
CH1 KEY TX TO TRIP	. . .	5 (OUTPUT)
CH2 RX TRIP	7 (INPUT)	. . .
CH2 CURRENT REVERSAL	. . .	7 (INPUT)
CH2 ECHO		8 (INPUT)
CH2 RECEIVED TRIP *	7 & 8 (OUTPUT)	. . .
CH2 KEY TX TO TRIP	. . .	7 (OUTPUT)

* The received trip output modules for Channels 5 and 6 are driven by the same input signal, and both supply the RECEIVED TRIP output of the first permissive channel. The received trip output modules for Channels 7 and 8 are also driven by the same signal and supply the RECEIVED TRIP output of the second permissive channel.

b. Receiver Functions. In standard analog permissive coordinating controllers such as the RFL 67 PER COOR, a true analog RX GUARD signal is used to trigger the guard clear timer. The RX TRIP signal is used as the input to the trip hold timer module, while an inverted RX TRIP signal is used to trigger the guard clear timer module. This setup will be satisfactory for most instances, but a problem may result if the communications link between the local and remote RFL 9700's is broken. If this happens, both trip and guard would be lost; the guard clear timer would not be reset, and the trip hold flip-flop would remain set.

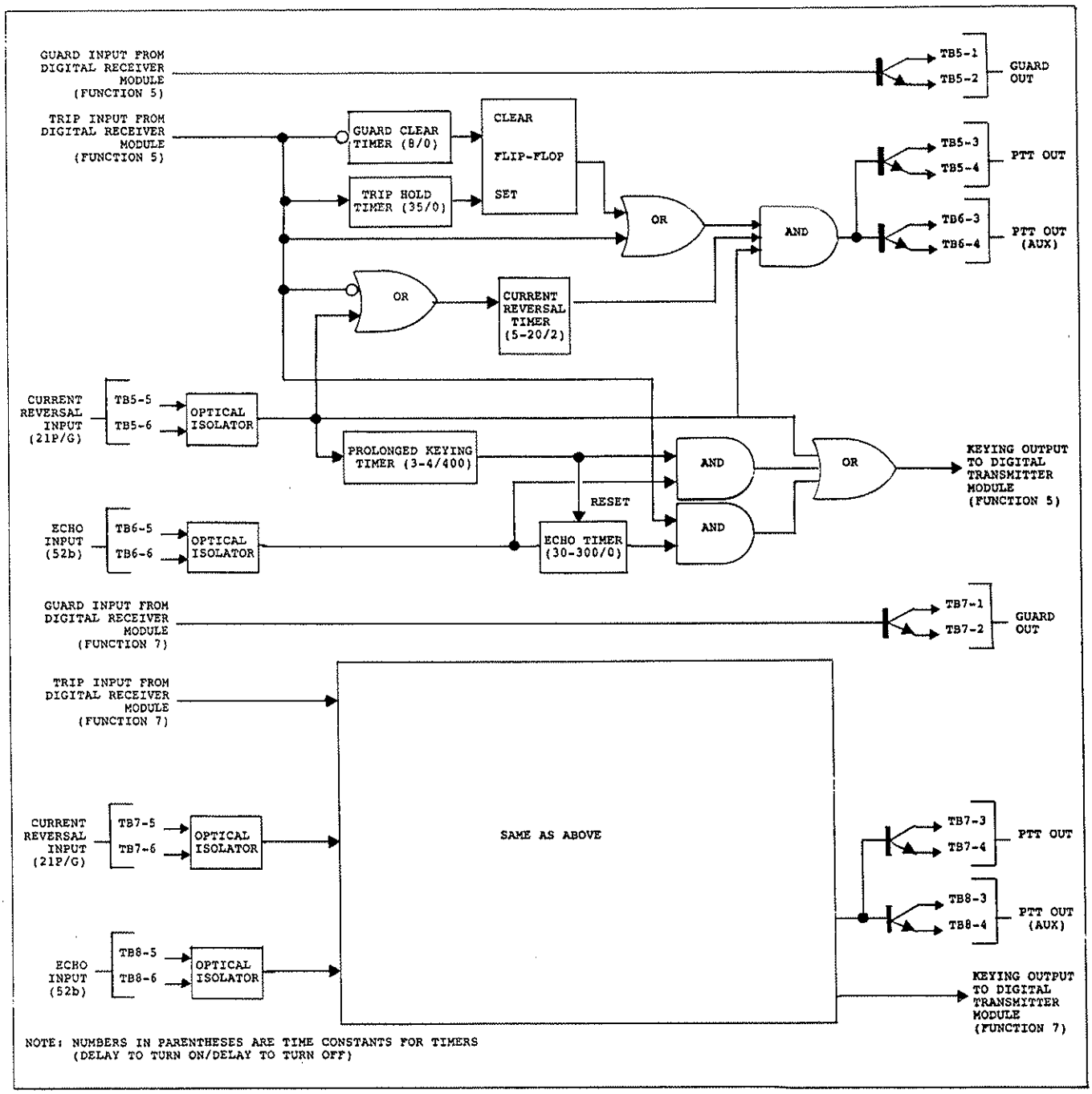


Figure 11-4. Block diagram, permissive coordinating software option

Should a current reversal trip signal be detected at the local RFL 9700 at some later time, a trip would occur, but the trip would be without the benefit of a permissive signal because the communications link is down.

When the inverted RX TRIP signal is used to trigger the guard clear timer, the trip hold flip-flop can only remain set for 8 ms after the RX TRIP signal is lost. At that point, the trip hold flip-flop would be reset by the guard clear timer and the received trip AND gate would be disabled.

When an RX TRIP signal is received, the trip hold timer is triggered. If the trip lasts longer than 35 ms, the trip hold timer will turn on, setting the trip hold flip-flop. The flip-flop can only be reset if the guard clear timer is triggered and allowed to time out for 8 ms. This implies that the RX TRIP signal must be lost for at least 8 ms before the RECEIVED TRIP output signal can be

lost. This will prevent glitches in the RX TRIP signal from appearing at the RECEIVED TRIP output.

The inverted RX TRIP signal is combined with the current reversal input signal (21 P/G) in an OR gate to form the input signal for the current reversal timer. The output of the current reversal timer must be on to enable the RECEIVED TRIP AND gate. The 21 P/G signal also serves as the third input to the RECEIVED TRIP enabling AND gate. The calculated output of the RECEIVED TRIP enabling AND gate is signal #8, which is passed to the interrupt routines at the start of INTERRUPT Ø. The I/O data read during the INTERRUPT Ø routine is passed to the background functions to be used as reference data for the timer routines. This is the same procedure used in the standard RFL 9700 program.

The interrupt routines have been modified to run through the logic necessary to combine signal #8 with the receiver contact mask to form the final output trip signal byte. This contact byte will contain the output of the direct transfer trip functions for Channels 1 and 2, as well as the permissive coordinating RECEIVED TRIP output signals on Channels 5 through 8. Also, due to amount of time it takes to execute the permissive coordinating routine, the background program must be executed over a four-interrupt interval (1.07 ms). This differs from the standard RFL 9700 program, where the background program operates over a three-interrupt interval (802 μs).

The trip delay for a permissive coordinating channel operating in the Very Dependable mode ranges from 3.76 to 5.7 ms, while the echo (round-trip) delay will range from 5.8 to 8.0 ms.

The permissive coordinating option has no effect on the standard software functions found on the receiver CPU module. The security and dependability programming functions found on this module still apply.

c. Transmitter Functions. Forward-looking current sensing relays at the local RFL 9700 provide the current reversal input signal. When these relays detect a fault, a permissive trip signal (KEY TX TO TRIP) is immediately transmitted to the remote RFL 9700. The transmitter portion of the permissive coordinating program has two main parts: the echo timer module and the prolonged keying timer modules.

The echo timer module is driven by the reverse-looking local relays, as long as they don't see a fault behind the local RFL 9700. If the remote RFL 9700 tries to energize its breaker when an internal fault exists, the echo signal will enable the local RFL 9700 to "echo" back the trip signal being received from the local RFL 9700; this will allow the remote breaker to trip. The echo timer sets a programmable pick-up delay before the echo signal can become established; this prevents faults on adjacent lines from causing false trips.

The prolonged keying timer insures that a trip signal will be provided for 400 ms to a slow or stuck remote breaker after the local breaker has tripped. It holds the echo timer in reset as long as the prolonged keying signal exists; this is necessary to prevent a permissive trip signal from being continuously transmitted by both RFL 9700's. This is referred to as "echo lock-up.

d. Timers. The permissive coordinating program has five timers, which control its operation. The current reversal, guard clear, and trip hold timers are used to control the receiver functions; the prolonged keying and echo timers are associated with the transmitting functions.

(1) Current Reversal Timer. The current reversal timer protects against false trips that occur because of sequential clearing of faults in adjacent lines. If a fault does occur on a adjacent line and the fault is picked up by the forward-looking relays at the remote RFL 9700 on the healthy line, the remote RFL 9700 will send a permissive trip signal to the local RFL 9700. When the fault is cleared, the current may reverse direction on the healthy line for a short time, because of sequential clearing of the faulted line. The current reversal relays at the local RFL 9700 will detect this and mistake it for a local fault. If the remote RFL 9700 is still sending a permissive trip signal, a false trip will occur.

The current reversal timer protects against this by preventing the current reversal signal from enabling the RECEIVED TRIP AND gate for a programmable delay interval. This will block the RECEIVED TRIP output signal until the remote RFL 9700 has had a chance to cancel the permissive trip signal. The timer features a pick-up delay which can be programmed to any value from 5 to 50 ms, and a fixed drop-out delay of 20 ms.

In a normal pre-fault situation, the output of the current reversal timer will be on, because there is no RX TRIP signal. Variations in protective relay pick-up times may cause the RX TRIP signal to appear before the local protective relay operates. The local protective relay supplies the current reversal signal; as long as the time delay between the arrival of the RX TRIP signal and the current reversal signal is less than the current reversal timer's drop-out delay, the timer output will not turn off. The RECEIVED TRIP output signal will immediately respond. If the delay exceeds the timer's drop-out

time, the output signal cannot respond until the current reversal timer times out. This will cause a delay of 5 to 50 ms, depending on how the timer was programmed.

The "rest" state of the timer output is directly dependent on the input state. If the timer input signal reverses prior to timeout, the timer will reverse with the opposite time constant and retrace its steps.

(2) Trip Hold Timer. The trip hold timer is activated by the RX TRIP signal. When the RX TRIP signal is received, it will start timing; its output will turn on 35 ms later. The timer output will immediately turn off when the RX TRIP turns off again.

The trip hold timer works together with the trip hold flip-flop to prevent momentary RX TRIP loss, which may result from channel noise that usually accompanies the opening of a circuit breaker. If an internal fault occurs, the remote RFL 9700 will transmit a permissive trip signal to the local RFL 9700. When the remote breaker opens, enough noise can be generated to disrupt communications between the two terminals. When the local RFL 9700 receives the RX TRIP signal, its trip hold timer will be started. 35 ms later, the timer's output turns on and sets the trip hold flip-flop, latching the RX TRIP signal.

The trip hold flip-flop can only be reset if the RX TRIP signal is lost for period of about 8 ms; on/off chatter in the received trip signal that lasts for shorter intervals will be ignored. If the RX TRIP signal is lost, the trip hold timer is immediately reset; the trip hold flip-flop can only be reset by the guard clear timer output turning on.

The 35-ms turn-on delay was established as a compromise between the amount of time required to trip a breaker (about 40 ms) and the highest degree of security possible against false trips. If breaker noise appears on the communication lines before the trip hold flip-flop is latched, the RX TRIP signal may not get latched at all. On the other hand, a longer delay time would require a trip signal to last longer before it is considered valid. This equates directly to security and dependability.

(3) Guard Clear Timer. The guard clear timer is activated by the falling edge of the RX TRIP signal. After an 8-ms pick-up delay, its output will turn on. This causes the trip hold flip-flop to reset if it has already been set, or to ignore any set commands it may receive from the trip hold timer until the guard clear timer is reset.

If the trip signal "bounces" but does not stay off for at least 8 ms, the guard clear timer will not time out and its output will remain off. This will allow the trip hold flip-flop to remain set, and the RECEIVED TRIP output will remain on with no bounce.

The guard clear timer is triggered by the loss of trip, rather than the establishment of guard used for triggering in analog permissive coordinating controllers such as the RFL 67 PER COOR. Triggering on loss of trip helps prevent false trips which can occur if an RX TRIP signal is latched by the trip hold flip-flop prior to a communications failure.

When a communications failure occurs, trip and guard are both lost; the guard clear timer will never be triggered if it is waiting for a guard signal to be established. The guard clear timer provides the only means of resetting the trip hold flip-flop. Once it is reset, the local breaker will trip without the benefit of a permissive trip signal any time the local relays detect a fault. By triggering the guard clear timer with the off-going RX TRIP signal, a reliable triggering source is available for the timer, and the trip signal latched by the trip hold flip-flop will be reset after a maximum of 8 ms.

(4) Prolonged Keying Timer. The prolonged keying timer is triggered by changes in the current reversal relay input signal. If an internal fault occurs on a protected line, the breakers at both ends must trip. If the remote breaker trips slowly or fails to trip, the local terminal must continue to send a permissive trip signal after its breaker opens. If it doesn't, the remote terminal will lose its permissive trip signal and the remote breaker will not operate at all. The permissive trip signal is maintained from the local terminal by the prolonged keying timer for 400 ms after the local forward-looking relays drop out and the current reversal signal is lost. This gives the remote terminal enough time for sequential tripping after the system fault currents re-distribute themselves.

The prolonged keying timer has a pick-up delay to prevent the creation of false prolonged keying signals by transient pulses at the current reversal input. The trip buffer module requires that a trip last for at least 100 μs before it will be recognized. Once it is recognized and accepted as a valid trip, it will be stretched to last a minimum of 2 ms. Data will be passed between the interrupt and background programs only at the start of INTERRUPT Ø. Input data read at the start of INTERRUPT Ø is used as reference data by the data program. Because the reference data is read at these precise intervals, the background program must see a trip change at least three times in order to guarantee that the change has lasted at least 2 ms. Since the

background program not runs for four message period intervals, the pick-up delay will last between 12 and 16 message intervals (3.2 to 4.3 ms). The output of the prolonged keying timer will remain on for the duration of the current reversal signal. It will become active again when the current reversal signal turns off; starting at this point, it will be held on for 400 ms. If the current reversal signal turns on again during this 400-ms period, the prolonged keying timer will be reset. When the current reversal signal turns off again, the prolonged keying timer will be activated again, and turn off 400 ms later.

(5) Echo Timer. The echo timer is triggered by the echo input signal, but the prolonged keying timer must be off before the echo timer can be energized. Its time period can be programmed to any value from 30 to 285 ms. The echo timer's output will immediately turn off if the echo input turns off, or if the prolonged keying timer output turns on. The reset condition always dominates from either source.

Echo keying is used to provide switch-into-fault and weak-feed protection. To illustrate its operation, consider an internal fault occurring on the line linking the local and remote stations, with the breakers at both stations tripped. If the remote breaker is energized, it will immediately detect that the fault still exists, and send a permissive trip signal to the local station. Since the local breaker is open, the local RFL 9700 will not detect a fault, so it won't send the permissive trip signal that the remote RFL 9700 needs to trip the remote breaker. The same condition can exist if the remote station sees a strong-feed fault while the local station sees a weak one. Again, the local RFL 9700 would not send the required permissive trip signal, simply because it doesn't see a fault.

Echo keying is used to correct this situation. Each station is equipped with a set of reverse-looking relay contacts, which will detect external faults. If these contacts don't operate, it means that any existing fault must be an internal fault. Whenever these reverse-looking contacts do not detect a fault, an echo input signal will be supplied to the transmitter interface module. This will cause any permissive trip signal received from the remote station to be echoed back. In effect, the remote station is providing its own permissive signal.

Whenever echo keying is used, there is the possibility of a bus fault causing a false trip. Suppose that the bus fault occurs behind the local station, and that the local station's reverse-looking relays see it and operate. The forward-looking relays at the remote station will see this fault, if it is within their "reach." When this happens, the remote station will send a permissive signal. The local station will not echo the permissive signal back, because it has no echo input signal. The remote station will not trip its breaker; since the fault is not internal, this is a normal condition. When the bus fault is cleared, the local station's reverse-looking relays will sense the cleared fault and supply an echo input signal.

The remote station's forward-looking relays will also sense the cleared fault, but will still be sending a permissive trip signal because of the action of the prolonged keying timer. Without the echo timer, this signal would be echoed back and the remote breaker would trip. The echo timer is used to prevent a received trip signal from being echoed back until the timer times out. During the time-out period, the remote RFL 9700 should detect that the fault has been removed and stop sending the trip signal to the local RFL 9700.

While echo keying solves one problem, it creates another in systems using prolonged keying. If an internal fault occurs on the line between the local and remote stations, it will be sensed at both stations. They will send permissive trip signals to each other, and the breakers at both stations will trip. However, once the fault is cleared, the stations will continue to echo back the trip signals they are receiving, because the prolonged keying timers are active at both RFL 9700's. In effect, the RFL 9700's are continuously transmitting trip signals; this is referred to as an "echo lock-up" condition.

Echo lock-up is prevented by having the prolonged keying timer disable the echo timer until the prolonged keying timer times out. The echo timer will not be triggered until the 400-ms prolonged keying interval has passed. From this point, the delay programmed into the echo timer comes into play. Either RFL 9700 will be disabled from echoing back a received trip signal until this time-out interval is over. By this time, both RFL 9700's will have stopped sending trip signals.

The echo timer input is combined with the inverted output of the prolonged keying timer, so that if the prolonged keying timer is on, the echo timer will be disabled. If the echo timer is already on when the prolonged keying timer turns on, it will be immediately shut off. This would be interpreted by the echo timer software as an echo input signal turning off.

e. Permissive Coordinating Operation. The permissive coordinating program contains two basic parts: a background program containing individual modules for each permissive coordinating timer, and additions

to the various interrupt routines that provide fast responses to changes in the TRIP input signals.

When the transmitter interface module's permissive coordinating option is active, the echo and current reversal signals associated with a permissive channel become two of the inputs to the trip buffer module. All the trip inputs are active-low; they are inverted for processing by the software as active-high signals and the outputs are re-inverted to produce the active-low signals required to fire the solid-state output relays.

The receiver input contact byte contains the permissive trip signal that was sent from the remote transmitter. The GUARD function block will produce the accompanying guard signal. These two signals become the RX TRIP and RX GUARD signals for the permissive coordinating function.

The ECHO, CURRENT REVERSAL, RX TRIP, and RX GUARD signals are then passed through the permissive coordinating algorithms. Two output signals are produced: RECEIVED TRIP and KEY TX TO TRIP.

RECEIVED TRIP is the name given to the trip signal on the local receiver output contact latch. It is the TRIP signal for the local breaker. The local RFL 9700 will not issue this signal unless it has received the RX TRIP signal from the remote RFL 9700, along with the local current reversal trip signal.

KEY TX TO TRIP is a transmitter output function. It can be produced by the echo function, or it is produced when the local current reversal relays detect a fault. It is the permissive trip signal being transmitted to the remote receiver.

The permissive coordinating function cannot be used in a unidirectional system. When permissive coordinating is installed, the operator must enable both the receiver and transmitter software functions before the program can be executed. Each RFL 9700 in the permissive coordinating scheme must contain all the modules required to configure a full duplex system. If the software is not enabled or all the modules are not present, the program will never exit its initialization block, and a fatal alarm signal will be issued.

Table 11-2. Replaceable parts, RFL 97A LOGIC CPU Logic CPU Module Assembly No. 103535-1

Circuit Symbol (Figs. 11-5 & 11-6)	Description	Part Number
	CAPACITORS	
C1	Capacitor,electrolytic,47µF,20%,16V,Nichicon ULB1C470M or equiv.	1007 1629
C2-11,14-17,19,22-26, 29-31	Capacitor,X7R ceramic,0.01µF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C12,13	Not used.	
C18,21	Capacitor,ceramic,33pF,5%,100V,AVX SA101A330JAA or equiv.	0125 13305
C19	Capacitor,X7R ceramic,0.1µF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C20	Resistor,zero-ohm,1/4-watt size,Corning OMA07 or equiv.	1510 2217
C27,28	Capacitor,X7R ceramic,0.033µF,10%,50V,AVX SA205C333KAA or equiv.	0130 53331
	RESISTORS	
R1	Resistor,metal film,200Ω,1%,1/4W, Type RN1/4	0410 1221
R2	Resistor,metal film,1.21KΩ,1%,1/4W, Type RN1/4	0410 1296
R3	Resistor,metal film,24.3Ω,1%,1/4W,Mepco/Electra 5053YD24R30F or equiv.	1510 2235
R4	Resistor,metal film,100KΩ,1%,1/4W, Type RN1/4	0410 1480
R5,6	Resistor,metal film,499Ω,1%,1/4W, Type RN1/4	0410 1259
R7	Resistor,metal film,143KΩ,1%,1/4W, Type RN1/4	0410 1495

Table 11-2. Replaceable parts, RFL 97A LOGIC CPU Logic CPU Module - continued.

Circuit Symbol (Figs. 11-5 & 11-6)	Description	Part Number
	RESISTORS - continued.	
R8	Resistor,metal film,5.62KΩ,1%,1/4W, Type RN1/4	0410 1360
RZ1-4,8-10	Resistor network,nine 10KΩ 2% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-103 or equiv.	32622
RZ5,6	Not used.	
RZ7	Resistor network,ten 221Ω 1% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-221 or equiv.	30165
	SEMICONDUCTORS	
DS1,2	Light-emitting diode array (four),red,right-angle PC mount,Industrial Devices 5640E1 or equiv.	30162
Q1	Transistor,PNP,2N4121	98486
U1	Microprocessor CPU,8-bit,8-MHz,Zilog Z84C0008PEC or equiv.	0640 18
U2	EPROM,8K x 8,UV-erasable,70-ns access time,28-pin DIP,factory-programmed	Contact factory
U3	MOS static RAM,2K x 8,24-pin DIP,MAtra-Harris HM3-6116-9 or equiv.	0615 333
U4	MOS octal transceiver,20-pin DIP,Motorola MC74ACT245N or equiv.	0615 389
U5,6,12	MOS octal tri-state D-type flip-flop,20-pin DIP,Motorola MC74HC574N or equiv.	0615 298
U7-9,23,24	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U10,11	Not used.	
U13,16	MOS 3-to-8 line decoder/demultiplexer,16-pin DIP,Texas Instruments SN74HCT138N or equiv.	0615 309
U14	MOS hex inverter,14-pin DIP,National Semiconductor MM74HC04N or equiv.	0615 185
U15	MOS quad 2-input OR gate,14-pin DIP,Motorola MC74ACT32N or equiv.	0615 386
U17	MOS 1-of-8 line decoder,16-pin DIP,Motorola MC74ACT138N or equiv.	0615 388
U18	MOS dual D-type flip-flop,14-pin DIP,Motorola MC74ACT74N or equiv.	0615 387
U19	MOS hex inverter,unbuffered,high-speed,14-pin DIP,RCA CD74HCU04E or equiv.	0615 304
U20	Retriggerable monostable multivibrator,14-pin ceramic DIP,Texas Instruments SN54LS123J or equiv.	0610 147
U21	MOS dual D-type flip-flop w/preset and clear,14-pin DIP,National Semiconductor MM74HC74N or equiv.	0615 166
U22	Microprocessor supervisor,8-pin DIP,Maxim MAX690EPA or equiv.	0635 27
	MISCELLANEOUS COMPONENTS	
L1	Inductor,rf,molded,100µH,10%,Gowanda 10/103 or equiv.	32505 1
S1-3	Not used.	
S4,5	Switch array,SPST,8-position,16-pin DIP,Grayhill 90B08S or equiv.	98493
Y1	Crystal,quartz,16.000 MHz	30297
. . .	Shorting bar,single,Molex 90059-0009 or equiv.	98306

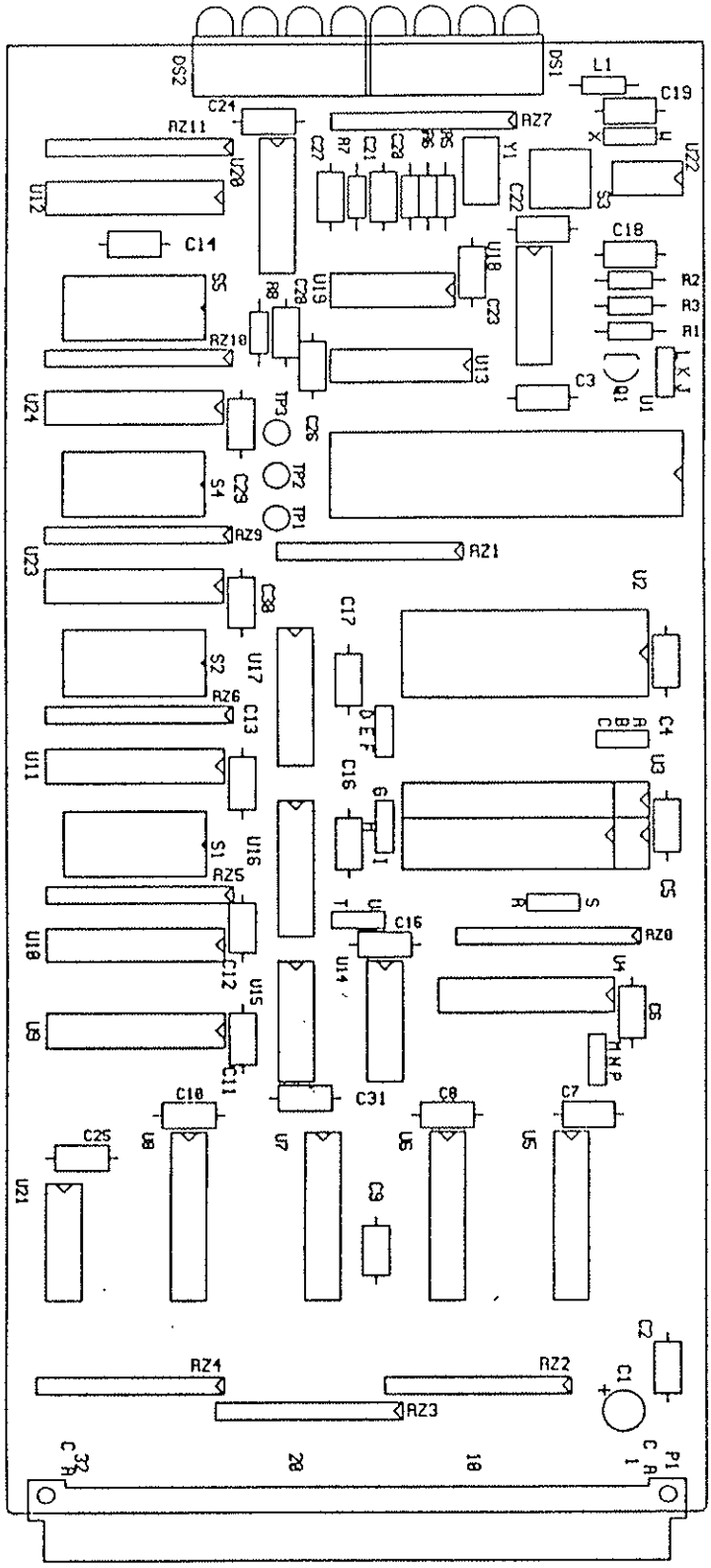


Figure 11-5. Component locator drawing, RFL 97A LOGIC CPU Logic CPU Module (Assembly No. 103535-1; Drawing No. D-101553-2, Rev. A)

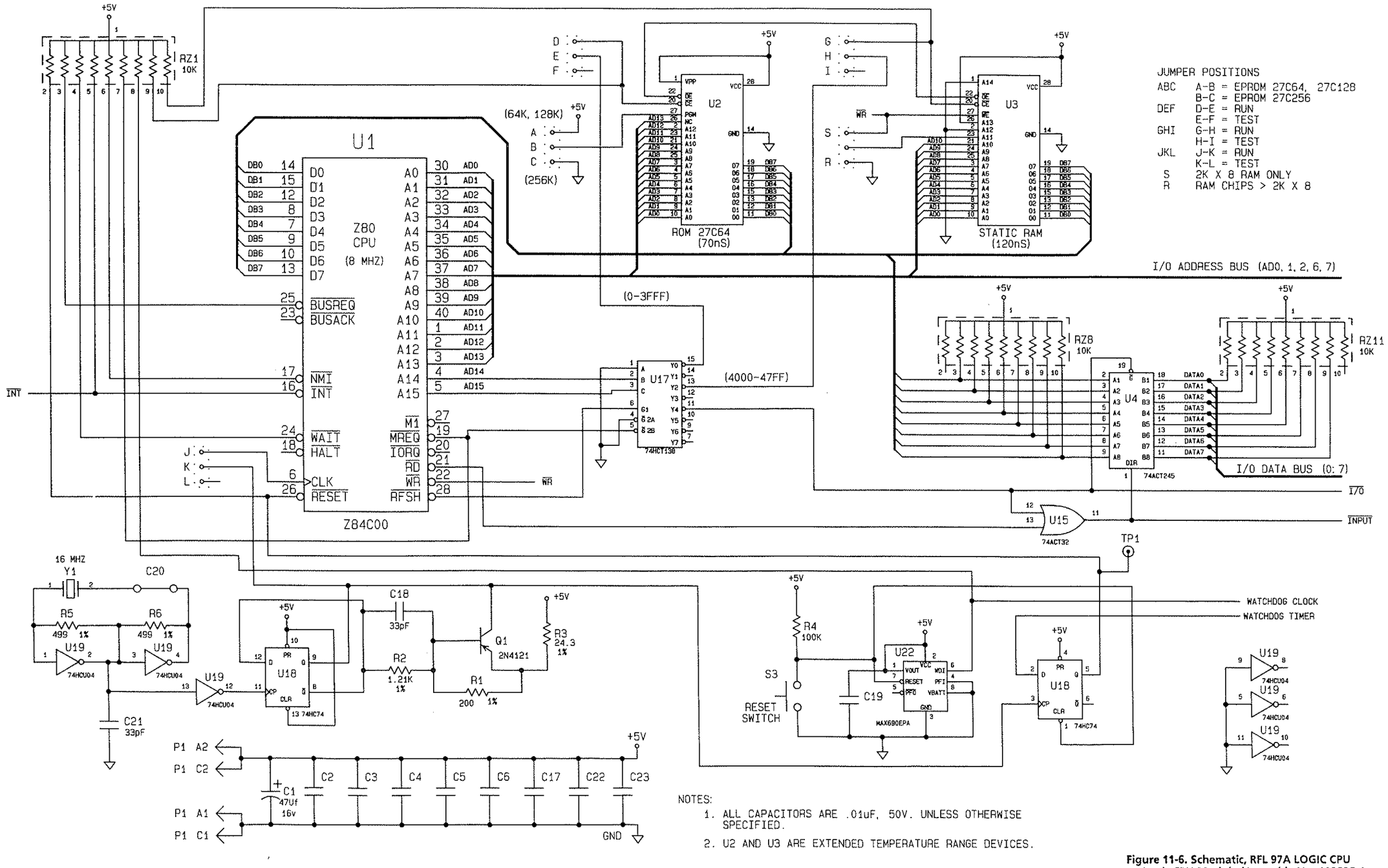


Figure 11-6. Schematic, RFL 97A LOGIC CPU Logic CPU Module (Assembly No. 103535-1; Schematic No. D-103539-1, Rev. A - Sheet 1 of 3)

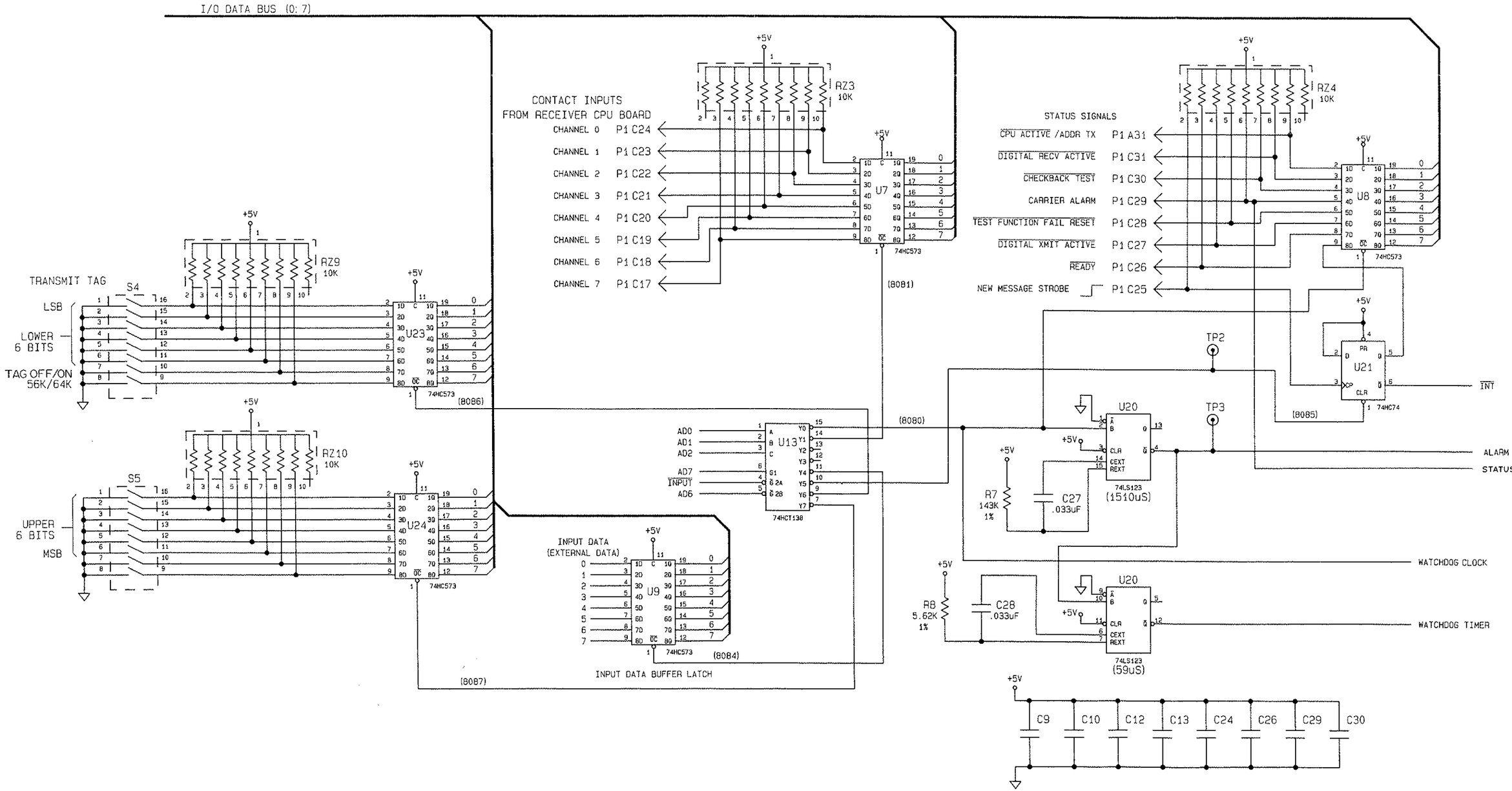


Figure 11-6. Schematic, RFL 97A LOGIC CPU Logic CPU Module (Assembly No. 103535-1; Schematic No. D-103539-1, Rev. A - Sheet 2 of 3)

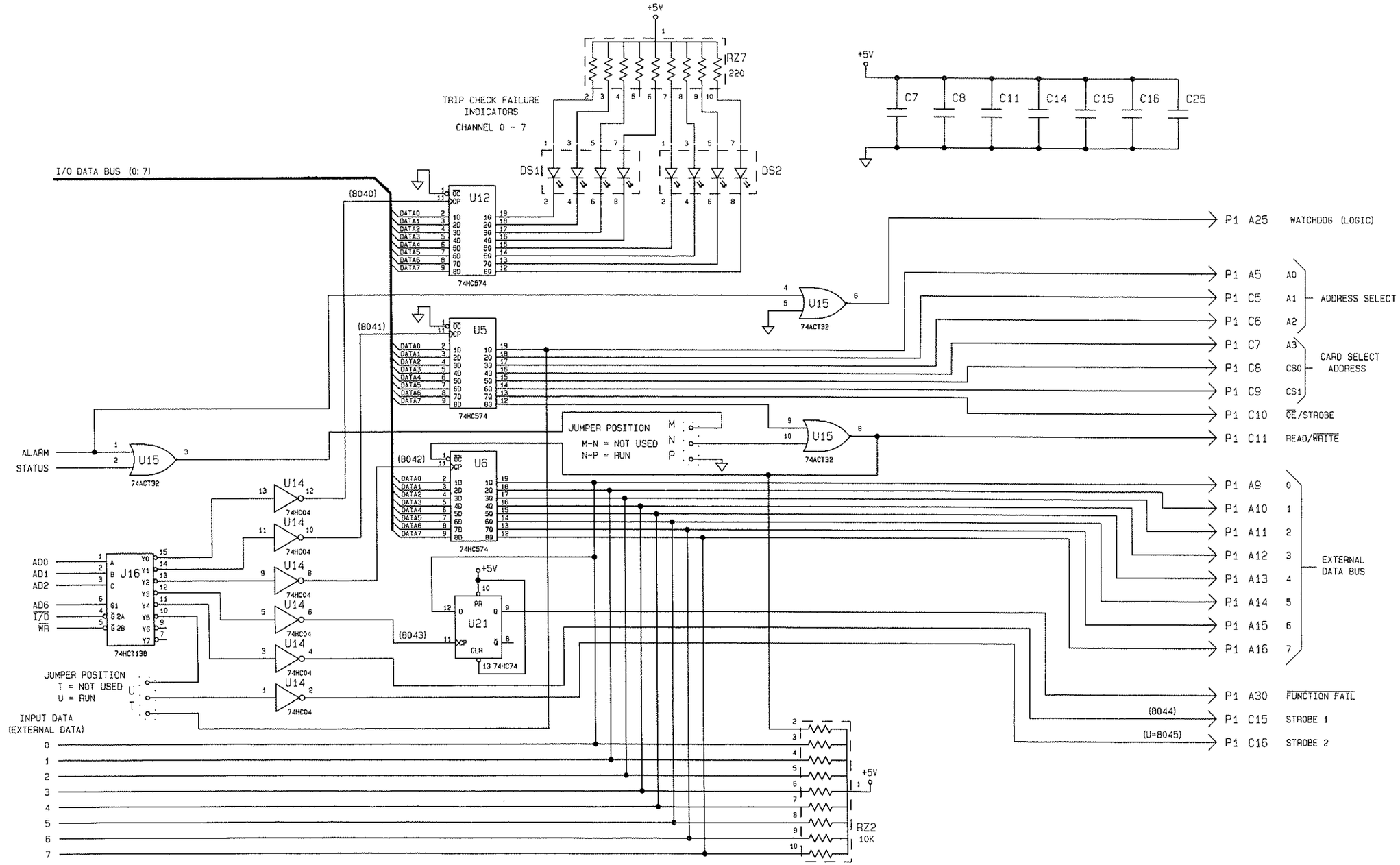


Figure 11-6. Schematic, RFL 97A LOGIC CPU Logic CPU Module (Assembly No. 103535-1; Schematic No. D-103539-1, Rev. A - Sheet 3 of 3)

Section 12. INDICATOR/OUTPUT MODULE

12.1. DESCRIPTION

The RFL 97A IND/OUT Indicator/Output Module (Fig. 12-1) contains the drivers for the output devices on the input/output module (Section 5). An LED array on its front panel indicates the channels that have received trips and displays current system status. The RFL 97A IND/OUT occupies a single dedicated module space in the RFL 97 CHAS chassis.

12.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to the RFL 97A IND/OUT module. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Load Resistance: 10,000Ω pull-up to +5-volt supply.

Input Signal Levels:
Inputs Accepted By 74HC-Type Devices:
Logic High: 3.15 Vdc minimum.
Logic Low: 0.9 Vdc maximum.
Inputs Accepted By KS74AHCT-Type Devices:
Logic High: 2.0 Vdc minimum.
Logic Low: 0.8 Vdc maximum.

Output Signal Levels:
Outputs Driven By KS74AHCT-Type Devices:
Logic High: 3.84 Vdc @ 6 mA.
Logic Low: 0.5 Vdc @ 24 mA.
Outputs Driven by 2N4401 Transistors: Capable of sinking 100 mA.

Front Panel Indicators: LED arrays on the front panel indicate when a channel has received a trip, and what condition has caused an alarm indication. A single LED (CHANNEL OK) lights when all channels are functioning properly.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

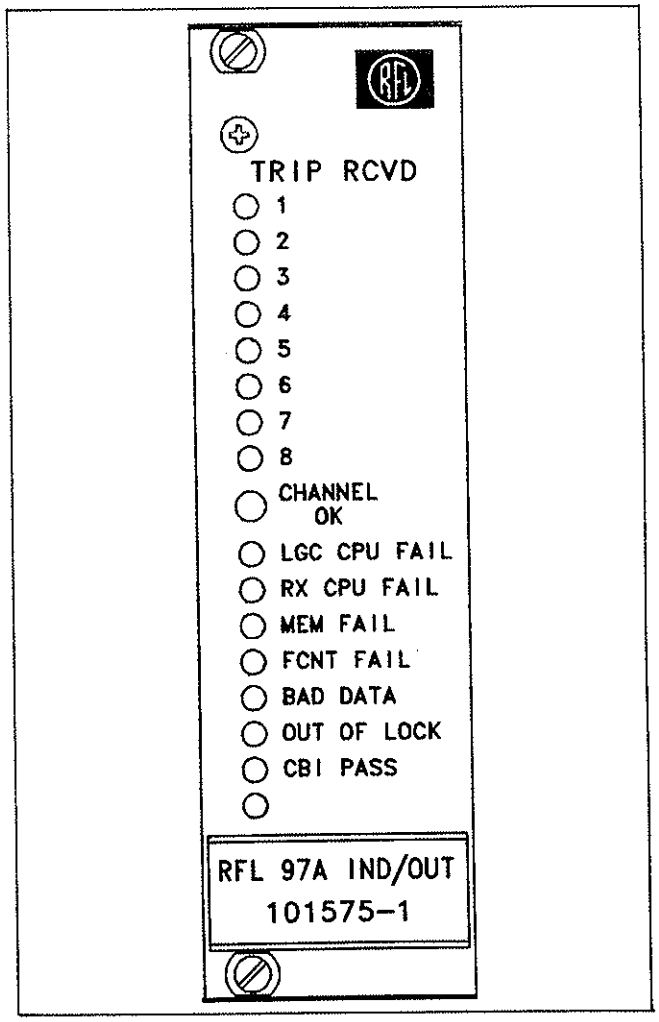


Figure 12-1. RFL 97A IND/OUT Indicator/Output Module

Input Power Requirements (from chassis supply):
+5-Volt Supply: 4.75 to 5.25 Vdc @ 275 mA.
+15-Volt Supply: 14.5 to 15.25 Vdc @ 10 mA.
-15-Volt Supply: 14.5 to 15.25 Vdc @ 10 mA.

Dimensions:
Panel Height: 5.1 inches (130 mm).
Panel Width: 1.4 inches (36 mm).
Depth (behind panel): 9.1 inches (231 mm).

12.3. THEORY OF OPERATION

The RFL 97A IND/OUT module acts as the buffer between the logic CPU module and the output relays and switches under its control. Indicators on its front

panel continuously monitor communications status; they also show when system errors occur, and when trips are received. A block diagram of the RFL 97A IND/OUT appears in Figure 12-2.

12.3.1. Address Decoders

Control bus signals from the logic CPU module are buffered by octal buffer U1 and then applied to address decoders U6 and U7. Data is only written to this module; no other modules can read data from it. In order to access the individual on-board latches (U3, U4, U5, U8, and U9), U6 must decode an address that causes its Y0 output to go low, enabling U7. In actual practice, once the output data is placed on the data bus, addressing the latch is a two-step process.

First an address is sent by CARD SELECT ADDRESS signals CS0 and CS1 on edge connector pins P1-C8 and P1-C9. The READ/WRITE* signal on P1-C11 is held low to serve as the WRITE* signal, and P1-C10 is forced high; this is the STROBE signal). Several microseconds later, after U6 and U7 have had a chance to decode the address, pin P1-C10 goes low to serve as the OE* signal. This allows a clean, glitch-free latching signal to appear on the outputs of U7 (Y0* on U7-15 through Y4* on U7-11). Buffer U2 places the data sent from the logic CPU module on the RFL 97A IND/OUT module's internal data bus. The decoded latch signals appearing on the output of U7 clock this data into the data latch.

12.3.2. Output Interface

Buffer chips U3, U4, and U5 form the interface to the output relays and switches on the input/output module (Section 5). These buffers sink the current necessary to energize these output devices: U3 sinks the turn-on current for the GUARD output modules, U4 sinks the current for the TRIP output modules, and U5 handles the turn-on current for the HAS TRIPPED solid-state switches. The output signals from latch U4 are also delivered to the transmitter interface module over the test bus. This enables the logic CPU module to read these signals and compare then with the data it attempted to send to the indicator/output module. If the two bytes don't match, a non-fatal alarm is initiated, the FUNCTION FAIL indicator lights, and the indicator array on the logic CPU module will show which channel (or channels) failed.

The output function test byte will match the test byte as long as jumper ABC is in position B-C and jumper DEF is in the E-F position. The RFL 9700 is capable of providing phase comparison protection on Channels 1 and 2. To implement this scheme, the jumpers must be moved to positions A-B and D-E. This allows the Channel 1 and 2 FCTN KEY signals to bypass the programmable functions and drive the output modules directly.

12.3.3. Alarm Decoder Circuits

The alarm signals developed on the other modules in the RFL 9700 are fed to buffer latch U8; the WATCHDOG LOGIC, WATCHDOG CPU, and READY signals are active-high, while the others are active-low. The WATCHDOG CPU signal is supplied with a pull-down resistor, so that the WATCHDOG CPU alarm will be bypassed in transmit-only terminals that do not contain receiver CPU modules.

The WATCHDOG LOGIC alarm signal controls the OUTPUT ENABLE pin (OE*) of all output buffer latches. If a failure occurs on the logic CPU module, these latches will be immediately disabled.

The receiver CPU module's MEMORY FAILURE signal is input to U8 directly from that card's output status latch. When the logic CPU module detects a memory error, it issues a CLR signal to U9A by way of decoder U7. This causes the output of U10B to go high, and the output of U10C to go low. This signal is sent to U17, and lights the MEMORY FAILURE indicator. This indicator will show that a memory failure has occurred, but it does not indicate which module has failed. The failed module will also have an active watchdog alarm.

12.3.4. Communications Alarm Delay Circuit

Octal D-type latch U12, timer U20, counter U21, programmable logic devices U22 and U23, and their associated components form a communications alarm delay circuit. It allows a fixed delay to be added to the RFL 9700's response to alarm conditions.

a. **Delay Circuit Programming.** The communications alarm delay circuit's operation is programmed by DIP switch SW1:

SW1-1 and 1-2 These switches select the delay time:

Delay Time	SW1-1	SW1-2
125 ms	ON	ON
500 ms	OFF	ON
1 sec	ON	OFF
2 sec	OFF	OFF

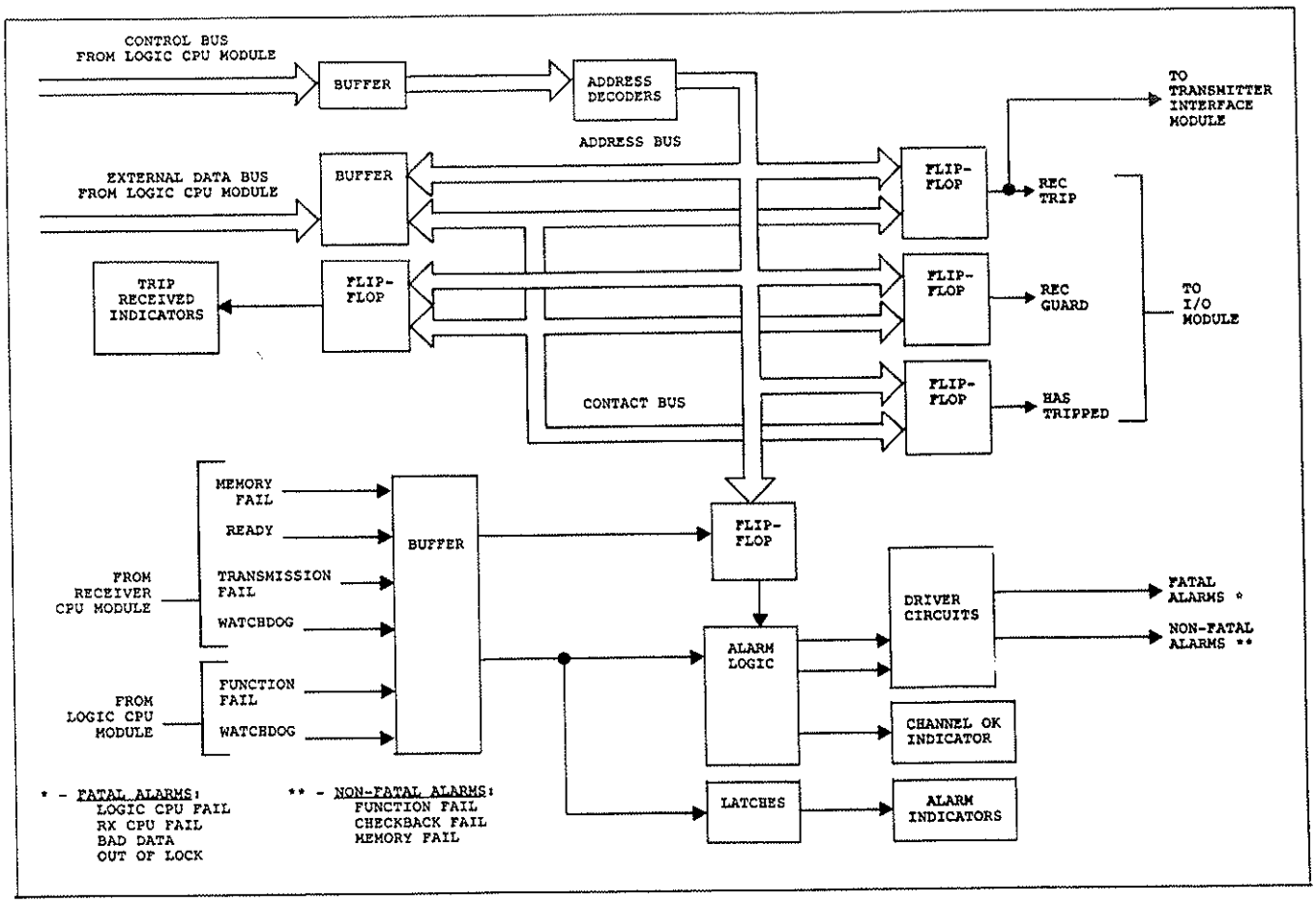


Figure 12-2. Block diagram, RFL 97A IND/OUT Indicator/Output Module

SW1-3 This switch controls the alarm delay function. To enable the function (add a delay), place SW1-3 in the ON position. To disable it (no added delay), place SW1-3 in the OFF position.

SW1-4 This switch determines which alarm outputs are subject to the delay set by Sw1-1 and SW1-2. When SW1-4 is placed in the ON position, non-fatal alarm outputs are not subject to the delay but fatal alarms are delayed. To delay all alarm outputs (fatal and non-fatal), place SW1-4 in the OFF position.

b. Timer/Counter. U20 functions as an astable multivibrator. It supplies a 4096-Hz clock signal to U21. U21's outputs provide four reference signals. One of these signals is selected by the logic circuits to determine the delay circuit's delay time. The selection is controlled by the settings of SW1-1 and SW1-2:

Output	Pin No.	No. Of Counts	Delay
Q14	U21-3	8192	2 seconds
Q13	U21-2	4096	1 second
Q12	U21-1	2048	500 ms
Q10	U21-15	512	125 ms

c. Logic Circuits. Programmable logic devices U22 and U23 perform the communications alarm delay circuit's logic functions. The desired delay time is set by SW1-1 and SW1-2; this directs one of U21's outputs to a data selector inside U22. The data selector's output will go high when the selected timing reference signal goes high. This high-going signal is used to latch the state of the /RDY and /TF communications alarm signals. It also clears U21 and restarts the counter. If SW1-3 has been placed in the ON position, the alarm delay function has been enabled and the fatal alarm signal will reflect the status of the communications alarm signals.

Any time the communications alarm signals change state, U21 is cleared by a pulse from U22's RESET output (U22-17). Resistor R25 and capacitor C23 shape this pulse. When the communications alarm delay function is enabled, the reset pulse blocks any change in state of the communications alarms from appearing on the fatal alarm output unless they have not changed state during the time programmed by SW1-1 and SW1-2.

Resistors R19 through R21, capacitor C25, and diode CR4 provide a path for communications alarms to appear on the non-fatal alarm output without delay. This fast-attack/slow-decay circuit eliminates nuisance alarms. If SW1-4 is in the ON position, the output of this network is shorted; this prevents communications alarms from appearing on the non-fatal alarm output. The LED indicators on the front panel will reflect the instantaneous true state of all alarm signals, regardless of how SW1 is set.

NOTE

The WLOG and WCPU fatal alarms cannot be programmed to trip the non-fatal alarm relay, and they are not subject to any delay. Once active, they instantly cause the fatal alarm relay to change states.

12.3.5. Alarm Relay Drive Circuits

There are two electromechanical alarm relays in each RFL 9700: one for fatal alarms, and one for non-fatal alarms. During normal operation, these relays are kept in an energized state by their drive circuits. If their drive circuits detect an error, they will drop out and their contacts will change state to indicate an alarm condition. The alarm relays will also drop out if the RFL 97A IND/OUT module is removed from the chassis.

The alarm relay drive circuits consist of optically-isolated photo-Darlingtons U14 and U15, transistors Q1 and Q2, resistors R10 through R12, and diodes CR1 through CR3. A logic circuit formed from three NAND gates in U11 and two NOR gates in U13 decode the non-fatal alarms; as long as all signals are high, the non-fatal alarm relay coil will be energized.

Diode CR2 and resistor R14 provide a small amount of negative voltage to the bases of Q1 and Q2. This insures that Q1 and Q2 will turn off when alarms occur.

12.3.6. Indicator Drive Circuits

Latch U16 provides the sink current required to energize the TRIP RCVD indicators on the RFL 97A IND/OUT's front panel. U16 is clocked by the same signal that clocks U4; this means that the indicators will light to indicate the trip data as it is output, not as it is received. This gives them the ability to display the trip hold and unblock intervals. They will also indicate any channels that are having their trips blocked by the guard-before-trip function. Latch U17 sinks the current necessary to light the error indicators. All error signals to this latch are active-low. A NOR gate in U13 and a NAND gate in U10 are used to invert the active-high alarms before they are passed to U17.

The TRANSMISSION FAIL and READY signals are fed into a NAND gate in U11. As long as communications are good, both signals will be high and U12 will sink the current required to light CHANNEL OK indicator DS3. DS3 will remain on as long as both watchdog alarm signals are high.

12.3.7. Power-On Reset Circuit

For the first few milliseconds after the RFL 9700 is turned on, transient signals can exist on the RFL 97A IND/OUT module's internal data bus. If the output latches were enabled, these signals could be sent to the input/output module and cause false trips. Capacitor C20, diode CR4, and resistor R13 are used to insure that U8's outputs remain disabled for about 100 ms after turn-on. This provides protection against these possible false trips.

Table 12-1. Replaceable parts, RFL 97A IND/OUT Indicator/Output Module
Assembly No. 101575-1

Circuit Symbol (Figs. 12-2 & 12-4)	Description	Part Number
	CAPACITORS	
C1	Capacitor,electrolytic,47µF,20%,16V,Nichicon ULB1C470M or equiv.	1007 1629
C2-19,21,24,26-29	Capacitor,X7R ceramic,0.01µF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C20	Capacitor,tantalum,4.7µF,20%,20V,Kemet T3228475M020AS or equiv.	1007 711
C22	Capacitor,polyester,0.0039µF,2%,100V,Wesco 32P or equiv.	5115 15
C23	Capacitor,ceramic,220pF,5%,100V,AVX SA101A221JAA or equiv.	0125 12215
C25	Capacitor,metallized polycarbonate,0.47µF,2%,100V,Wesco 32MPC or equiv.	1007 971
	RESISTORS	
R1-8	Resistor,metal film,649Ω,1%,1/4W, Type RN1/4	0410 1270
R9,22-24	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
R10,15	Resistor,metal film,3.16KΩ,1%,1/4W, Type RN1/4	0410 1336
R11,16	Resistor,metal film,4.64KΩ,1%,1/4W, Type RN1/4	0410 1352
R12,17	Resistor,metal film,301Ω,1%,1/4W, Type RN1/4	0410 1238
R13	Resistor,metal film,33.2KΩ,1%,1/4W, Type RN1/4	0410 1434
R14	Resistor,metal film,2.67KΩ,1%,1/4W, Type RN1/4	0410 1329
R18	Resistor,metal film,178Ω,1%,1/4W, Type RN1/4	0410 1216
R19	Resistor,metal film,499KΩ,1%,1/4W, Type RN1/4	0410 1547
R20	Resistor,metal film,1.5KΩ,1%,1/4W, Type RN1/4	0410 1305
R21	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R25	Resistor,metal film,4.75KΩ,1%,1/4W, Type RN1/4	0410 1353
R26	Resistor,metal film,45.3KΩ,1%,1/4W, Type RN1/4	0410 1447
RZ1,3,6	Resistor network,nine 10KΩ 2% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-103 or equiv.	32622
RZ2	Resistor network,seven 10KΩ 2% resistors,1.1W total,8-pin SIP,CTS of Berne 750-81-R10K or equiv.	47878
RZ4,5	Resistor network,ten 221Ω 1% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-221 or equiv.	30165
	SEMICONDUCTORS	
CR1,3	Diode,silicon,1N4001	38876
CR2,4,5	Diode,silicon,1N914B or 1N4448	26482
DS1,2,4,5	Light-emitting diode,red,right-angle PC mount,Industrial Devices 5360F1 or equiv.	98487
DS3	Light-emitting diode,green,right-angle PC mount,Data Display Products PCL-200-EG or equiv.	32566

Table 12-1. Replaceable parts, RFL 97A IND/OUT Indicator/Output Module - continued.

Circuit Symbol (Figs. 12-2 & 12-4)	Description	Part Number
	SEMICONDUCTORS - continued.	
Q1,2	Transistor,NPN,40V,TO-92 case,2N4401	42574
U1,2	MOS octal tri-state non-inverting buffer/line driver,20-pin DIP, National Semiconductor MM74HC541N or equiv.	0615 297
U3-5,16	MOS octal tri-state D-type flip-flop,20-pin DIP,Motorola MC74HC574N or equiv.	0615 298
U6,7	MOS decoder,3-line to 8-line,16-pin DIP,National Semiconductor MM74HC138N or equiv.	0615 168
U8,12,17	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U9	MOS dual D-type flip-flop w/preset and clear,14-pin DIP,National Semiconductor MM74HC74N or equiv.	0615 166
U10,11	MOS quad 2-input NAND gate,14-pin DIP,National Semiconductor MM74HC00N or equiv.	0615 159
U13	Not used.	
U14,15	Optically isolated photo-Darlington,6-pin DIP,General Instrument MCA230 or equiv.	41084
U20	MOS timer,8-pin DIP,General Electric/Intersil ICM7555IPA or equiv.	0615 328
U21	MOS 14-stage ripple-carry binary counter/divider and oscillator,16-pin DIP,RCA CD4060BE or equiv.	0615 131
U22,23	Programmable logic array (PAL), programmed at the factory	Contact factory
	MISCELLANEOUS COMPONENTS	
SW1	Switch array,four SPST switches,8-pin DIP,Grayhill 90B04S or equiv.	98492
. . .	Shorting bar,single,Molex 90059-0009 or equiv.	98306

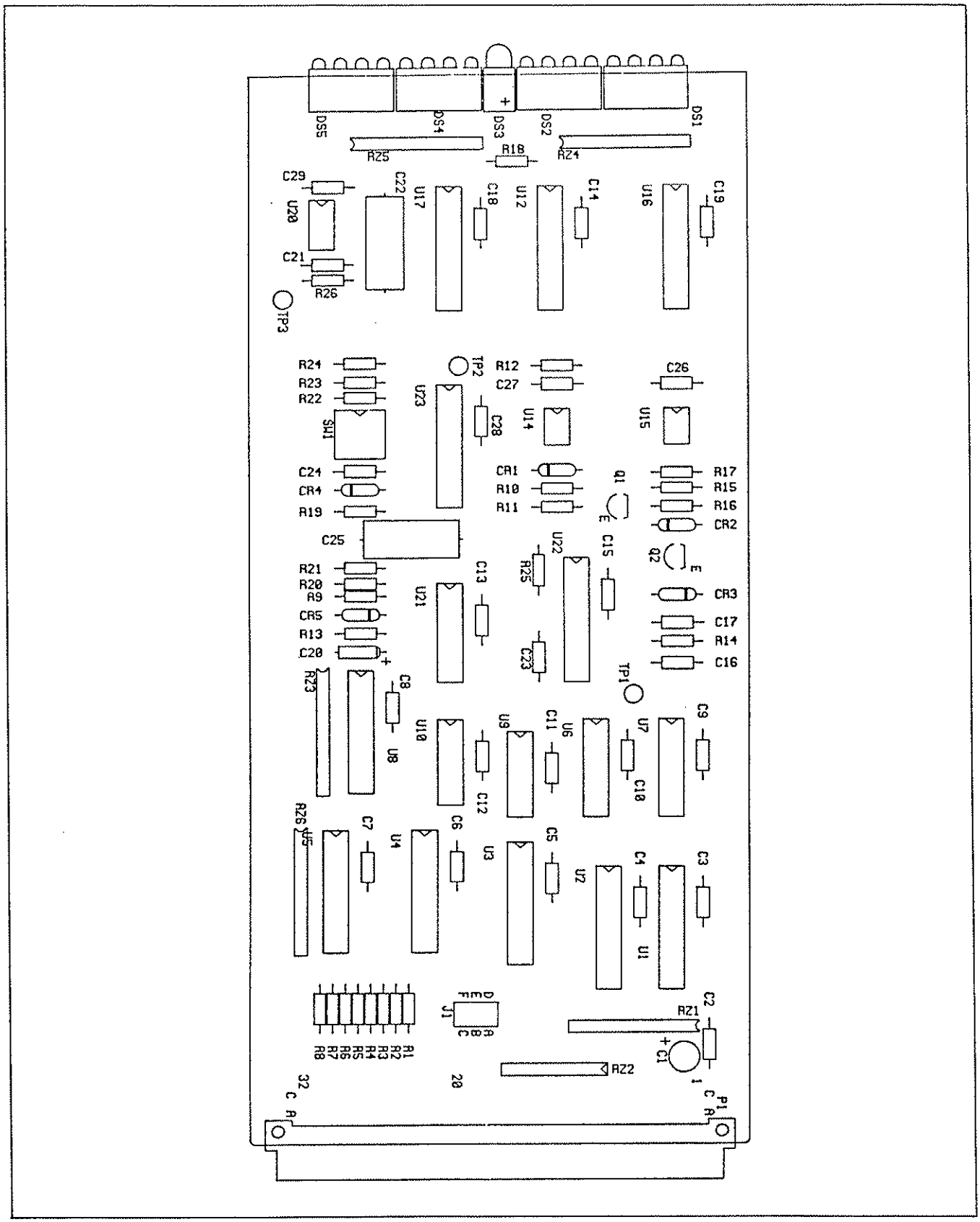
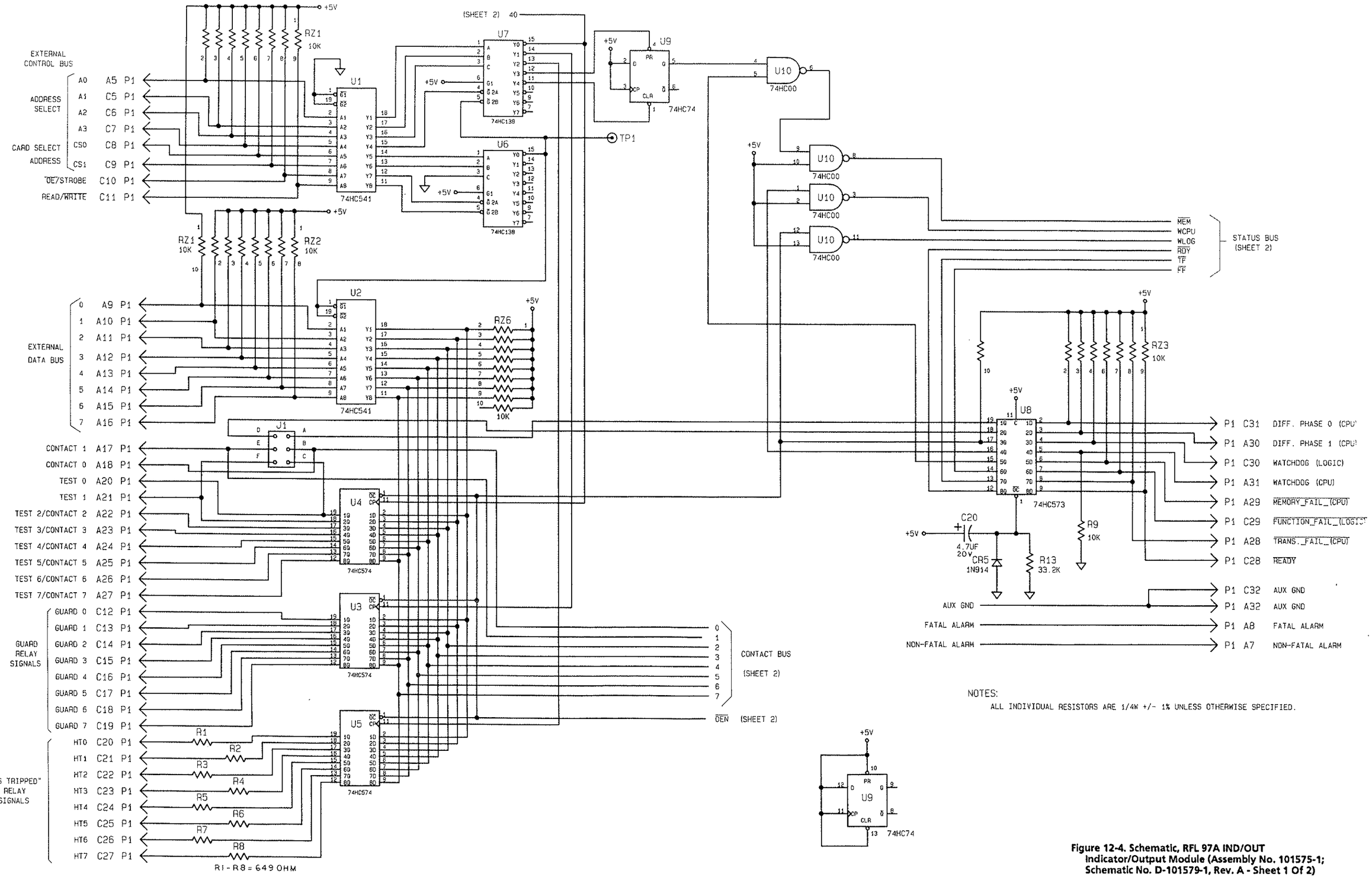


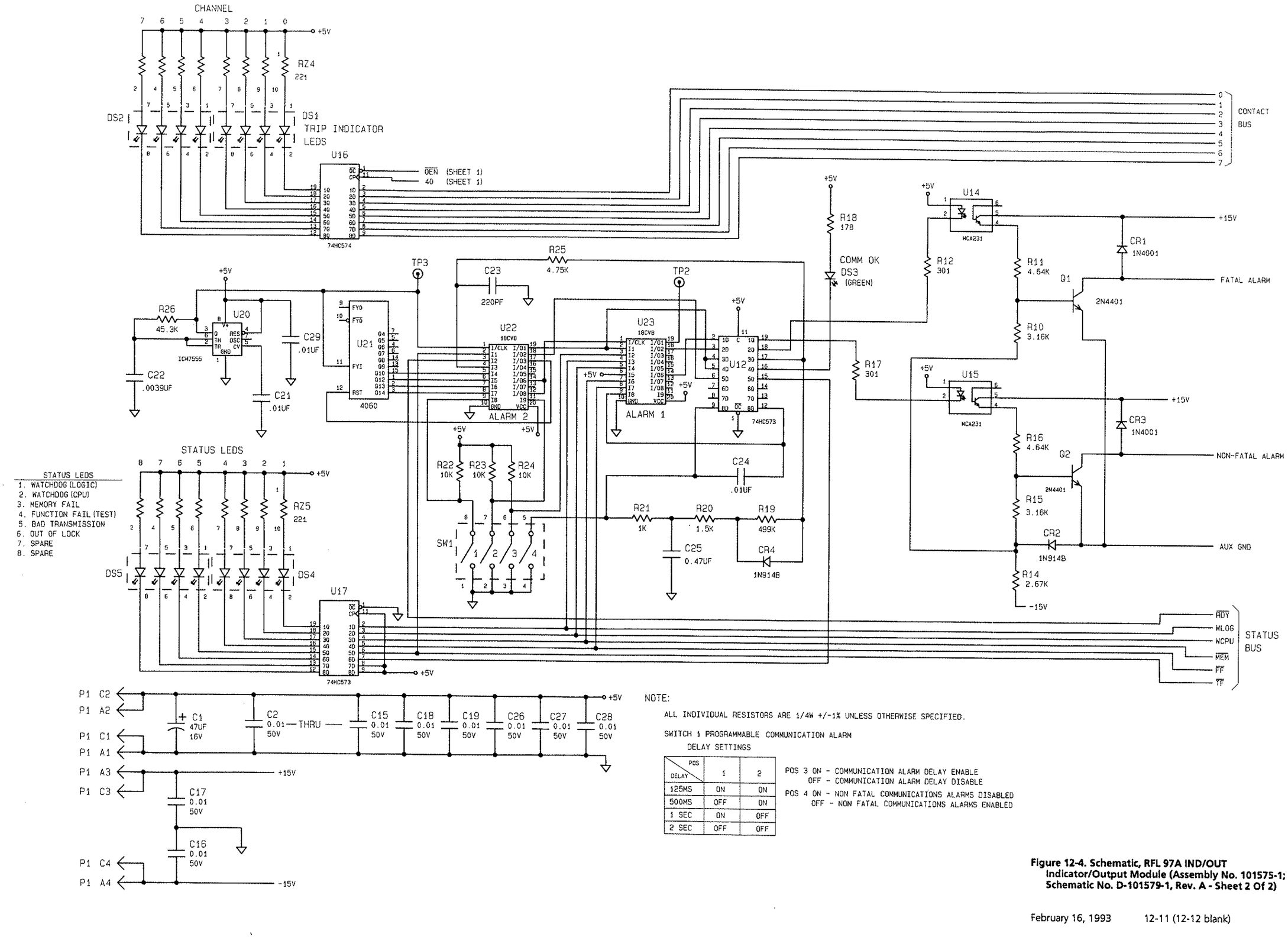
Figure 12-3. Component locator drawing, RFL 97A IND/OUT Indicator/Output Module (Assembly No. 101575-1; Drawing No. D-101578-1, Rev. A)



NOTES:

ALL INDIVIDUAL RESISTORS ARE 1/4W +/- 1% UNLESS OTHERWISE SPECIFIED.

Figure 12-4. Schematic, RFL 97A IND/OUT Indicator/Output Module (Assembly No. 101575-1; Schematic No. D-101579-1, Rev. A - Sheet 1 Of 2)



NOTE:

ALL INDIVIDUAL RESISTORS ARE 1/4W +/-1% UNLESS OTHERWISE SPECIFIED.

SWITCH 1 PROGRAMMABLE COMMUNICATION ALARM DELAY SETTINGS

DELAY \ POS	1	2
125MS	ON	ON
500MS	OFF	ON
1 SEC	ON	OFF
2 SEC	OFF	OFF

POS 3 ON - COMMUNICATION ALARM DELAY ENABLE
OFF - COMMUNICATION ALARM DELAY DISABLE

POS 4 ON - NON FATAL COMMUNICATIONS ALARMS DISABLED
OFF - NON FATAL COMMUNICATIONS ALARMS ENABLED

Figure 12-4. Schematic, RFL 97A IND/OUT Indicator/Output Module (Assembly No. 101575-1; Schematic No. D-101579-1, Rev. A - Sheet 2 Of 2)

Section 13. FIBER OPTIC TRANSMITTER MODULES

NOTE

The fiber optic emitter head selected for use with the fiber optic transmitter module will determine the fiber optic cable interface characteristics, such as wavelength, output level, and mating connector type. Refer to Section 15 of this manual for further information on the fiber optic emitter heads.

13.1. DESCRIPTION

RFL 9700 fiber optic transmitter modules accept the signals generated by the RFL 97 DIG TX module (Section 8) and condition them for optic transmission. Two different fiber optic transmitter modules are available: the RFL 97 FO INTX that accepts a single 56-Kbps RS-422 input, and the RFL 97 FO INTX-1 that contains multiplexer circuits for up to eight RS-422 channels.

Both fiber optic transmitter modules accept the data presented to their inputs and condition them for optic transmission. A subcarrier and differential phase-shift keying is used; this results in reduced bandwidth requirements and enhanced S/N ratio. A transmitter output monitor is also provided on each module, which will activate an alarm if transmitter power is lost.

Each fiber optic transmitter module occupies one dedicated module space in the RFL 97 CHAS chassis, and is used with a fiber optic emitter head that is located at the rear of the chassis. All the currently-available fiber optic emitter heads are described in Section 15 of this manual.

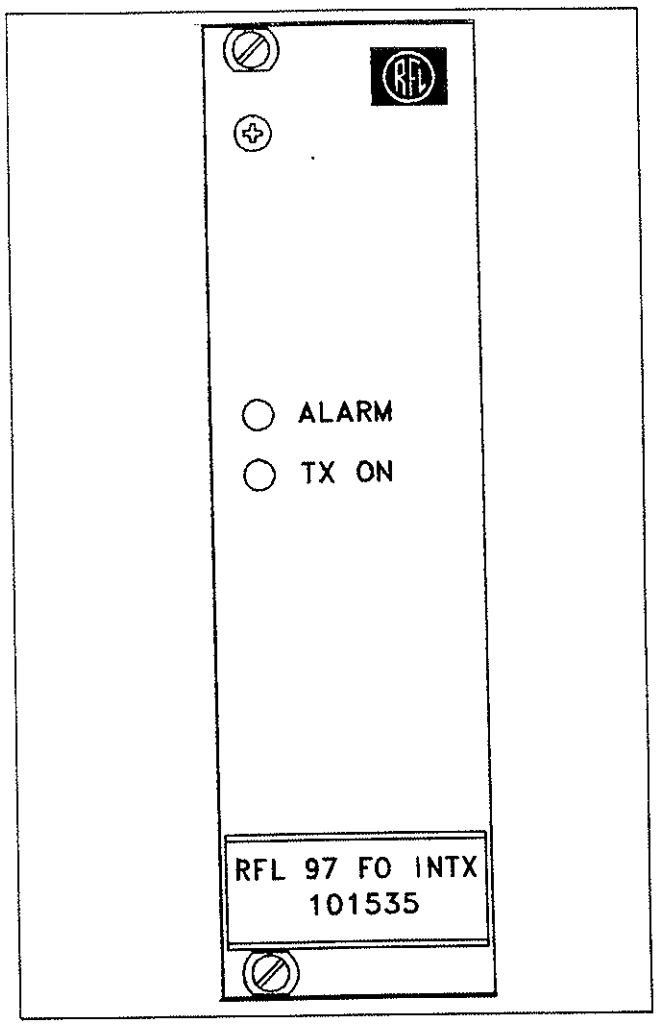


Figure 13-1. Typical RFL 9700 fiber optic transmitter module

13.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to both RFL 9700 fiber optic transmitter modules, unless otherwise indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Signal:

RFL 97 FO INTX: One RS-449 channel, obtained from chassis backplane. Maximum data rate is 56 Kbps, with a nominal amplitude of 5 Vp-p.

RFL 97 FO INTX-1: Eight RS-449 channels; one reserved for the RFL 9700 itself, the balance available for use by external equipment. Maximum data rate is 56 Kbps, with a nominal amplitude of 5 Vp-p.

Output Signal: Phase-shift keyed (PSK) signal, with a nominal level of 5 volts; used by fiber optic emitter head (Section 15) to drive light source.

STATUS Output Line: Active-high signal, placed on control bus to inform other modules in the RFL 9700 of transmission status. Line is high when input signal is being applied to module, and low when no input signal is present.

Front Panel Indicators:

ALARM: Red LED that lights when an alarm condition exists.

TX ON: Green LED that lights when an output signal is being sent to the fiber optic emitter head, and the head is producing a light signal; this is the normal operation condition.

Temperature:

Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements (from chassis supply):

+5-Volt Supply: 4.75 to 5.25 volts @ 150 mA.
+15-Volt Supply: 14.5 to 15.5 volts @ 20 mA.

Dimensions:

Panel Height: 5.1 inches (130 mm).
Panel Width: 1.4 inches (36 mm).
Depth (behind panel): 9.1 inches (231 mm).

13.3. THEORY OF OPERATION

The RFL 97 FO INTX converts a single RS-422 data input into a phase-modulated signal, suitable for transmission over a fiber optic cable. The RFL 97 FO INTX-1 accepts up to eight RS-422 data inputs, multiplexing them into a single phase-modulated output signal. A clock signal is included in the output signal; this clock signal is detected at the receiving RFL 9700 and used for synchronization.

A block diagram for both fiber optic transmitter modules appears in Figure 13-2. Figure 13-3 is a timing diagram for the RFL 97 FO INTX, and Figure 13-4 is a timing diagram for the RFL 97 FO INTX-1.

The carrier used in the both fiber optic transmitter modules has a nominal frequency of 3.136 MHz. This carrier is phase-shift modulated ±90 degrees in a T1-type format, in which logic ones are alternated from +90 degrees to -90 degrees. In other words, if a logic one is to be sent, a string of 24 consecutive ones will be transmitted as twelve positive phase shifts alternating with twelve negative ones (positive during the first time slot, and negative during the second). Then the clock synchronization pattern appears, as a bit-polar violation code consisting of two positive phase shifts alternating with two negative shifts. The bit takes 28 time slots to be transmitted (24 for data, four for the synchronization pattern). If a one is to be sent as the next bit, there would again be twelve positive phase shifts, alternating with twelve negative ones. If a zero is to be sent, an unmodulated carrier (no phase shift) will be sent for the next 24 time slots.

U15 is a level translator, that accepts RS-422 signals as a ±2-volt differential signal. Its output (pin 13) is a 5-volt logic-level signal. Only one input is applied to U15 on the RFL 97 FO INTX, across pins U15-14 and U15-15. On the RFL 97 FO INTX-1, four inputs are applied to U15, and four more are applied to level translator U22; the outputs of both translators are fed to multiplexer U20, which combines the eight inputs into one.

The signal then passes through two NOR gates in U19 and one flip-flop in U2. This alternates the signal to prepare it for the phase shift circuit.

The NAND gates in U10 are used to insert the synchronization code and a return-to-zero code into the data stream.

Flip-flops U1 and U5, NAND gates U9 and U16, and their associated components form a phase-shift modulator.

Transistor Q7, crystal Y1, and their associated components form a 6.272-MHz clock; its frequency can be monitored at test point TP1. This is the source clock for the transmitter module, as well as for the receiver module at the other end of the fiber optic cable; the receiver module will synchronize itself to this signal.

Binary counter U17 forms a 56-Kbps clock; it establishes the 24 time slots during which data will be sent, and the four time slots for sending the bipolar violation code. Flip-flop U18, binary counter U13, and NAND gate U12 work together to produce the bipolar violation synchronization code. The synchronization code is combined with the data by quad NAND gate U10.

The two front panel indicators are driven by transistor Q5. The base drive signal for Q5 comes from the fiber optic emitter head, through capacitor C17, diode CR3, and resistor R24. If the fiber optic head is producing a light signal, a voltage will be fed back to Q5's base, turning it on and lighting green XMTR ON indicator DS2. If no light signal is being produced, Q5 will turn off, and red ALARM indicator DS1 will light.

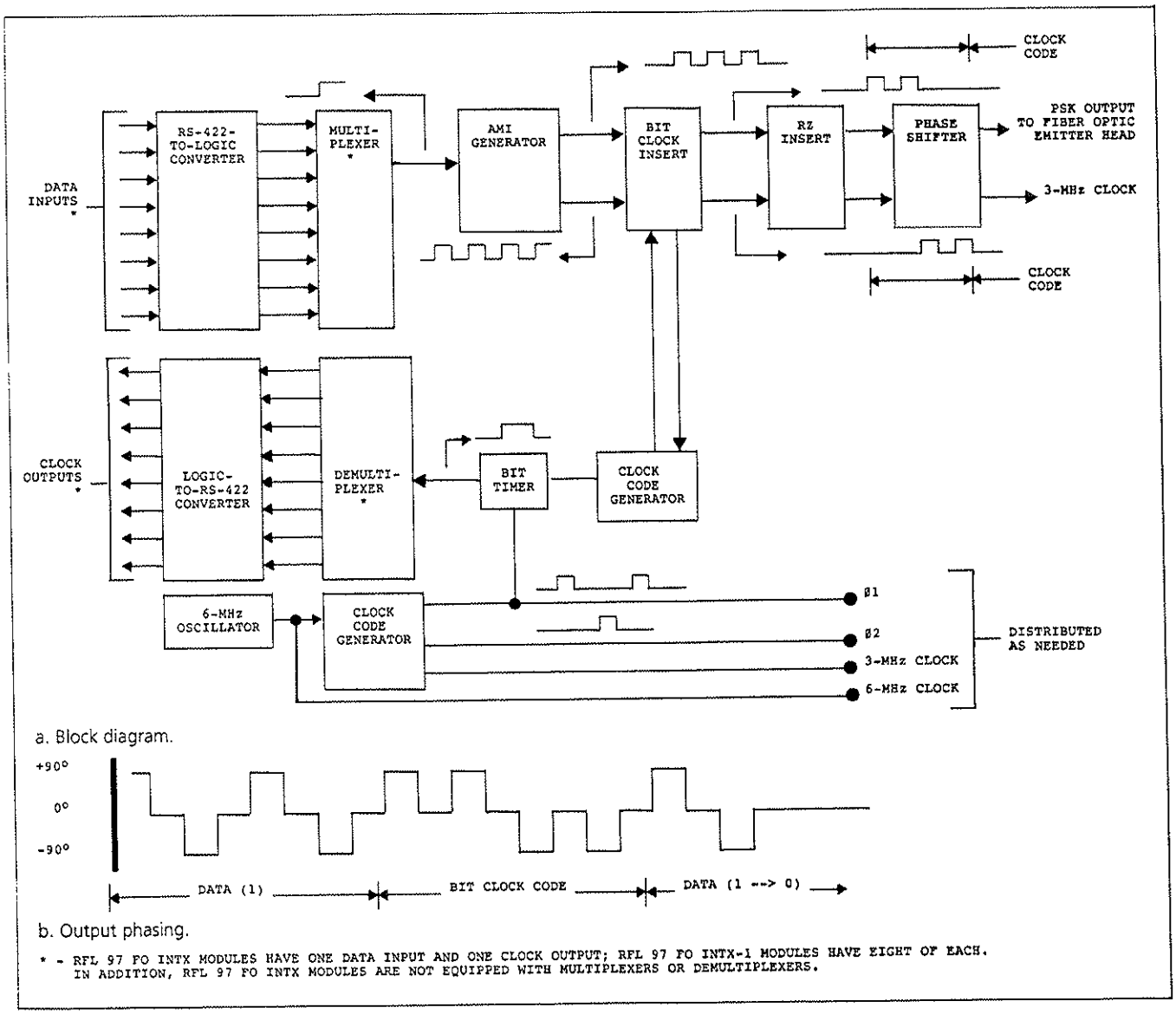


Figure 13-2. Block diagram, RFL 9700 fiber optic transmitter modules

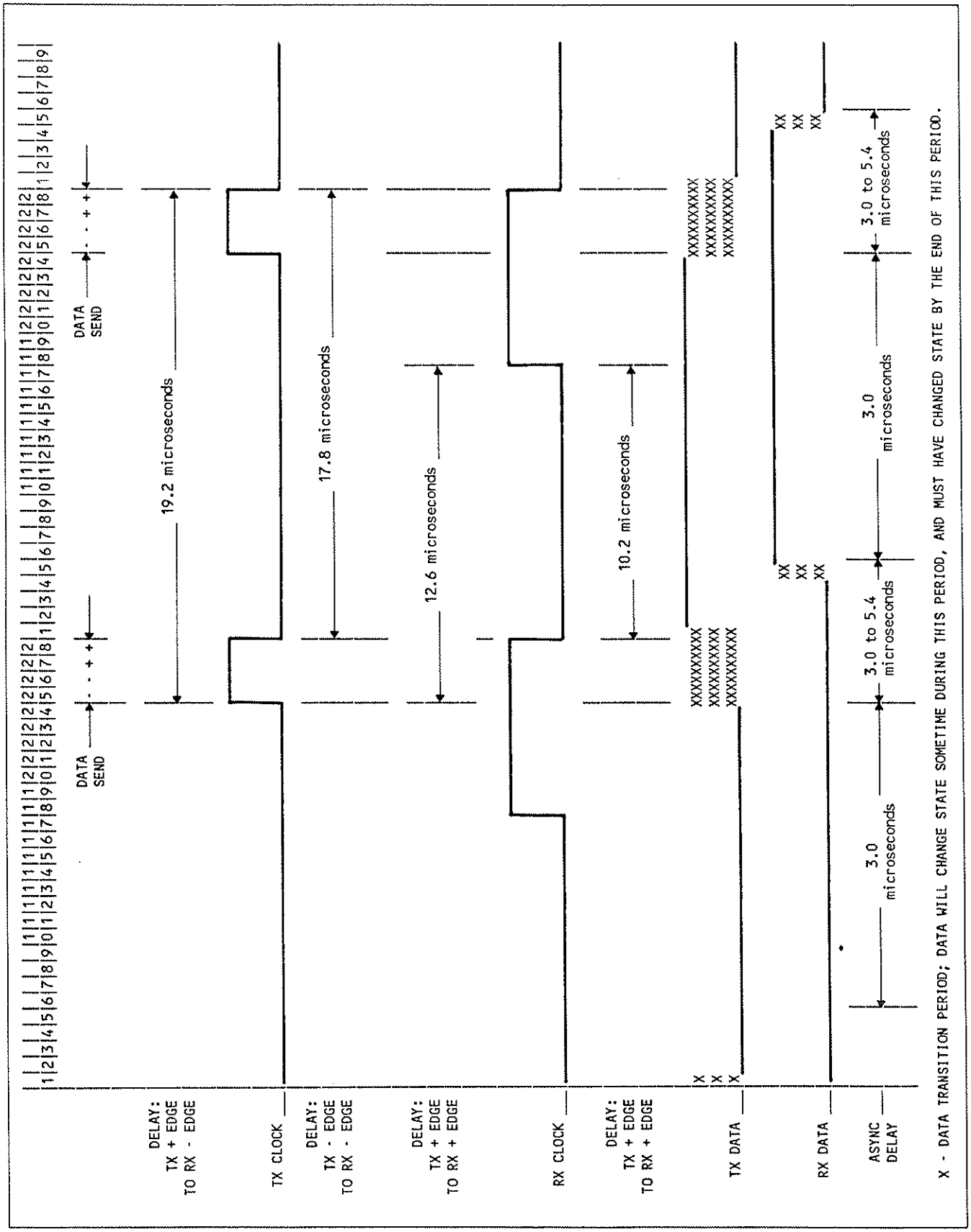


Figure 13-3. Timing diagram, RFL 97 FO INTX Single-Input Fiber Optic Transmitter Module

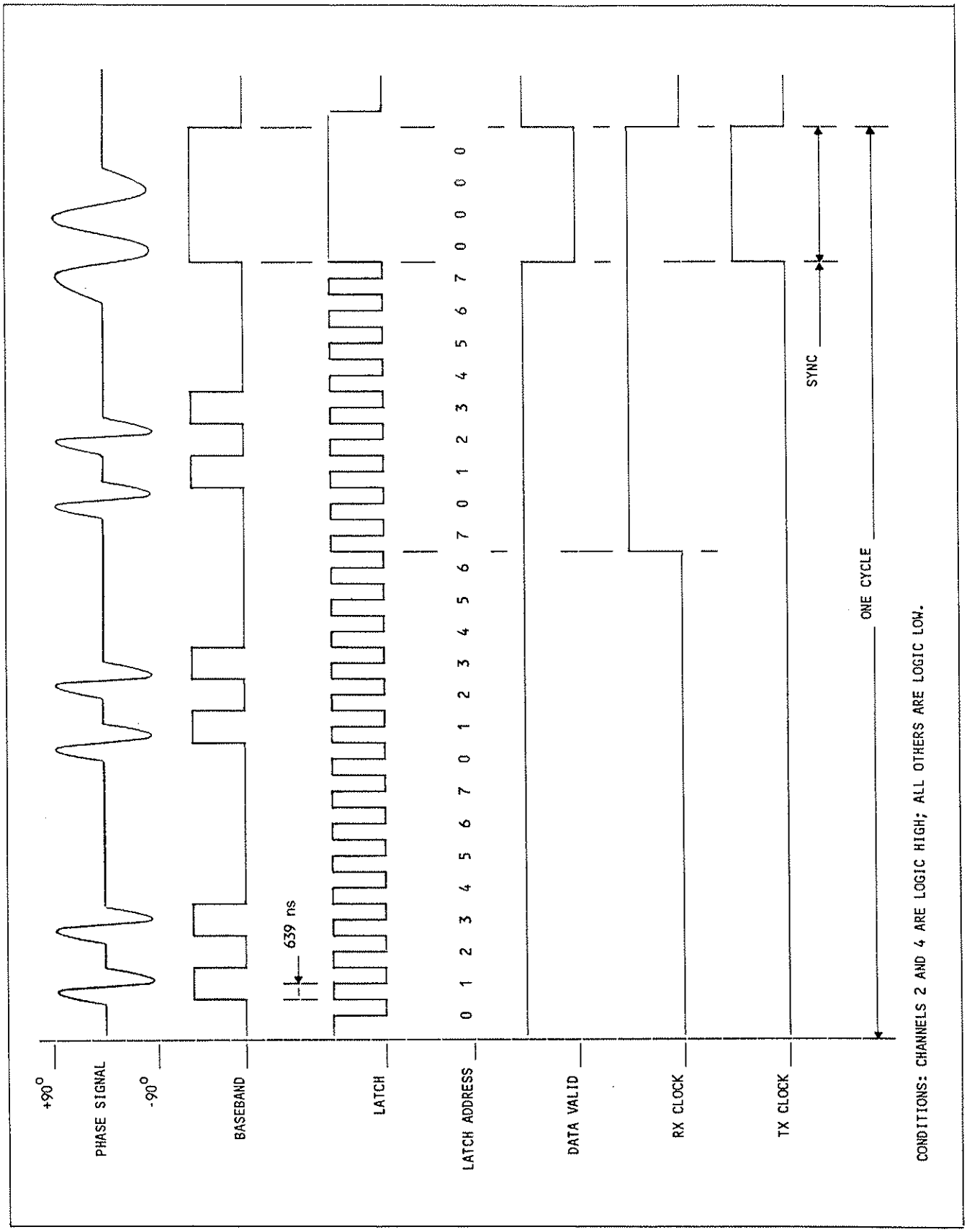


Figure 13-4. Timing diagram, RFL 97 FO INTX-1 Eight-Input Fiber Optic Transmitter Module

Table 13-1. Replaceable parts, RFL 9700 fiber optic transmitter modules
RFL 97 FO INTX (Single-Input) - Assembly No. 101530
RFL 97 FO INTX-1 (Eight-Input) - Assembly No. 101535

Circuit Symbol (Figs. 13-5 thru 13-8)	Description	Part Number
	CAPACITORS	
C1	Capacitor,tantalum,1μF,tolerance and voltage rating dependent upon model: RFL 97 FO INTX: 10%,35V;Kemet T362A105K035AS or equiv. RFL 97 FO INTX-1: 20%,35V;Kemet T322B105M035AS or equiv.	1007 1566 1007 496
C2-4,6,11-15,18,19,25	Not used.	
C5,7,10	Capacitor,X7R ceramic,0.01μF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C8	Capacitor,ceramic,150pF,5%,100V,AVX SA101A151JAA or equiv.	0125 11515
C9,16	Capacitor,ceramic,33pF,5%,100V,AVX SA101A330JAA or equiv.	0125 13305
C17,20-24,26-30, 33-36,38,39	Capacitor,X7R ceramic,0.1μF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C31,32,37	Capacitor,presence dependent upon model: RFL 97 FO INTX: Not used. RFL 97 FO INTX-1: Same as C17.	
	RESISTORS	
R1-21,27,32-46	Not used.	
R22,24,29	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R23	Resistor,metal film,200Ω,1%,1/4W, Type RN1/4	0410 1221
R25	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
R26	Resistor,metal film,475Ω,1%,1/4W, Type RN1/4	0410 1257
R28,31	Resistor,metal film,100KΩ,1%,1/4W, Type RN1/4	0410 1480
R30,47	Resistor,metal film,100Ω,1%,1/4W, Type RN1/4	0410 1192
R32	Resistor, presence dependent upon model: RFL 97 FO INTX: Same as R28. RFL 97 FO INTX-1: Not used.	
RZ1	Resistor network,presence dependent upon model: RFL 97 FO INTX: Not used. RFL 97 FO INTX-1: Nine 1KΩ 2% resistors,1.1W total,10-pin SIP,Allen-Bradley 110A102 or equiv.	32349
	SEMICONDUCTORS	
CR1	Not used.	
CR2-5	Diode,silicon,1N914B or 1N4448	26482
DS1	Light-emitting diode,red,right-angle PC mount,extended length, Industrial Devices 5300H1 or equiv.	99294
DS2	Light-emitting diode,green,right-angle PC mount,Industrial Devices 5300H5 or equiv.	32567
Q1-4	Not used.	
Q5	Transistor,NPN,40V,TO-92 case,2N4401	42574

Table 13-1. Replaceable parts, RFL 9700 fiber optic transmitter modules - continued.

Circuit Symbol (Figs. 13-5 thru 13-8)	Description	Part Number
	SEMICONDUCTORS - continued.	
Q6	Transistor,NPN,TO-92 case,2N5551	39484
Q7	Transistor,N-channel JFET,VHF/UHF,TO-92 case,Siliconix J309 or equiv.	32531
U1,18	MOS dual D-type flip-flop w/preset and clear,14-pin DIP, National Semiconductor MM74HC74N or equiv.	0615 166
U2,5	MOS dual J-K flip-flop,14-pin DIP,National Semiconductor MM74HC107N	0615 153
U3,4,8	Not used.	
U6,9,10,12	MOS quad 2-input NAND gate,14-pin DIP,National Semiconductor MM74HC00N	0615 159
U7,11	MOS hex inverter,unbuffered,high-speed,14-pin DIP,RCA CD74HCU04E or equiv.	0615 304
U13	MOS dual 4-bit binary counter,14-pin DIP,National Semiconductor MM74HC393N or equiv.	0615 192
U14	MOS quad differential line driver,16-pin DIP,National Semiconductor DS34C87N or equiv.	0615 395
U15	MOS quad differential line receiver,16-pin DIP,National Semiconductor DS34C86N or equiv.	0615 394
U16	MOS triple 3-input NAND gate,14-pin DIP,National Semiconductor MM74HC10N	0615 162
U17	MOS 7-stage binary counter,14-pin DIP,National Semiconductor MM74HC4024N or equiv.	0615 186
U19	MOS quad 2-input OR gate,14-pin DIP,National Semiconductor MM74HC02N	0615 160
U20	Integrated circuit, presence dependent upon model: RFL 97 FO INTX: Not used. RFL 97 FO INTX-1: MOS 8-channel digital multiplexer,16-pin DIP, National Semiconductor MM74HC151N or equiv.	0615 286
U21	Integrated circuit, presence dependent upon model: RFL 97 FO INTX: Not used. RFL 97 FO INTX-1: Same as U14.	
U22	Integrated circuit, presence dependent upon model: RFL 97 FO INTX: Not used. RFL 97 FO INTX-1: Same as U15.	
	MISCELLANEOUS COMPONENTS	
L1	Inductor,rf,molded,100µH,10%,Gowanda 10/103 or equiv.	32505 1
Y1	Crystal,quartz,6.272 MHz	99122 2

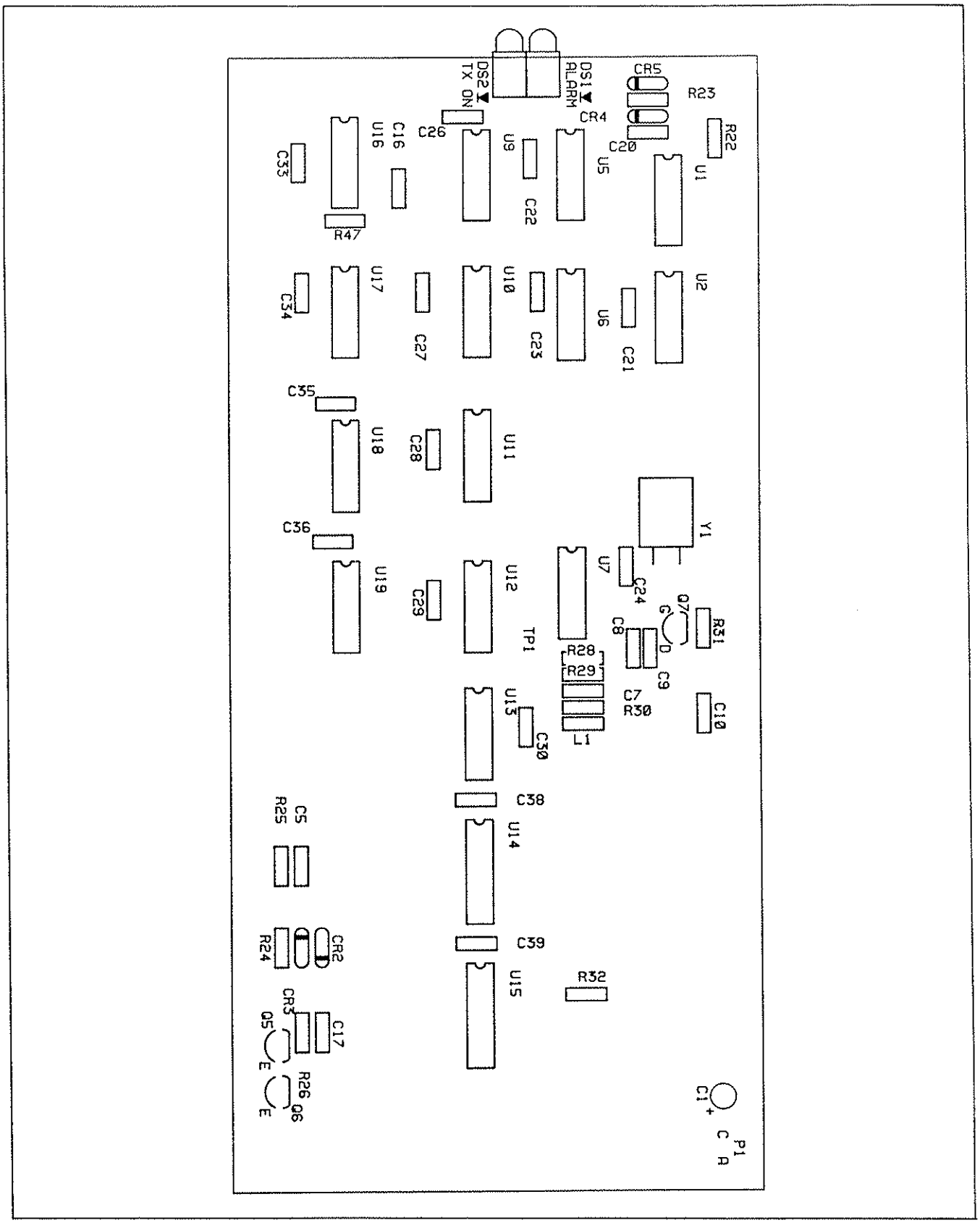


Figure 13-5. Component locator drawing, RFL 97 FO INTX Single-Input Fiber Optic Transmitter Module (Assembly No. 101530; Drawing No. D-101533, Rev. C)

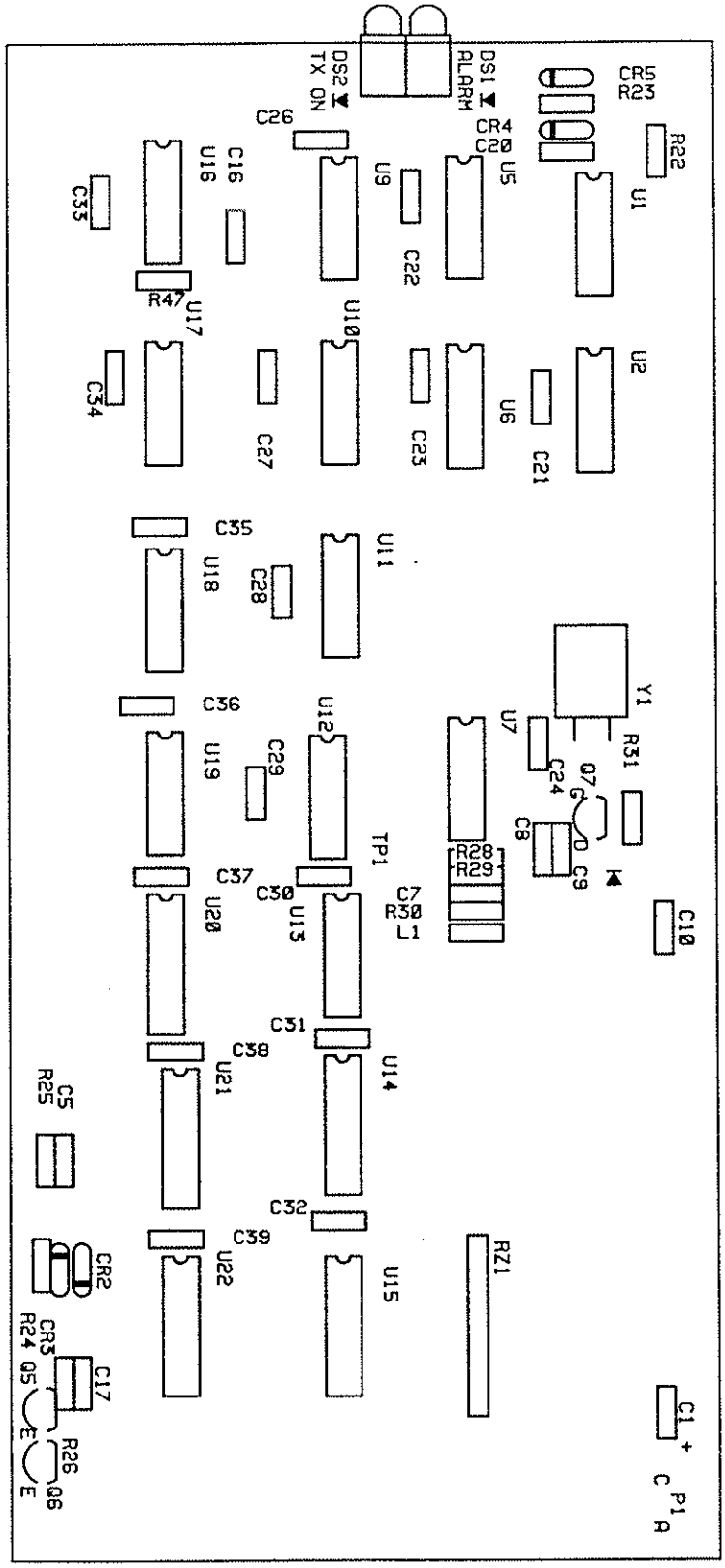


Figure 13-6. Component locator drawing, RFL 97 FO INTX-1 Eight-Input Fiber Optic Transmitter Module (Assembly No. 101535; Drawing No. D-101538, Rev. A)

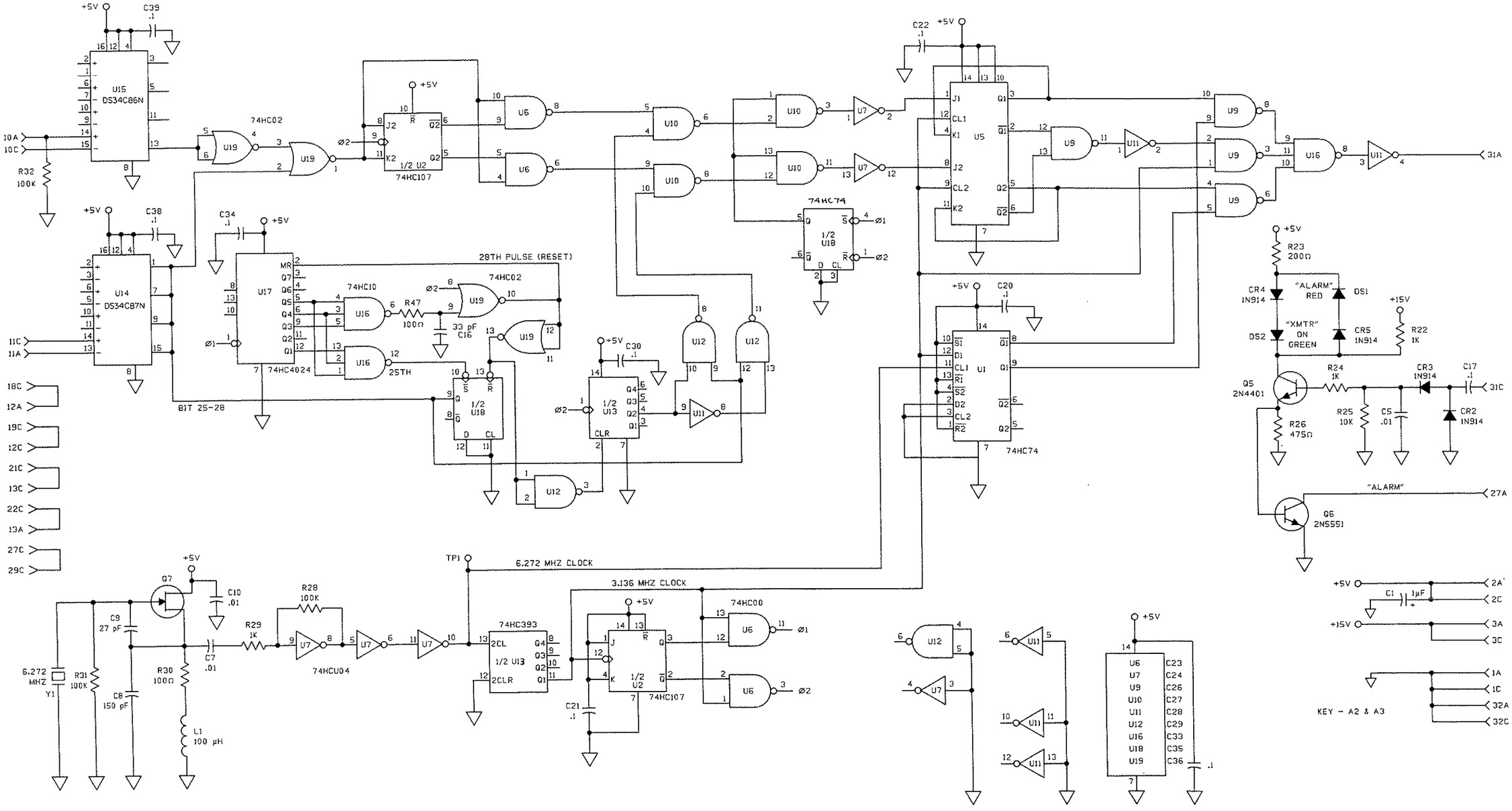


Figure 13-7. Schematic, RFL 97 FO INTX
Single-Input Fiber Optic Transmitter Module
(Assembly No. 101530; Schematic No. D-101534, Rev. C)

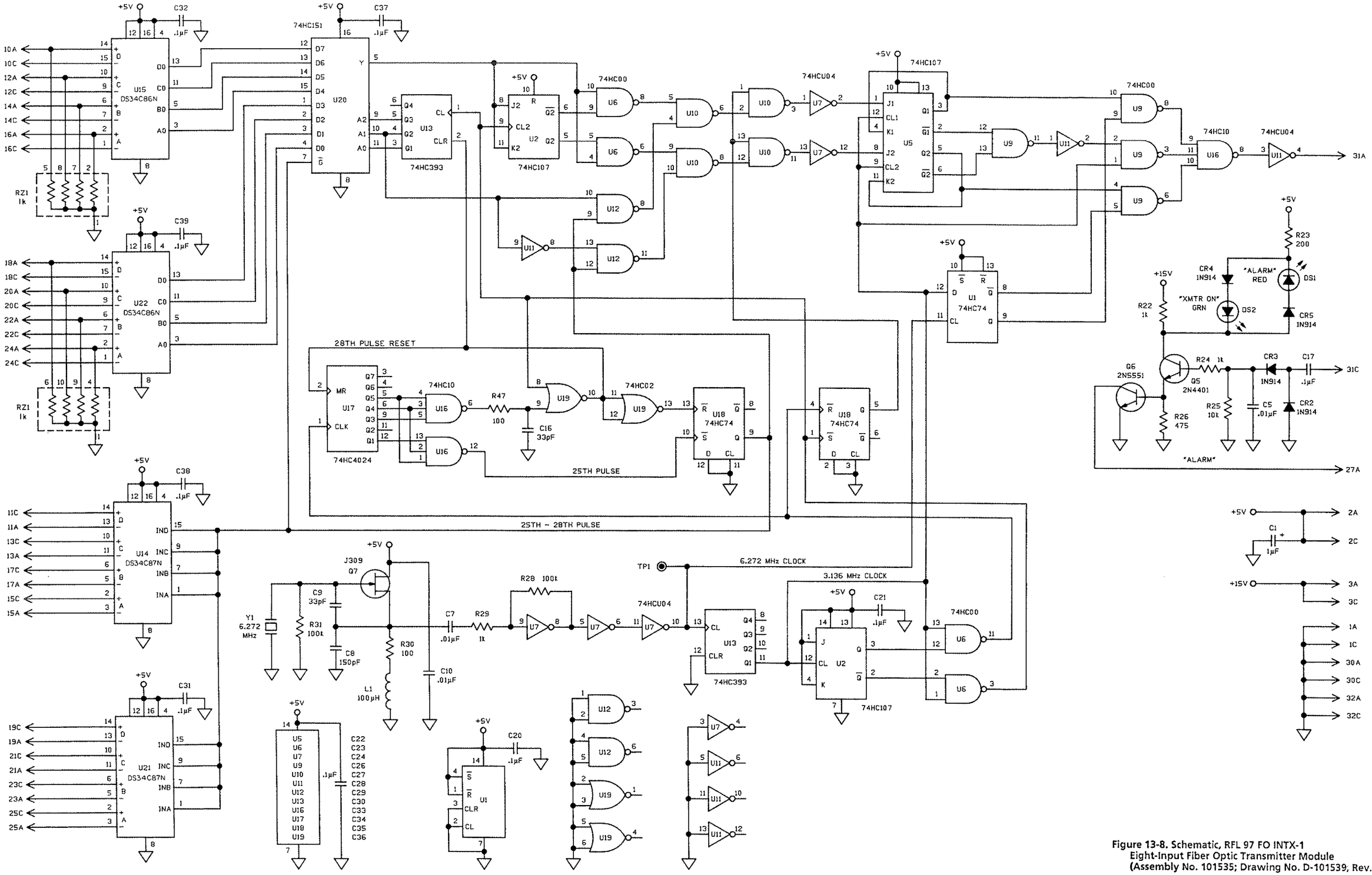


Figure 13-8. Schematic, RFL 97 FO INTX-1
Eight-Input Fiber Optic Transmitter Module
(Assembly No. 101535; Drawing No. D-101539, Rev. C)

Section 14. FIBER OPTIC RECEIVER MODULES

NOTE

The fiber optic detector head selected for use with the fiber optic receiver module will determine the interface characteristics, such as wavelength, input sensitivity, and mating connector type. Refer to Section 15 of this manual for further information on the fiber optic emitter heads.

14.1. DESCRIPTION

RFL 9700 fiber optic receiver modules accept inputs from fiber optic detector heads (Section 15) and convert them back into the RS-422 signals that can be processed by the RFL 97 DIG RX 56KB (Section 9). Two different fiber optic receiver modules are available: the RFL 97 FO INRX (Fig. 14-1) that produces a single RS-422 output at up to 56 Kbps, and the RFL 97 FO INRX-1 that contains demultiplexer circuits that can produce up to eight 56-Kbps channels.

Both fiber optic receiver modules are equipped with a relative signal strength indicator, along with a signal-to-noise (S/N) detector that can activate an alarm if signal is lost, or shut down a protective relaying unit to prevent false trips.

Each fiber optic receiver module occupies one dedicated module space in the RFL 97 CHAS chassis, and is used with a fiber optic detector head that is located at the rear of the chassis. All the currently-available fiber optic detector heads are described in Section 15 of this manual.

14.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to the RFL 97 FO INRX and the RFL 97 FO INRX-1, unless otherwise indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Frequency: 3.136 MHz ±40 ppm.

Modulation Method: Phase-shift keying (PSK), as produced by fiber optic detector head.

Input Amplitude: 20 to 30 mVp-p.

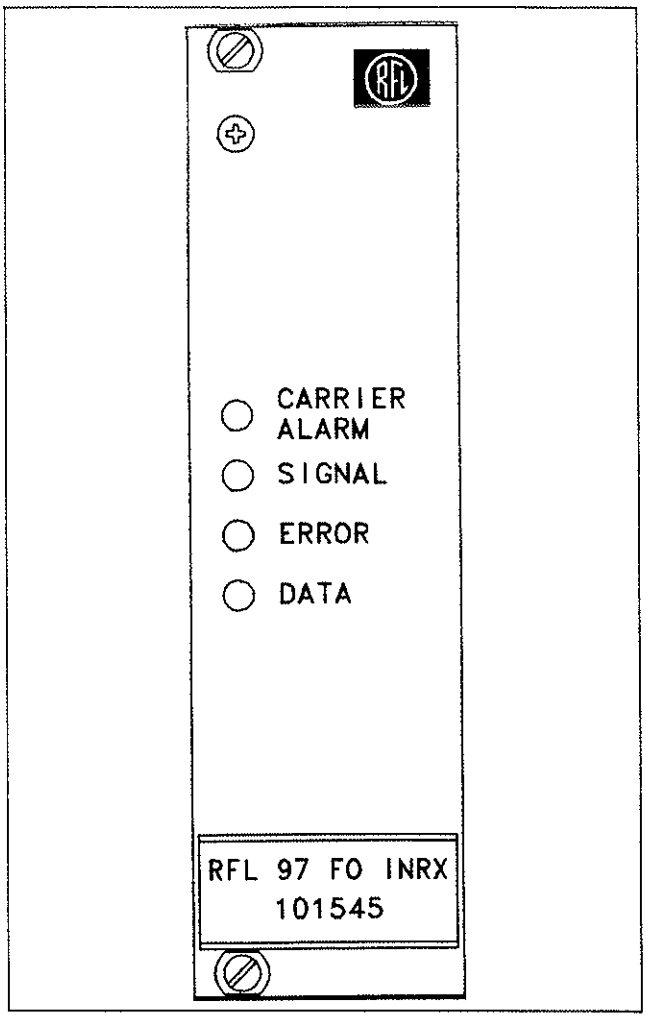


Figure 14-1. Typical RFL 9700 fiber optic receiver module

Output Signals:
- RFL 97 FO INRX: One RS-449 channel, passed to chassis backplane.
- RFL 97 FO INRX-1: Eight RS-449 channels; one passed to chassis backplane, the balance available for use by external equipment.

Maximum Data Rate: 56 Kbps, with a nominal amplitude of 5 Vp-p.

Front Panel Indicators:
- CARRIER ALARM: Red LED that lights when the incoming signal is lost.
- DATA: Green LED that lights when data is being decoded; this is the normal operation condition.

ERROR: Red LED that lights when an error has been detected.
SIGNAL: Green LED that lights when a valid input signal is being received.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements (from chassis supply):
+5-Volt Supply: 4.75 to 5.25 volts @ 150 mA.
+15-Volt Supply: 14.5 to 15.5 volts @ 50 mA.
-15-Volt Supply: 14.5 to 15.5 volts @ 50 mA.

Dimensions:
Panel Height: 5.1 inches (130 mm).
Panel Width: 1.4 inches (36 mm).
Depth (behind panel): 9.1 inches (231 mm).

14.3. THEORY OF OPERATION

The RFL 97 FO INRX module converts logic-level phase-shift keyed (PSK) signals it receives from the fiber optic detector head into output signals that conform with EIA Standard RS-422. The RFL 97 FO INRX-1 contains demultiplexers that can produce up to eight separate output signals, corresponding to the signals that were multiplexed at the transmitting RFL 9700. A block diagram of both fiber optic receiver modules appears in Figure 14-2. Figure 14-3 is a timing diagram for the RFL 97 FO INRX, and Figure 14-4 is a timing diagram for the RFL 97 FO INRX-1.

a. Preamplifier. The incoming signal at edge connector pin P1-A31 is passed through a preamplifier formed from four inverters in U22. This produces a 5-volt square wave, which can be monitored at test point TP5.

b. Demodulator. The output of the preamplifier is fed to U10-13. U10 is an Exclusive-OR gate, which serves as a phase demodulator. It accepts this signal as well as the re-constructed 3.136-MHz signal produced by the phase-locked loop. Compared to the system clock, the demodulator output will decrease for an increasing change in phase. The output of the demodulator (U10-11) is fed to the low-pass filter.

c. Phase-Locked Loop. The output of the phase detector is used in a phase-locked loop to control the system clock. The output of the phase demodulator is compared to a 2.5-volt reference. Any change in the phase angle will cause a voltage to be applied to the clock oscillator circuit, formed from crystal Y1, field-effect transistor Q3, and their associated components. The oscillator will react to the voltage to bring the 6.272-MHz clock signal back into phase. The output of this oscillator is amplified by being passed through three inverters in U6 to produce a logic-level signal. The signal at test point TP4 is phase-coherent and frequency-coherent at 6.272 MHz, and is locked onto and phase-related to the carrier at the transmitter.

Decade counter U5 divides the reconstructed carrier in half to produce a 3.136-MHz clock signal, which is offset by 90 degrees, and divided again to produce the 784-kHz clock signal.

d. Low-Pass Filter. The output of the phase demodulator is passed through a low-pass Bessel filter formed from capacitor C5, resistor R3, and inductors L1 through L5. This filter strips the carrier away, leaving the data and sync signal present at test point TP1.

e. Window Comparator And Sync Gate. The output of the low-pass filter (which can be monitored at test point TP1) is an average 1.25 volts; it will raise by 0.7 volts for a positive phase shift, and fall by 0.7 for a negative shift. Dual differential comparator U3 serves as a window comparator, converting this signal into two outputs that are fed into dual JK flip-flop U7. U7-9 and U7-12 are its clock inputs, which are driven by the 3.136-MHz clock signal. Potentiometer R4 is used to set the threshold voltage for these detectors.

f. Bit Clock Detector. The sync gate's outputs are fed to dual shift register U21, which is used to detect the bipolar violation code that serves as the synchronization clock for the 56-Kbps inputs and outputs. The bipolar violation code is received as two positive-going 90-degree phase excursions, followed by two negative-going excursions. When this code is received, counter U18 is reset. U18 will start up-counting, until it is reset by the next bipolar violation code; this re-creates the clock signal that was sent by the transmitter. This clock signal is sent from U18-5 to line driver U1, which converts it into an RS-422 signal.

g. Data Latch. The data portion of the received signal is combined by another Exclusive-OR gate in U10; its output (U10-3) is a baseband signal that contains only the data and the sync signal, not in digital form. The output of U10 is fed to octal latch U15. The strobe signals applied to U15-14 occur when the bipolar violation code is not being sent. If a data bit of one is sent, there will be 24 consecutive pulses at U10-3, and each one of these would be latched.

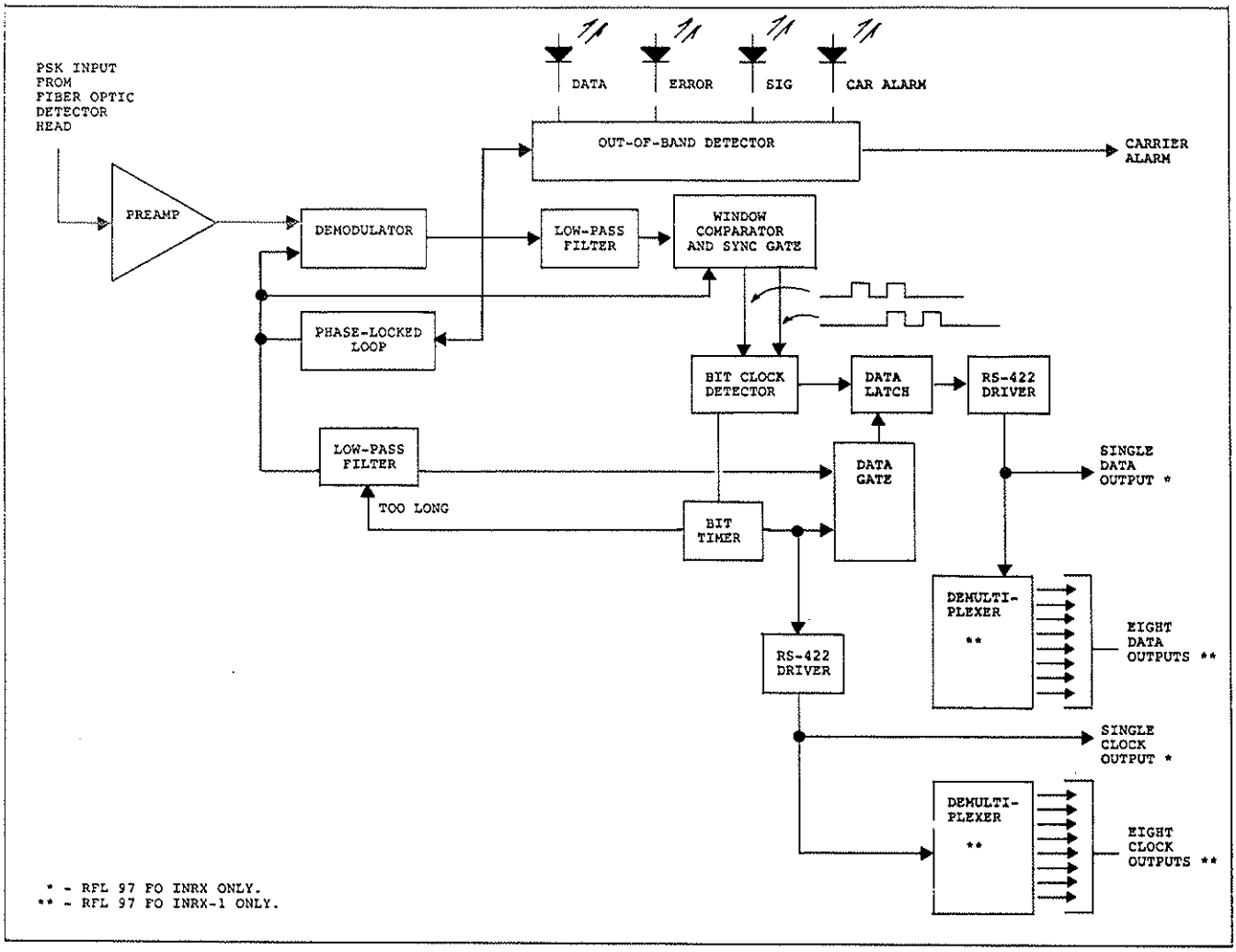


Figure 14-2. Block diagram, RFL 9700 fiber optic receiver modules

h. Out-Of-Band Detector. The phase-shift keying technique used in the RFL 9700 has characteristics that are similar to those experienced in FM radio. Incoming signals appear as a small amount of raspy noise followed by a clear signal; when the signal level falls below an acceptable minimum, it can disappear and re-appear several times. This is caused by a phenomenon called "capture."

In addition, the incoming signal must be between 1.5 MHz and 6.3 MHz before it can be accepted as a valid signal. Anything beyond these limits is considered noise. The out-of-band detector is used to monitor the output of the preamplifier; if the incoming signal is too weak or its frequency is beyond the limits established for the RFL 9700 system, alarm outputs will be produced. It also drives the front-panel LED indicators.

Decade counter U5 is clocked by the carrier pulses in the preamplifier output signal, and reset by the 784-kHz clock signal applied to U5-14. If eight carrier pulses are received from the preamplifier between pulses on the 784-kHz clock line, a NAND gate in U10 will change state, triggering monostable multivibrator U4. U4 will latch on, indicating that an error has occurred; this will light ERROR indicator DS3. Whenever DS3 is not lit, SIGNAL indicator DS2 will light, indicating that the incoming signal is within limits. If sixteen carrier pulses are received between clock pulses, CARRIER ALARM indicator DS1 will light.

i. Output Clock Signals. The 3.136-MHz system clock is divided by a binary counter in U9 to produce Phase 1 and Phase 2 clocks that are 180 degrees apart. Each has a period of 639 ns and a 75-percent duty cycle. A 56-kHz sync signal is produced by one of the NAND gates in U19 (obtained from U19-6). These signals are used to create the output timing signals, and the signals used to control the de-multiplexers on the RFL 97 FO INRX-1 module.

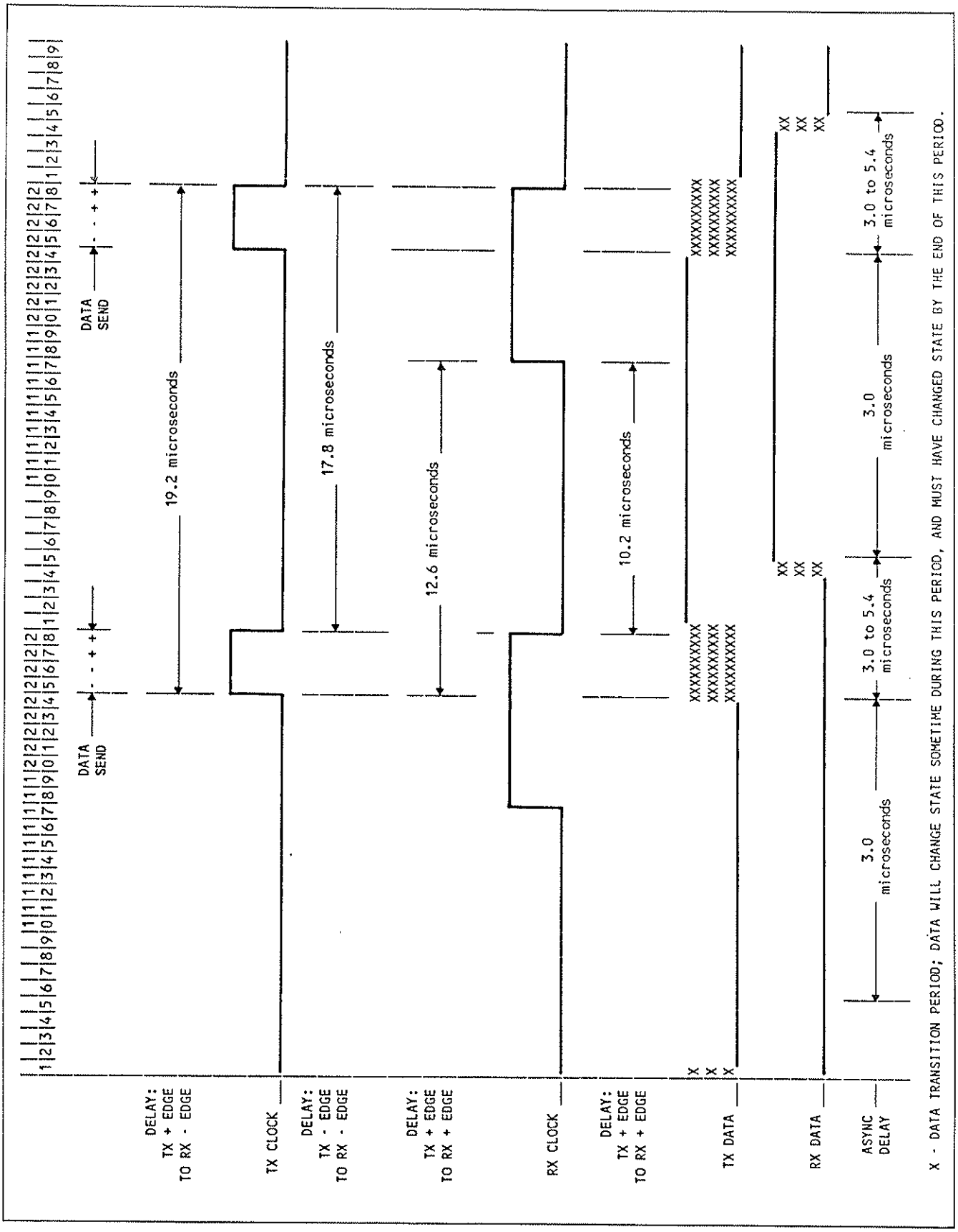


Figure 14-3. Timing diagram, RFL 97 FO INRX Single-Output Fiber Optic Receiver Module

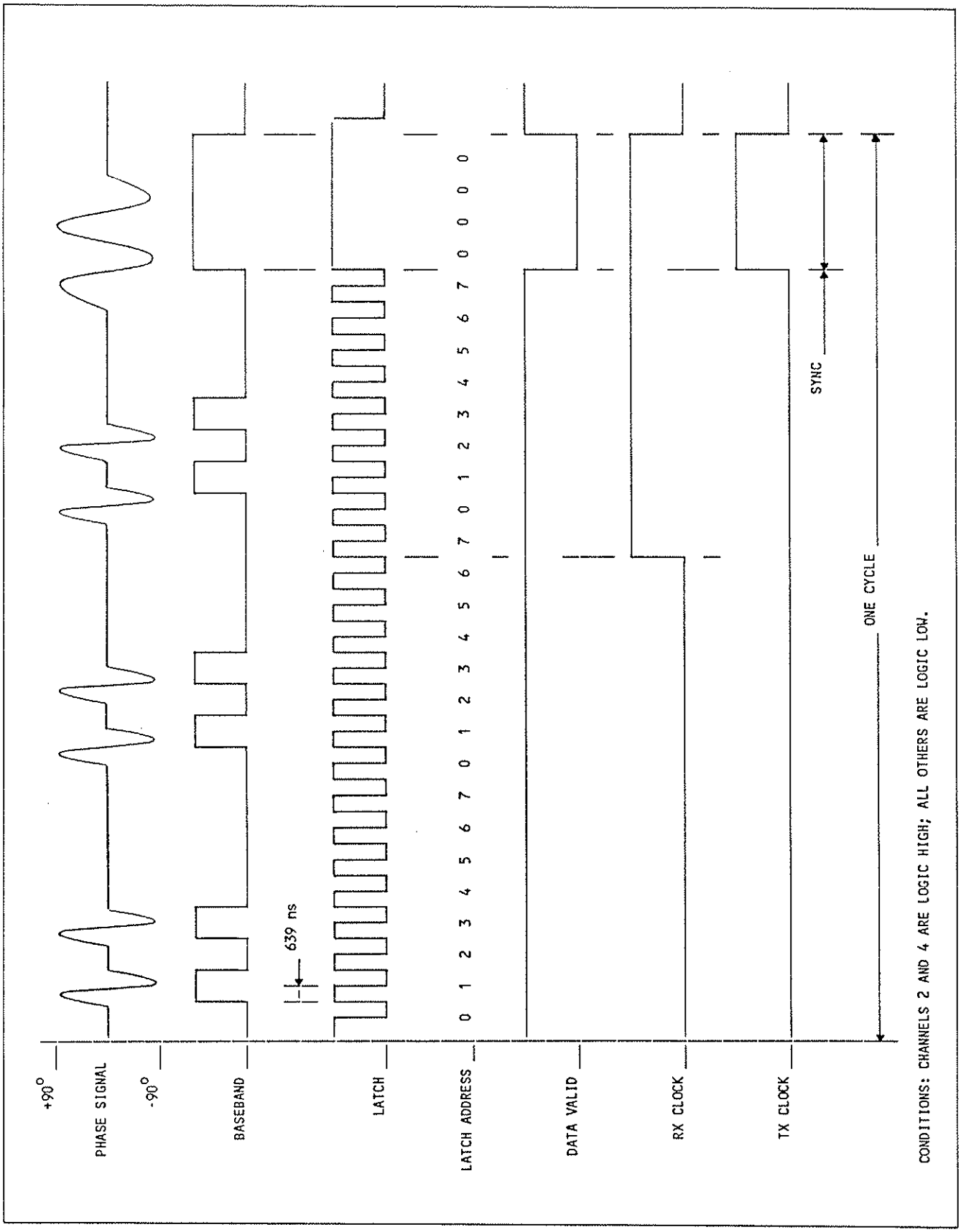


Figure 14-4. Timing diagram, RFL 97 FO INRX-1 Eight-Output Fiber Optic Receiver Module

The Phase 1 clock signal is fed into seven-stage counter U18, and the 56-kHz sync signal resets U18 after 28 bit cycles. If 88 clock pulses are received between sync pulses, an out-of-sync pulse is sent to U9 to reset Phase 1 and Phase 2. A latch signal is needed to latch the output data; it must pulse in time with the data, but not with the sync pulses. Bits 2, 3, and 4 of U19's output are inverted and combined to lock out the last four bits of each timing cycle, creating a DATA VALID signal. The DATA VALID signal is combined with the Phase 1 clock to allow for the correct output latching pulses.

j. Output Circuits (RFL 97 FO INRX Only). The Q7 output of octal latch U15 (U15-12) is fed to the D input of RS-422 line driver U11. Its D output becomes the module's data output signal.

The Q5 output from U18 (U18-5) drives the C input of RS-422 line drivers U11 (U11-9); this in turn becomes the module's clock output signal.

k. Demodulator/Output Circuits (RFL 97 FO INRX-1 Only). The Phase 2 clock, the baseband, and the latching signals are used to de-multiplex the data. 4-bit counter U9 is reset by the inverted DATA VALID signal and is clocked by the Phase 2 clock signal. The three low-ordered bits are used to address octal latch U15. The baseband provides the data and the latch signal releases the data from U15 at the proper time. U15 directly drives RS-422 line drivers U11 and U16; their outputs serve as the data outputs for all eight RS-422 output ports.

The Q5 output from U18 (U18-5) drives RS-422 line drivers U12 and U17; their outputs serve as clock outputs for all eight RS-422 output ports.

Table 14-1. Replaceable parts, RFL 9700 fiber optic receiver modules
RFL 97 FO INRX (Single-Output) - Assembly No. 101540
RFL 97 FO INRX-1 (Eight-Output) - Assembly No. 101545

Circuit Symbol (Figs. 14-5 thru 14-8)	Description	Part Number
	CAPACITORS	
C1-3	Capacitor,tantalum,1μF,tolerance and voltage rating dependent upon model: RFL 97 FO INRX: 10%,35V;Kemet T362A105K035AS or equiv. RFL 97 FO INRX-1: 20%,35V;Kemet T322B105M035AS or equiv.	 1007 1566 1007 496
C4,9,10,14,51	Capacitor,X7R ceramic,0.01μF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C5,16	Capacitor,Z5U ceramic,0.33μF,+80-20%,50V,Murata RPA3025U334Z50V or equiv.	0135 53348
C6	Capacitor,ceramic,82pF,5%,100V,AVX SA101A820JAA or equiv.	0125 18205
C7,13	Capacitor,ceramic,150pF,5%,100V,AVX SA101A151JAA or equiv.	0125 11515
C8	Capacitor,ceramic,22pF,5%,100V,AVX SA101A220JAA or equiv.	0125 12205
C11	Capacitor,ceramic,0.001μF,5%,100V,AVX SA201A102JAA or equiv.	0125 11205
C12	Capacitor,ceramic,220pF,5%,100V,AVX SA101A221JAA or equiv.	0125 12215
C15,17,22,24,25-35, 37,39,42-45	Capacitor,X7R ceramic,0.1μF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C18,20,21,23,47-49	Not used.	
C36,38,40,41	Capacitor, presence dependent upon model: RFL 97 FO INRX: Not used. RFL 97 FO INRX-1: Same as C17.	
C46,50	Capacitor,ceramic,100pF,5%,100V,AVX SA101A101JAA or equiv.	0125 11015

Table 14-1. Replaceable parts, RFL 9700 fiber optic receiver modules - continued.

Circuit Symbol (Figs. 14-5 thru 14-8)	Description	Part Number
	RESISTORS	
R1,3,5,10,11,23,26	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R2,27	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
R4	Resistor,variable,18-turn cermet,1KΩ,10%,1/2W,Beckman Helipot 68WR1K or equiv.	49995
R6,9	Resistor,metal film,2.37KΩ,1%,1/4W, Type RN1/4	0410 1324
R7,8	Resistor,metal film,64.9Ω,1%,1/4W, Type RN1/4	0410 1174
R12-16,30,31, 33-39,41-50,54	Not used.	
R17,21,51	Resistor,metal film,2.21KΩ,1%,1/4W, Type RN1/4	0410 1321
R19	Resistor,metal film,43.2Ω,1%,1/4W, Type RN1/4	0410 1445
R20	Resistor,metal film,2.05KΩ,1%,1/4W, Type RN1/4	0410 1318
R22	Resistor,metal film,20KΩ,1%,1/4W, Type RN1/4	0410 1413
R24,28,29,53	Resistor,metal film,100KΩ,1%,1/4W, Type RN1/4	0410 1480
R25,55	Resistor,metal film,100Ω,1%,1/4W, Type RN1/4	0410 1192
R32,40,52	Resistor,metal film,4.75KΩ,1%,1/4W, Type RN1/4	0410 1353
RZ1	Resistor network,five 220Ω 2% resistors,0.75W total,6-pin SIP, Bourns 4306R-101-221 or equiv.	99117
RZ2	Resistor network,seven 10KΩ 2% resistors,1.1W total,8-pin SIP, CTS of Berne 750-81-R10K or equiv.	47878
RZ3	Resistor network,four 4.7KΩ 2% resistors,1.1W total,8-pin SIP,CTS 750-83-R4.7K or equiv.	49458
	SEMICONDUCTORS	
CR1	Diode,varactor,26-32pF,Motorola MV209 or equiv.	32509
CR2	Diode,presence dependent upon model: RFL 97 FO INRX: Same as CR3. RFL 97 FO INRX-1: Not used.	
CR3	Diode,silicon,1N914B or 1N4448	26482
CR4	Diode,presence dependent upon model: RFL 97 FO INRX: Not used. RFL 97 FO INRX-1: Same as CR3.	
CR5	Diode,Zener,10V,5%,1W,1N4740A	33342
DS1,3	Light-emitting diode,red,right-angle PC mount,extended length, Industrial Devices 5300H1 or equiv.	99294
DS2,4	Light-emitting diode,green,right-angle PC mount,Industrial Devices 5300H5 or equiv.	32567
Q1,2	Not used.	
Q3	Transistor,N-channel JFET,VHF/UHF,TO-92 case,Siliconix J309 or equiv.	32531

Table 14-1. Replaceable parts, RFL 9700 fiber optic receiver modules - continued.

Circuit Symbol (Figs. 14-5 thru 14-8)	Description	Part Number
	SEMICONDUCTORS - continued.	
Q4-6,9,10	Transistor,NPN,plastic package,2N2222A	37445
Q7,8	Transistor,NPN,TO-92 case,2N5551	39484
U1,19	MOS triple 3-input NAND gate,14-pin DIP,National Semiconductor MM74HC10N or equiv.	0615 162
U2	Linear operational amplifier,JFET input,8-pin DIP,Texas Instruments TL081IP or equiv.	0620 228
U3	Linear dual differential comparator,14-pin DIP,Signetics LM219F or equiv.	0620 290
U4	Retriggerable monostable multivibrator,14-pin ceramic DIP,Texas Instruments SN54LS123J or equiv.	0610 147
U5	MOS dual 4-bit decade counter,16-pin DIP,National Semiconductor MM74HC390N or equiv.	0615 252
U6,13,22	MOS hex inverter,unbuffered,high-speed,14-pin DIP,RCA CD74HCU04E or equiv.	0615 304
U7	MOS dual J-K flip-flop,14-pin DIP,National Semiconductor MM74HC107N or equiv.	0615 153
U8	MOS quad 2-input NAND gate,14-pin DIP,National Semiconductor MM74HC00N or equiv.	0615 159
U9	MOS dual 4-bit binary counter,14-pin DIP,National Semiconductor MM74HC393N or equiv.	0615 192
U10	MOS quad 2-input Exclusive-OR gate,14-pin DIP, National Semiconductor MM74HC86N or equiv.	0615 268
U11	MOS quad differential line driver,16-pin DIP,National Semiconductor DS34C87N or equiv.	0615 395
U12,16,17	MOS quad differential line driver,presence dependent upon model: RFL 97 FO INRX: Not used. RFL 97 FO INRX-1: Same as U11.	
U14	MOS quad 2-input NAND gate,presence dependent upon model: RFL 97 FO INRX: Not used. RFL 97 FO INRX-1: Same as U8.	
U15	MOS 8-bit latch/3-to-8 line decoder,16-pin DIP, National Semiconductor MM74HC259N or equiv.	0615 288
U18	MOS 7-stage binary counter,14-pin DIP,National Semiconductor MM74HC4024N or equiv.	0615 186
U20	MOS dual 4-input NAND gate,14-pin DIP,National Semiconductor MM74HC20N or equiv.	0615 163
U21	MOS dual 4-stage static shift register,16-pin DIP,RCA CD74HC4015E or equiv.	0615 330
	MISCELLANEOUS COMPONENTS	
L1,3	Inductor,molded,33µH,10%,130mA,ferrite core,Jeffers Electronics Type 09 1326-1K or equiv.	32868
L2,7,8	Inductor,rf,molded,100µH,10%,Gowanda 10/103 or equiv.	32505 1
L4,5	Inductor,rf,molded,180µH,10%,Gowanda 10/183 or equiv.	32505 2
Y1	Crystal,quartz,6.272 MHz	99122 2

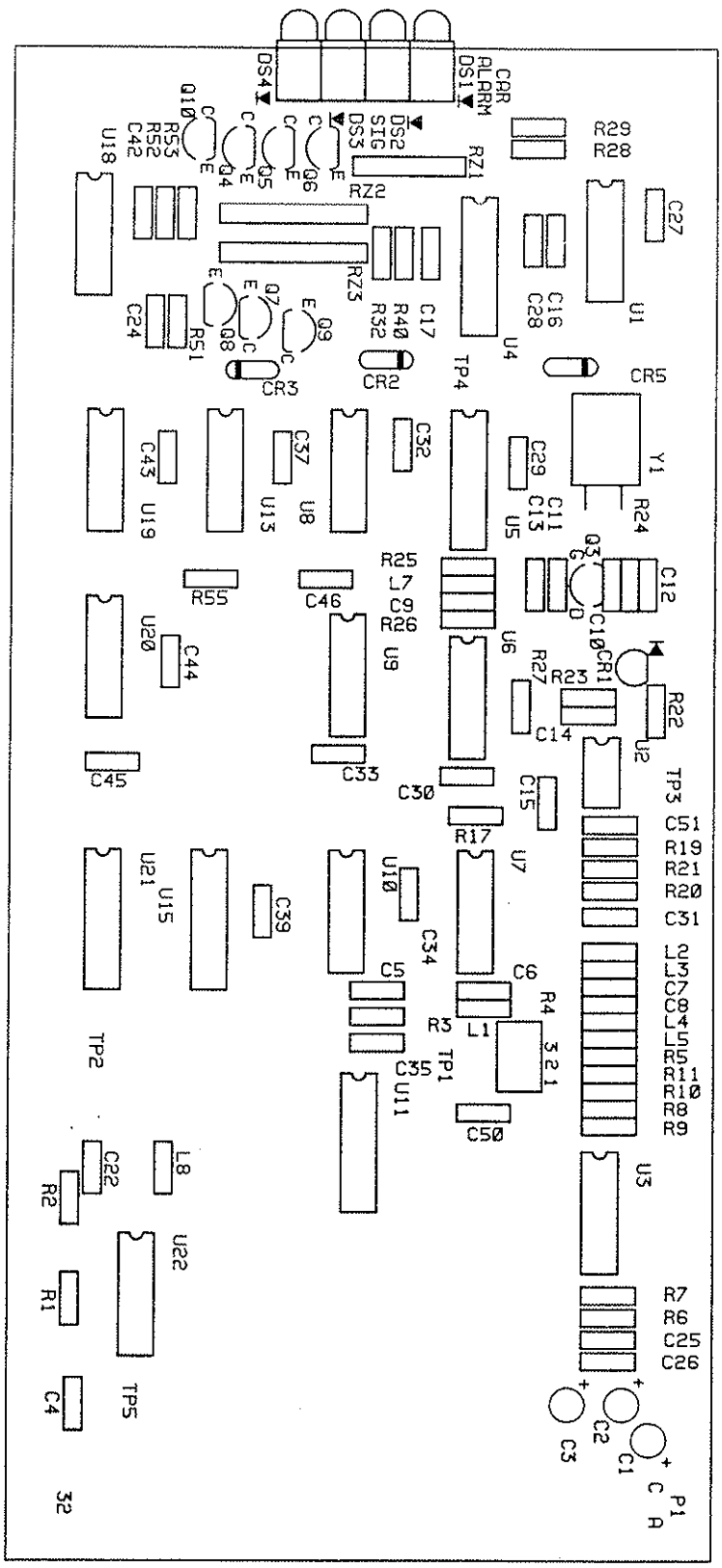


Figure 14-5. Component locator drawing, RFL 97 FO INRX Single-Output Fiber Optic Receiver Module (Assembly No. 101540; Drawing No. D-101543, Rev. D)

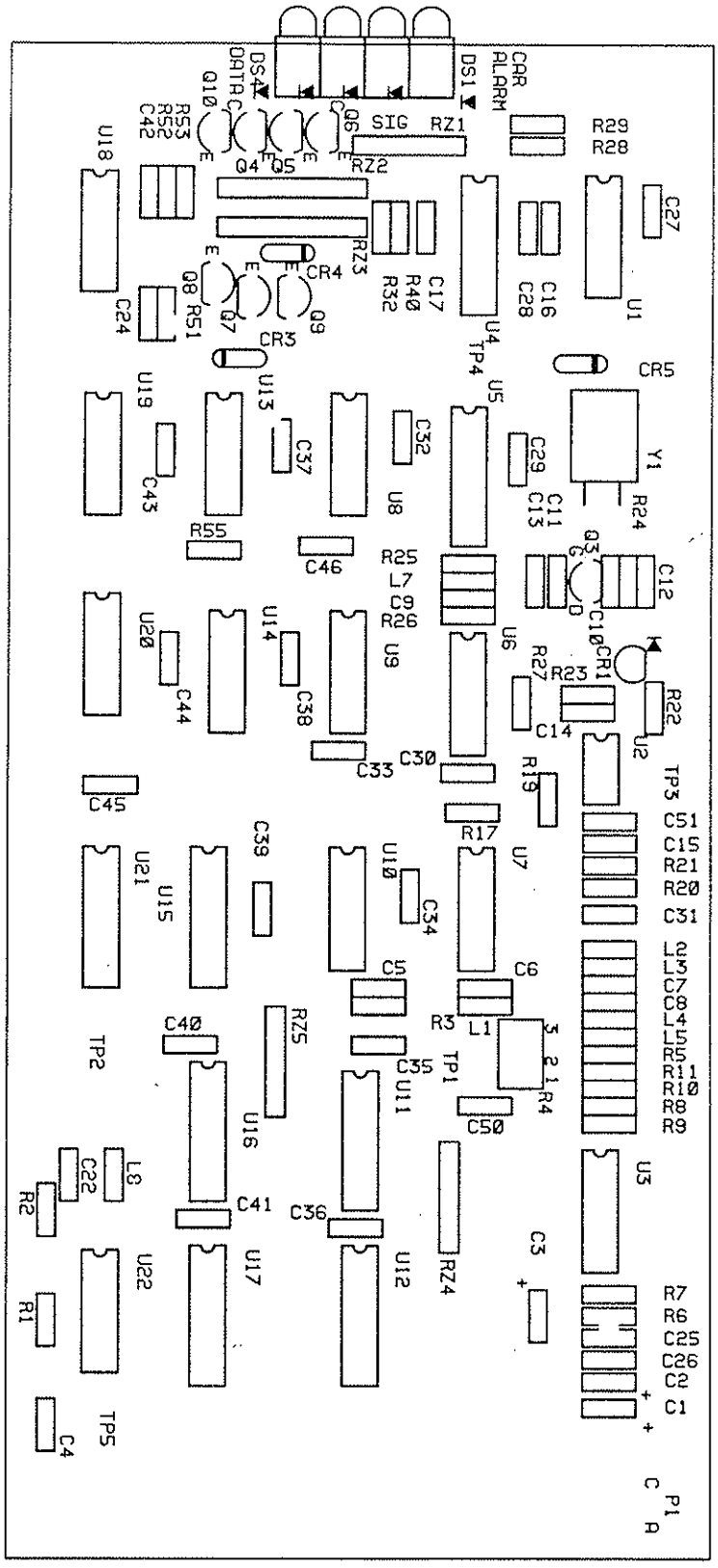


Figure 14-6. Component locator drawing, RFL 97 FO INRX-1 Eight-Output Fiber Optic Receiver Module (Assembly No. 101545; Drawing No. D-101548, Rev. E)

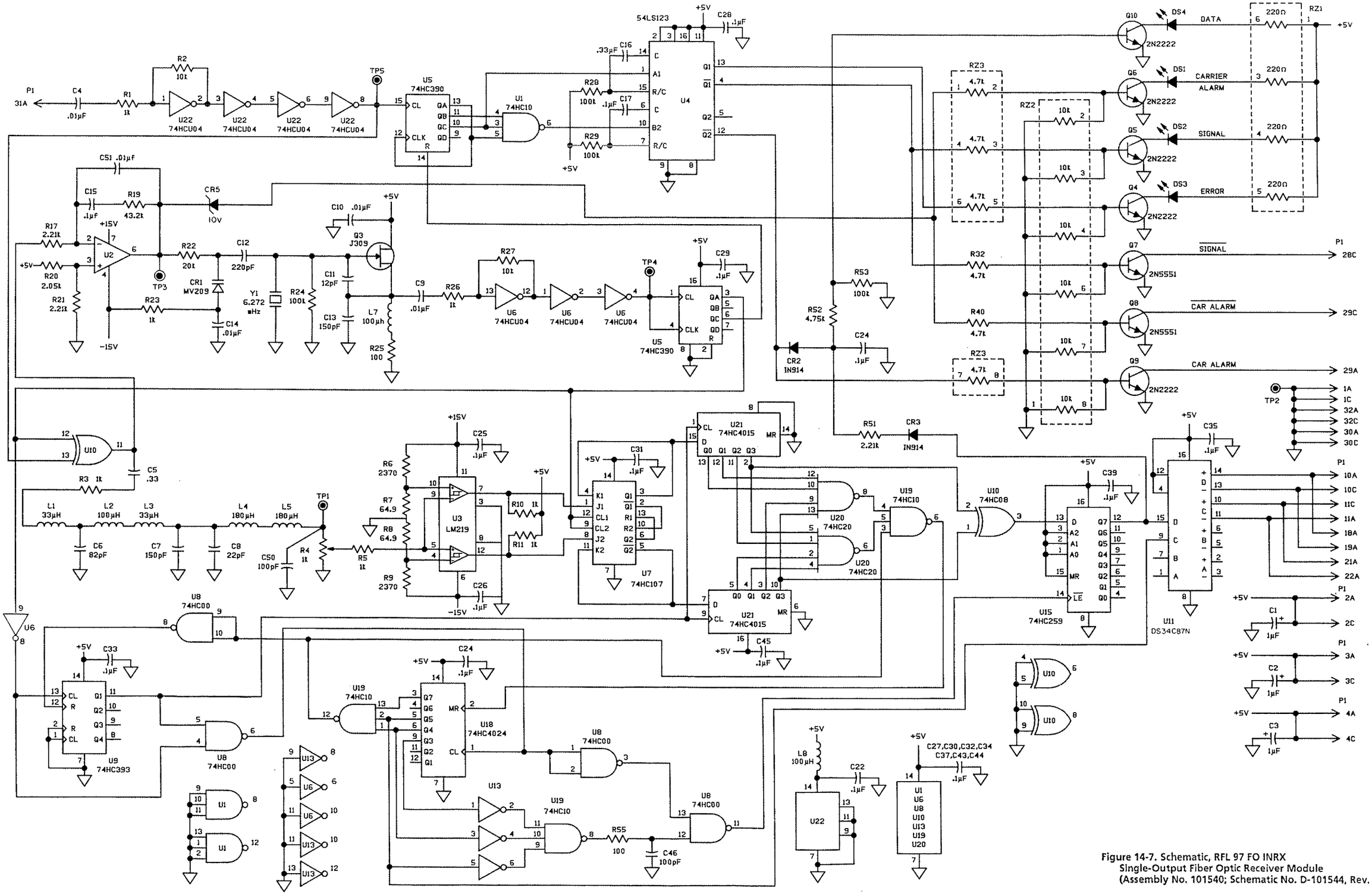


Figure 14-7. Schematic, RFL 97 FO INRX
Single-Output Fiber Optic Receiver Module
(Assembly No. 101540; Schematic No. D-101544, Rev. E)

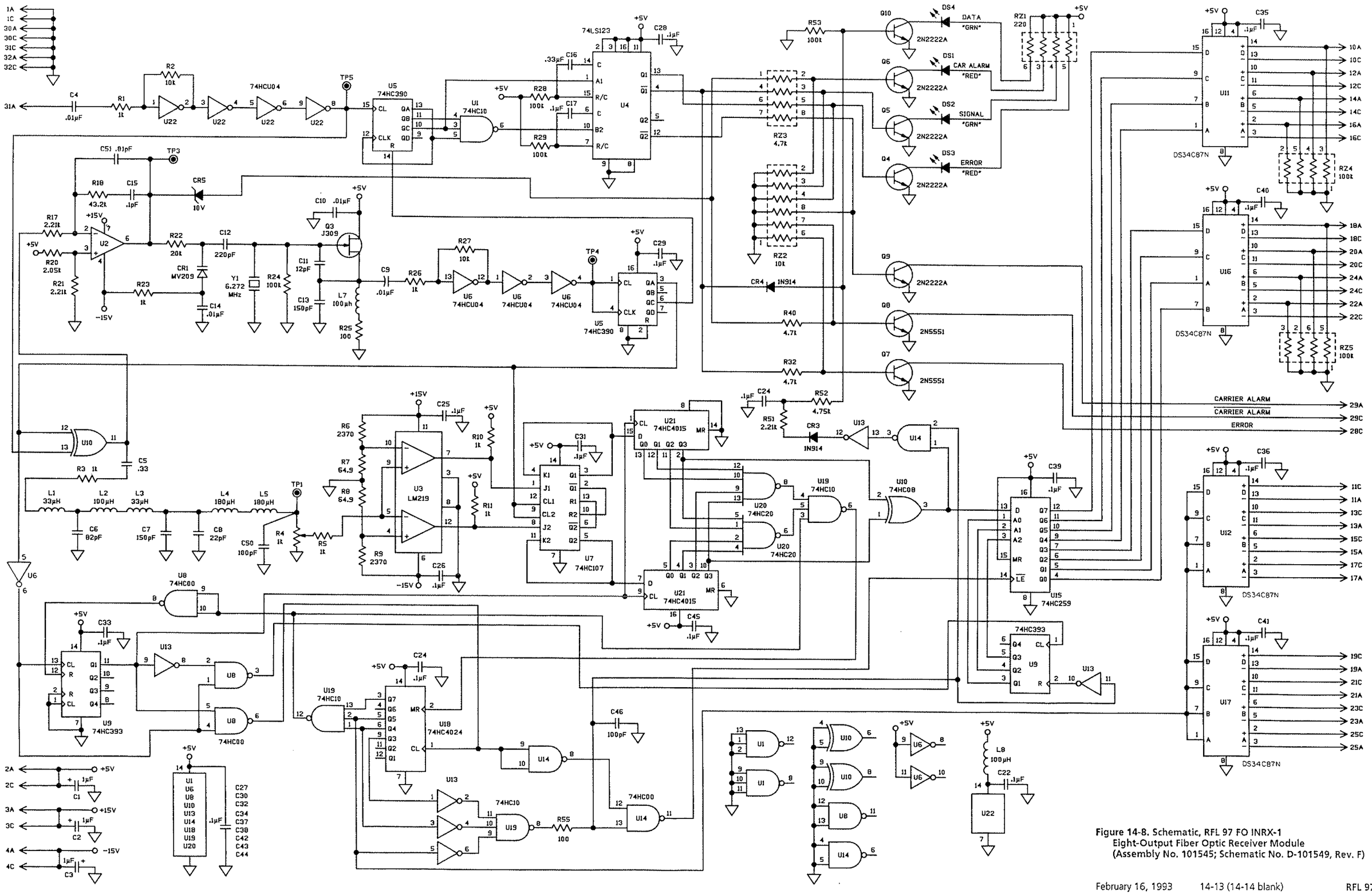


Figure 14-8. Schematic, RFL 97 FO INRX-1
Eight-Output Fiber Optic Receiver Module
(Assembly No. 101545; Schematic No. D-101549, Rev. F)

Section 15. FIBER OPTIC HEADS

15.1. INTRODUCTION

Each RFL 9700 fiber optic module uses a fiber optic head, which is mounted at the rear of the chassis. This allows the fiber optic modules to be removed from the chassis without having to draw the fiber through the chassis. A variety of heads are available, allowing the RFL 9700 to be used with many different types of fiber optic cables.

Table 15-1 summarizes the differences between the various fiber optic emitter heads and detector heads. RFL 9700 fiber optic emitter heads are described in paragraph 15.2 and its subordinates, starting on this page. Paragraph 15.3 and its subordinates starting on page 15-17 describe RFL 9700 fiber optic detector heads.

15.2. FIBER OPTIC EMITTER HEADS

15.2.1. Description

Fiber optic emitter heads serve as the interface between the fiber optic transmitter module (Section 13) and the fiber optic cable. They convert the signals produced by the fiber optic transmitter module into light energy, which is applied to the customer-supplied fiber optic cable. A typical fiber optic head is shown in Figure 15-1.

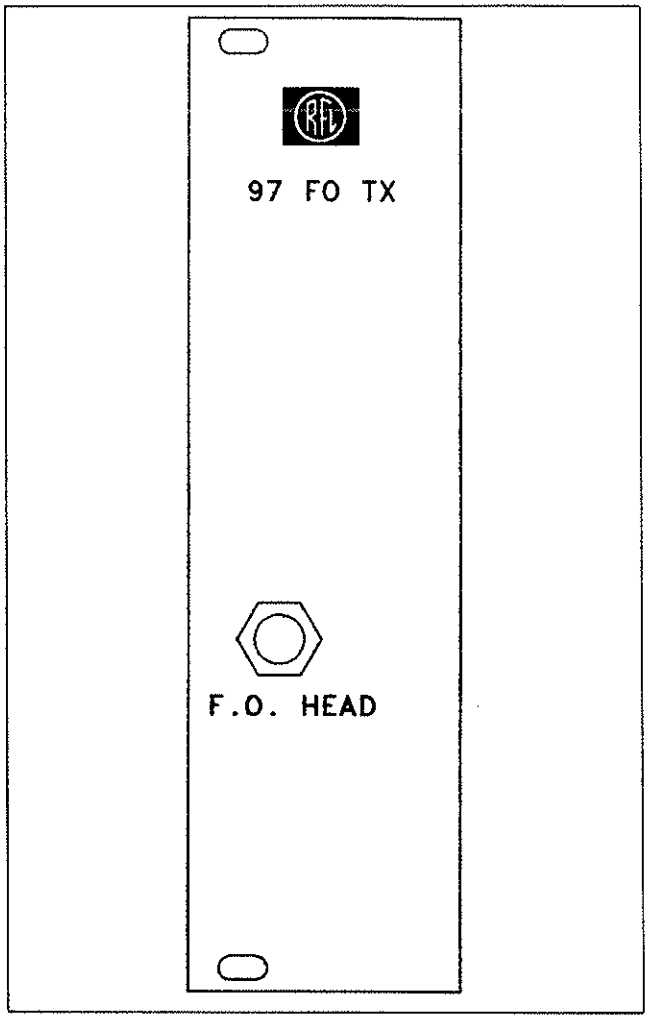


Figure 15-1. Typical fiber optic emitter head

15.2.2. Specifications

As of the date this manual was published, the following specifications apply to all fiber optic emitter heads used with RFL 9700 equipment, except where indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Drive Signals: TTL logic-level, generated by RFL 9700 fiber optic transmitter modules (Section 13).

Output Light Signal Characteristics: See Table 15-1.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F).
Operating: -30°C to +65°C (-22°F to +149°F).

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements (from chassis supply):
RFL 97 FO TX-8M:
+5-Volt Supply: 500 mA.
+15-Volt Supply: 50 mA.
-15-Volt Supply: 50 mA.
RFL 97 FO TX-13M And RFL 97 FO TX-13S:
+5-Volt Supply: 1.2A.
+15-Volt Supply: 30 mA.
-15-Volt Supply: 50 mA.
RFL 97 FO TX-13LS:
+5-Volt Supply: 150 mA.
+15-Volt Supply: 50 mA.
-15-Volt Supply: 50 mA.

Table 15-1. Differences between RFL 9700 fiber optic emitter and detector heads

Model Number	Assembly Number	Type	Wavelength/Mode	Connector	Peak Light Level *	Average Light Level *
RFL 97 FO TX-8M	102435	LED Emitter	850-nm Multimode	Amphenol 906	-18 dBm	-21 dBm
RFL 97 FO TX-13M	102440	LED Emitter	1300-nm Multimode	Amphenol 906	-13 dBm	-16 dBm
RFL 97 FO TX-13S	102445	LED Emitter	1300-nm Singlemode	ST	-27 dBm	-30 dBm
RFL 97 FO TX-13LS	101505	Laser Emitter	1300-nm Singlemode	ST	-7 dBm	-10 dBm
RFL 97 FO RX-8M	101515	Detector	850-nm Multimode	Amphenol 906	-48 dBm	-51 dBm
RFL 97 FO RX-13M	101520-1	Detector	1300-nm Multimode	Amphenol 906	-48 dBm	-51 dBm
RFL 97 FO RX-13/15S	101520-2	Detector	1300-nm Singlemode	ST	-48 dBm	-51 dBm

* Light levels are outputs for fiber optic emitter heads, and inputs for fiber optic detector heads. -30 dBm is the maximum permissible light level input for 1300-nm detector heads. If the incoming light level is greater than -30 dBm, attenuation must be added.

Dimensions:

Width (including panel): 1.4 inches (3.6 cm)
Height (including panel): 5 inches (12.7 cm)
Depth (behind panel): 3.3 inches (8.4 cm)

15.2.3. Theory Of Operation

Fiber optic emitter heads accept the amplitude-modulated signal produced by the fiber optic transmitter module and convert it into a modulated light signal, suitable for transmission over an optic fiber. Although they perform the same function, each operates in a slightly different manner, so theories or operation are provided for all emitter heads in paragraphs 15.2.3.1 through 15.2.3.3.

15.2.3.1. RFL 97 FO TX-8M 850-nm Multimode Fiber Optic Emitter Head

The RFL 97 FO TX-8M uses an LED light source to produce 850-nm light signals which are transmitted over multimode fiber optic cables. A block diagram of the RFL 97 FO TX-8M appears in Figure 15-2.

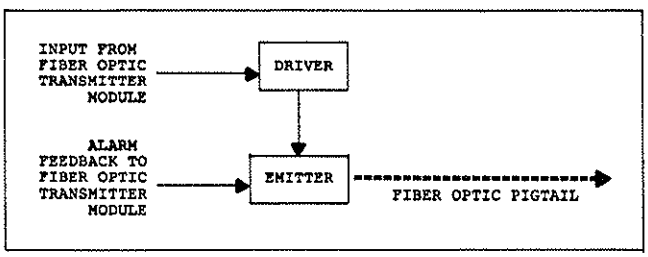


Figure 15-2. Block diagram, RFL 97 FO TX-8M 850-nm fiber optic LED emitter head

The RFL 97 FO TX-8M converts logic-level pulses into 850-nm light energy pulses for transmission over a multimode fiber optic cable. The light emitter is U102, a GaAlAs light-emitting diode with a graded index fiber optic pigtail permanently attached to it. The current through the LED is limited to 100 mA. This helps prolong the LED's life.

The input signal is used to control transistors Q101 and Q102. These transistors modulate the current through the LED, producing a modulated light signal. The peak light energy level injected into the fiber is -18 dBm.

The current through resistor R105 creates a voltage at U101-6. This voltage is compared to the reference voltage at U101-9; the difference between these two voltages causes a current limiting effect through U101-5. After going through Q101, the input signal causes a voltage through edge connector terminal 2C. This feedback signal is used to detect that the head is in place and operating. Test point TP101 provides a measuring point for the current passing through the LED.

15.2.3.2. RFL 97 FO TX-13M And RFL 97 FO TX-13S 1300-nm Fiber Optic Emitter Heads

The RFL 97 FO TX-13M uses an LED light source to produce multimode light signals which are transmitted over fiber optic cables. The RFL 97 FO TX-13S performs a similar function, but produces singlemode light signals. A block diagram for both of these fiber optic heads appears in Figure 15-3.

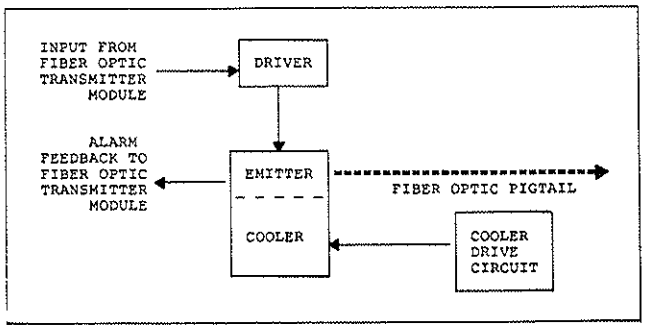


Figure 15-3. Block diagram, RFL 97 FO TX-13M and RFL 97 FO TX-13S 1300-nm fiber optic LED emitter heads

Logic-level pulses enter the fiber optic head at edge connector terminal 2A. These pulses are fed to a current amplifier formed from transistors Q101 and Q102, which supplies drive current to the LED inside fiber optic emitter U103. Resistor R105 and transistor array U101 limit the current peaks through the LED; it is rated for a maximum current of 150 mA, and normally operates near this limit.

A voltage is developed across R105 that is proportional to the current through the LED in U103. This voltage is compared to the reference voltage at U101-9. When the voltage at U101-6 exceeds the voltage at U101-9, current limiting is affected through U101-5. The voltage across resistor R106 is passed through resistor R108 to edge connector terminal 2A. This is the feedback signal the fiber optic transmitter module uses to determine whether the fiber optic emitter head is present and functioning properly.

Temperature variations inside U103 will result in a change in the light output. To compensate for this effect, the temperature of the LED in U103 is closely controlled by a thermistor inside U103. The thermistor is held at a constant resistance by a Peltier device, which functions as a combination heater/cooler. The thermistor and the Peltier device are driven by a circuit formed from operational amplifier U102, transistors Q104 through Q107, and their associated components. Diodes CR101 through CR104 form a bridge, which is balanced when the thermistor is at 10,000Ω. If the temperature inside U103 goes up, the thermistor's resistance drops; Q104 and Q105 will inject a current into U101-1, directing the Peltier device to cool U103. If the temperature inside U103 gets too low, the thermistor's resistance will increase. Q106 and Q107 will inject a current into U101-14; the Peltier device will then heat U103.

The current through the Peltier device is limited to about 1 ampere by transistor Q108. This holds the current to a safe level if the transmitter is turned on while U103 is hot or cold. This will result in a slower temperature variation that will not cause component damage.

15.2.3.3. RFL 97 FO TX-13LS 1300-nm Singlemode Laser Fiber Optic Emitter Head

The RFL 97 FO TX-13LS uses a laser light source to produce light signals which are transmitted over fiber optic cables. Figure 15-4 is a block diagram of the RFL 97 FO TX-13LS.

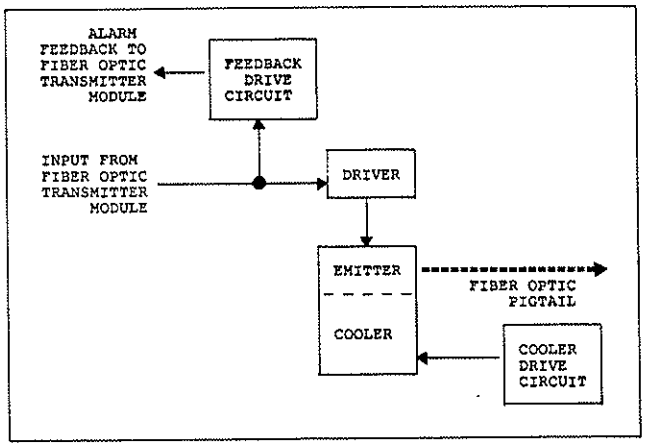


Figure 15-4. Block diagram, RFL 97 FO TX-13LS 1300-nm fiber optic laser emitter head

The modulated carrier signal produced by the fiber optic transmitter module (Section 13) is applied to edge connector terminal 2A, and drives a transistor connected to terminal 2C. This is used as an alarm feedback signal. The carrier is then put through a voltage divider, formed from resistors R107 and R108. This divider sets the amplitude of the modulation current. That signal is tied in parallel with the bias current signal produced by U101. The resultant signal drives the base of the current driving transistor for the light source.

a. Light Source. Unlike the other emitter heads that use light-emitting diodes as their light sources, the RFL 97 FO TX-13LS uses laser diode module U104, which contains a laser diode, a Peltier device, a thermistor, and a photodiode. These parts are housed in a hermetically-sealed 14-pin DIP package, with a permanently-attached fiber optic pigtail.

When the laser diode inside U104 is forward biased above its threshold current, it will emit light. The amount of light emitted will vary according to the amount of forward current passing through the laser diode and the setting of potentiometer R102. Current through the laser diode is limited to 90 mA.

The anode of the laser diode is connected to ground. Its cathode is fed by current driving transistor Q101, which is connected to the -11-volt rail through current sensing resistor R111. If the voltage across R111 is greater than the reference voltage produced by resistors R127 and R112, the input to the transistor that drives Q101 is pulled down. This acts as a current limiter to prevent damage to the laser diode.

b. Compensation. The laser diode must be compensated to counteract the effects of temperature, device aging, and normal variations in device performance. These effects are compensated for by the Peltier device and thermistor, and the photodiode.

The Peltier device works together with the thermistor to reduce the variations in light output caused by temperature changes. The thermistor's resistance changes as the temperature of U104's case goes up and down. The thermistor is part of a bridge circuit comprised of resistors R119, R120, and R121. The output voltage from this bridge circuit is used to make two comparisons. Half of dual comparator U102 uses the voltage to determine if the temperature is above or below the set point. U102's output is then used to either disable transistors Q107 and Q108 or transistors Q106 and Q109. This determines the polarity of the current flowing through the cooler. Q107 or Q109 control the magnitude of this current; these transistors receive their input from the other half of U102. Diodes CR102 through CR105 work together with the bridge circuit to supply U102 with a unipolar difference signal. The resulting output is an unsigned magnitude quantity, proportional to the difference in temperatures. Current flowing in one direction will cause the Peltier device to cool the laser diode; current in the opposite direction will cause the Peltier device to warm the laser diode. If the module is powered up at any temperature other than the set point, the Peltier device will have a large current draw. If it tries to draw more than 1.0 ampere, transistor Q110 is activated to limit the current. The limiting current value is set by potentiometer R126.

The photodiode monitors the laser diode's light output and compensates for the other factors. Because the photodiode is actually sampling the laser diode output, it provides very good feedback for adjusting the bias current. Its output is fed into integrating different operational amplifier U101. U101 compares the light level to a 2.5-volt reference to determine the proper bias current. U101's time constant is long enough to prevent the modulated signal from affecting its performance. Any factor that causes the laser diode's light output to drop will cause the photodiode current to also drop; this will result in an increase in laser diode bias current. If the light output increases, the current through the photodiode will also increase and the bias current will be decreased.

c. -11-Volt Supply. The -11-volt supply is generated from the -15-volt input to the RFL 97 FO TX-13LS. Zener diode CR101 and the junction drop of transistor Q103 produce the -11-volt reference. Capacitor C112 is made large enough to bring the supply up slowly.

Table 15-2. Replaceable parts, RFL 97 FO TX-8M 850-nm multimode fiber optic emitter head Assembly No. 102435

Circuit Symbol (Figs. 15-5 & 15-6)	Description	Part Number
C101	Capacitor,X7R ceramic,0.01μF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C102-104	Capacitor,X7R ceramic,0.1μF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C107	Capacitor,tantalum,22μF,20%,15V,Kemet T322D226M015AS or equiv.	1007 656
C108	Capacitor,ceramic,0.1μF,20%,50V,Centralab CZ20C104M or equiv.	1007 1574
C109	Capacitor,electrolytic,100μF,20%,50V,Nichicon ULB1H101M or equiv.	1007 1513
C111	Capacitor,tantalum,1μF,10%,35V,Kemet T110A105K035AS or equiv.	1007 1156
CR101	Diode,Zener,2.4V,5%,500mW,DO-7 case,1N5221B	40476
L101,102	Inductor,molded,33μH,10%,130mA,ferrite core,Jeffers Electronics Type 09 1326-1K or equiv.	32868
R101,102	Resistor,metal film,3.57KΩ,1%,1/4W, Type RN1/4	0410 1341
R103	Resistor,metal film,499Ω,1%,1/4W, Type RN1/4	0410 1259
R104	Resistor,metal film,4.99KΩ,1%,1/4W, Type RN1/4	0410 1355
R105	Resistor,metal film,12.1Ω,1%,1/2W,Type RN65D	1510 2109
R106,107	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R108	Resistor,metal film,249Ω,1%,1/4W, Type RN1/4	0410 1230
R109	Resistor,metal film,100Ω,1%,1/4W, Type RN1/4	0410 1192
R111	Resistor,metal film,3.01MΩ,1%,1/4W,Mepco/Electra SPR5053YD3M010F or equiv.	1510 1811
Q101,102	Transistor,NPN,TO-92 case,2N3903	21562
U101	Transistor array,five NPN transistors w/matched pair,14-pin ceramic DIP,RCA CA3045F or equiv.	0720 18
U102	Fiber optic emitter,LED,850-nm multimode w/SMA connector,Laser Diode IRE-160FB or equiv.	30437

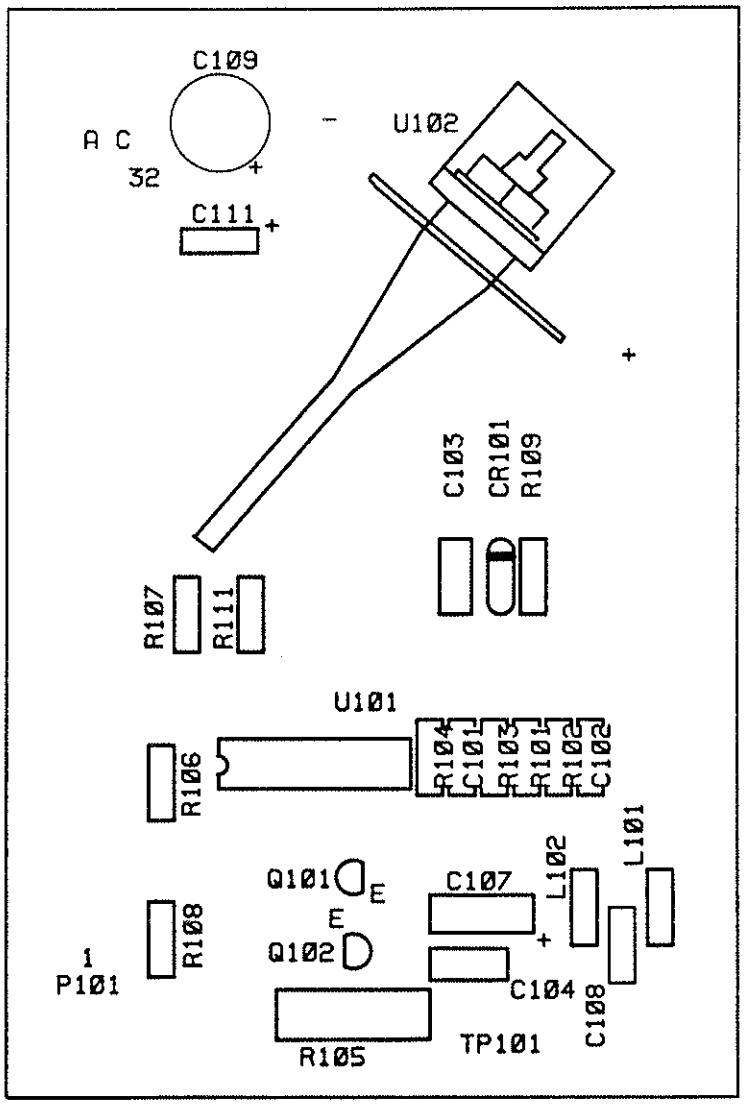


Figure 15-5. Component locator drawing, RFL 97 FO TX-8M 850-nm Multimode Fiber Optic Emitter Head (Assembly No. 102435; Drawing No. C-102438, Rev. A)

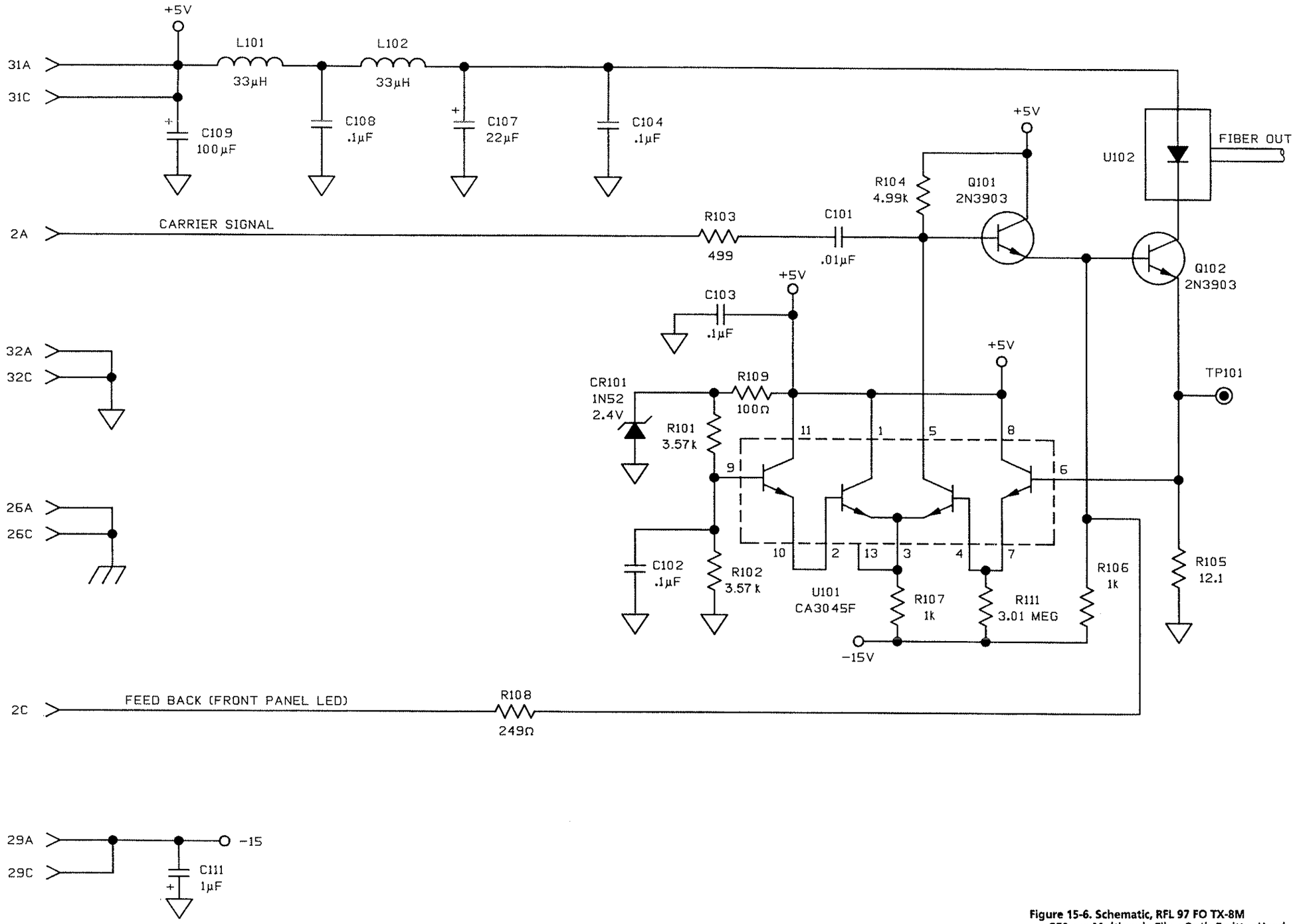


Figure 15-6. Schematic, RFL 97 FO TX-8M
850-nm Multimode Fiber Optic Emitter Head
(Assembly No. 102435; Schematic No. C-102439, Rev. A)

Table 15-3. Replaceable parts, 1300-nm LED fiber optic emitter heads
RFL 97 FO TX-13M (Multimode) - Assembly No. 102440
RFL 97 FO TX-13S (Singlemode) - Assembly No. 102445

Circuit Symbol (Figs. 15-7 & 15-8)	Description	Part Number
	CAPACITORS	
C101	Capacitor,X7R ceramic,0.01μF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C102-106	Capacitor,X7R ceramic,0.1μF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C107	Capacitor,tantalum,22μF,20%,15V,Kemet T322D226M015AS or equiv.	1007 656
C108	Capacitor,ceramic,0.1μF,20%,50V,Centralab CZ20C104M or equiv.	1007 1574
C109	Capacitor,electrolytic,100μF,20%,50V,Nichicon ULB1H101M or equiv.	1007 1513
C110,111	Capacitor,tantalum,1μF,20%,35V,Kemet T322B105M035AS or equiv.	1007 496
C112	Capacitor,Z5U ceramic,0.33μF,+80/-20%,50V,Murata RPA3025U334Z50V or equiv.	0135 53348
C113	Capacitor,ceramic,27pF,5%,100V,AVX SA101A270JAA or equiv.	0125 12705
	RESISTORS	
R101	Resistor,metal film,1.24KΩ,1%,1/4W, Type RN1/4	0410 1297
R102	Resistor,metal film,5.62KΩ,1%,1/4W, Type RN1/4	0410 1360
R103	Resistor,metal film,499Ω,1%,1/4W, Type RN1/4	0410 1259
R104	Resistor,metal film,4.99KΩ,1%,1/4W, Type RN1/4	0410 1355
R105	Resistor,metal film,12.1Ω,1%,1/2W,Type RN65D	1510 2109
R106,107	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R108	Resistor,metal film,249Ω,1%,1/4W, Type RN1/4	0410 1230
R109	Resistor,wirewound,0.75Ω,1%,1W,Dale RS-1A or equiv.	1780 671
R110	Resistor,metal film,1MΩ,1%,1/4W,Mepco/Electra SPR5053YD1M000F or equiv.	1510 1813
R111,114,118	Resistor,metal film,100KΩ,1%,1/4W, Type RN1/4	0410 1480
R113	Resistor,metal film,49.9KΩ,1%,1/4W, Type RN1/4	0410 1451
R115-117	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
R119	Resistor,metal film,100Ω,1%,1/4W, Type RN1/4	0410 1192
R120	Resistor,metal film,3.01MΩ,1%,1/4W,Mepco/Electra SPR5053YD3M010F or equiv.	1510 1811
RZ1,2	Resistor network,four 2KΩ 2% resistors,1W total,8-pin SIP,Bourns 4308R-102-202 or equiv.	32670
	SEMICONDUCTORS	
CR101-104	Diode,germanium,1N100A	28507
CR106-114	Diode,silicon,1N914B or 1N4448	26482
CR115	Diode,Zener,2.4V,5%,500mW,DO-7 case,1N5221B	40476
Q101,108-110	Transistor,NPN,TO-92 case,2N3903	21562
Q102	Transistor,NPN,TO-18 case,2N2222A	44178

Table 15-3. Replaceable parts, 1300-nm LED fiber optic emitter heads - continued.

Circuit Symbol (Figs. 15-7 & 15-8)	Description	Part Number
	SEMICONDUCTORS - continued.	
Q104-107	Transistor,NPN Darlington,plastic package,Texas Instruments TIP-120 or equiv.	40698
U101	Transistor array,five NPN transistors w/matched pair,14-pin ceramic DIP,RCA CA3045F or equiv.	0720 18
U102	Linear operational amplifier,JFET input,8-pin DIP,Texas Instruments TL082IP or equiv.	0620 227
U103	Fiber optic emitter,LED,1300-nm w/cooler; mode and connector type dependent upon model: RFL 97 FO TX-13M: Multimode w/SMA connector, Lasertron QLED1300MM-503 or equiv. RFL 97 FO TX-13S: Singlemode w/ST connector,Lasertron QLED1300SM-503 or equiv.	 30440 30433
	MISCELLANEOUS COMPONENTS	
L101,102	Inductor,molded,33µH,10%,130mA,ferrite core,Jeffers Electronics Type 09 1326-1K or equiv.	32868

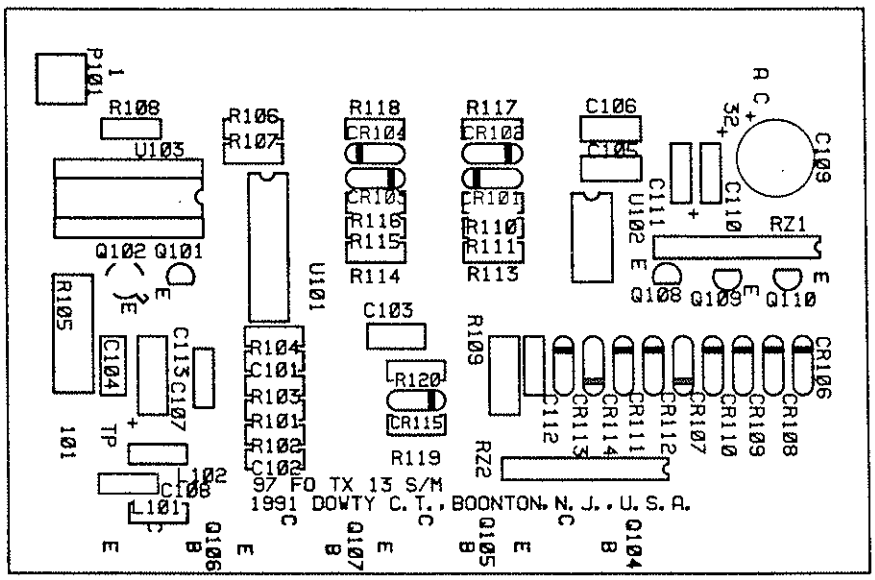


Figure 15-7. Component locator drawing, 1300-nm LED fiber optic emitter heads (Assembly Nos. 102440 and 102445; Drawing No. C-102448, Rev. D)

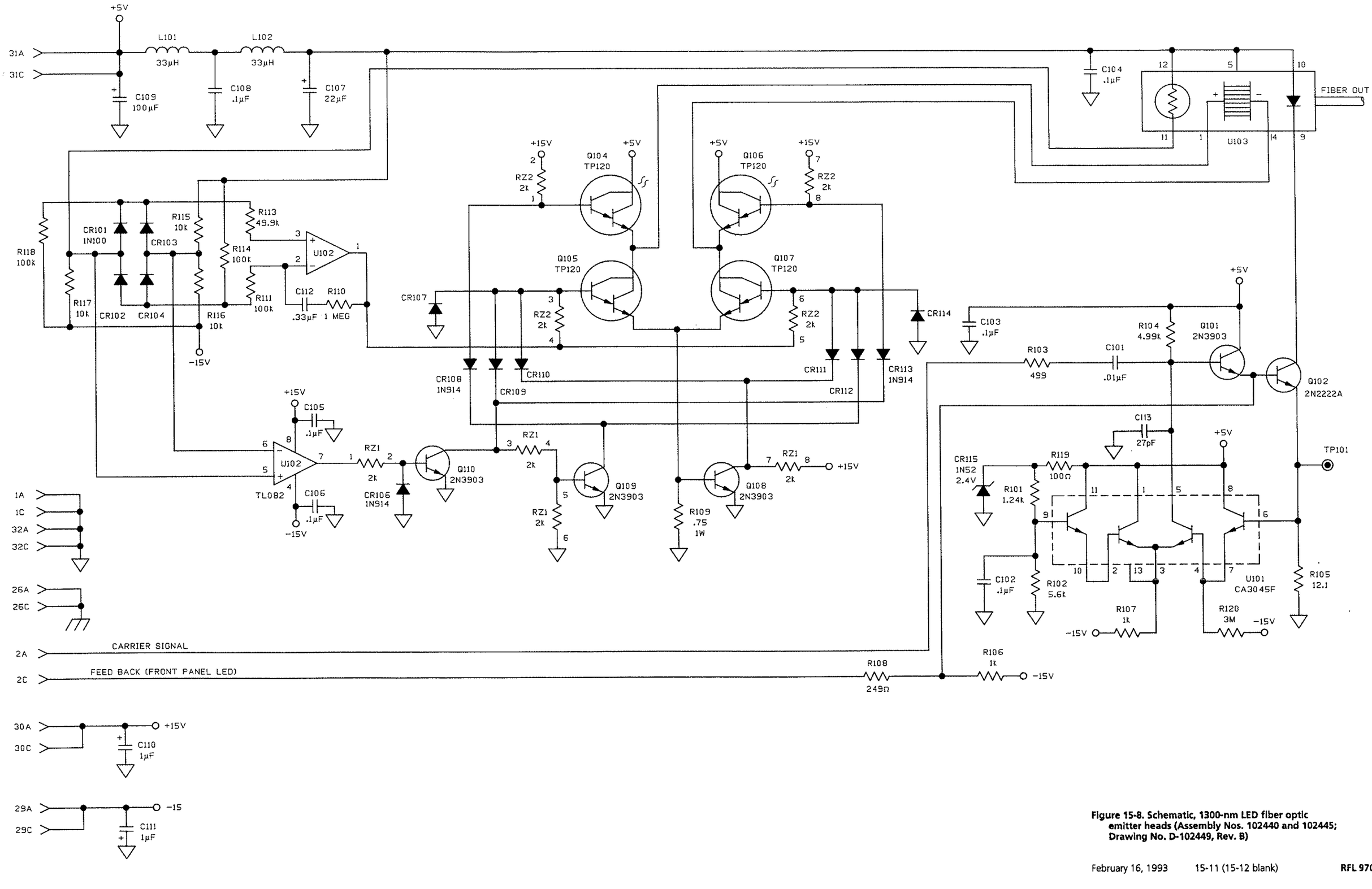


Figure 15-8. Schematic, 1300-nm LED fiber optic emitter heads (Assembly Nos. 102440 and 102445; Drawing No. D-102449, Rev. B)

Table 15-4. Replaceable parts, RFL 97 FO TX-13LS 1300-nm Singlemode Laser Fiber Optic Emitter Head Assembly No. 101505

Circuit Symbol (Figs. 15-9 & 15-10)	Description	Part Number
	CAPACITORS	
C101,112,113	Capacitor,electrolytic,100µF,20%,50V,Nichicon ULB1H101M or equiv.	1007 1513
C102,103	Capacitor,tantalum,1µF,20%,35V,Kemet T322B105M035AS or equiv.	1007 496
C104-111	Capacitor,X7R ceramic,0.1µF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C114	Capacitor,Z5U ceramic,0.33µF,+80/-20%,50V,Murata RPA3025U334Z50V or equiv.	0135 53348
	RESISTORS	
R101	Resistor,metal film,6.65KΩ,1%,1/4W, Type RN1/4	0410 1367
R102	Resistor,variable,12-turn cermet,50KΩ,10%,1/4W,top adjust,Bourns 3266W-1-503 or equiv.	32998
R103,104,118,122,123	Resistor,metal film,100KΩ,1%,1/4W, Type RN1/4	0410 1480
R105,107,110	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R106,119-121	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
R108,113	Resistor,metal film,499Ω,1%,1/4W, Type RN1/4	0410 1259
R109,112	Resistor,metal film,60.4Ω,1%,1/4W, Type RN1/4	0410 1171
R111	Resistor,metal film,10Ω,1%,1/8W,Type RN55D	1510 1092
R114	Resistor,metal film,4.99KΩ,1%,1/4W, Type RN1/4	0410 1355
R115	Resistor,metal film,475Ω,1%,1/4W, Type RN1/4	0410 1257
R116	Resistor,metal film,2.21KΩ,1%,1/4W, Type RN1/4	0410 1321
R117	Resistor,metal film,27.4Ω,1%,1/8W,Type RN55D	1510 1425
R124	Resistor,metal film,49.9KΩ,1%,1/4W, Type RN1/4	0410 1451
R125	Resistor,metal film,1MΩ,1%,1/4W,Type RN60D	1510 508
R126	Resistor,wirewound,0.75Ω,1%,1W,Dale RS-1A or equiv.	1780 671
R127	Resistor,metal film,681Ω,1%,1/4W, Type RN1/4	0410 1272
R128	Resistor,metal film,30.1KΩ,1%,1/4W, Type RN1/4	0410 1430
RZ1,2	Resistor network,four 2KΩ 2% resistors,1W total,8-pin SIP,Bourns 4308R-102-202 or equiv.	32670
	SEMICONDUCTORS	
CR101	Diode,Zener,10V,5%,1W,1N4740A	33342
CR102-105	Diode,germanium,1N100A	28507
CR106-115	Diode,silicon,1N914B or 1N4448	26482
Q101,104,105,110	Transistor,NPN,TO-92 case,2N3903	21562
Q102	Transistor,PNP,60V,1A,plastic case similar to TO-220,Texas Instruments TIP30A or equiv.	36996
Q103	Transistor,PNP,TO-92 case,2N3905	21564
Q106-109	Transistor,NPN Darlington,plastic package,Texas Instruments TIP-120 or equiv.	40698

Table 15-4. Replaceable parts, RFL 97 FO TX-13LS 1300-nm Singlemode Laser Fiber Optic Emitter Head - continued.

Circuit Symbol (Figs. 15-9 & 15-10)	Description	Part Number
	SEMICONDUCTORS - continued.	
U101	Linear operational amplifier,JFET input,8-pin DIP,Texas Instruments TL081IP or equiv.	0620 228
U102	Linear operational amplifier,JFET input,8-pin DIP,Texas Instruments TL082IP or equiv.	0620 227
U103	Transistor array,five NPN transistors w/matched pair,14-pin ceramic DIP,RCA CA3045F or equiv.	0720 18
U104	Fiber optic emitter,laser,1300-nm singlemode w/cooler and ST connector, Lasertron QLM3S855-052 or equiv.	30434
	MISCELLANEOUS COMPONENTS	
L101	Inductor,molded,390µH,5%,200mA,Stanwyck ESA-390 or equiv.	92267
L102,103	Inductor,molded,33µH,10%,130mA,ferrite core,Jeffers Electronics Type 09 1326-1K or equiv.	32868

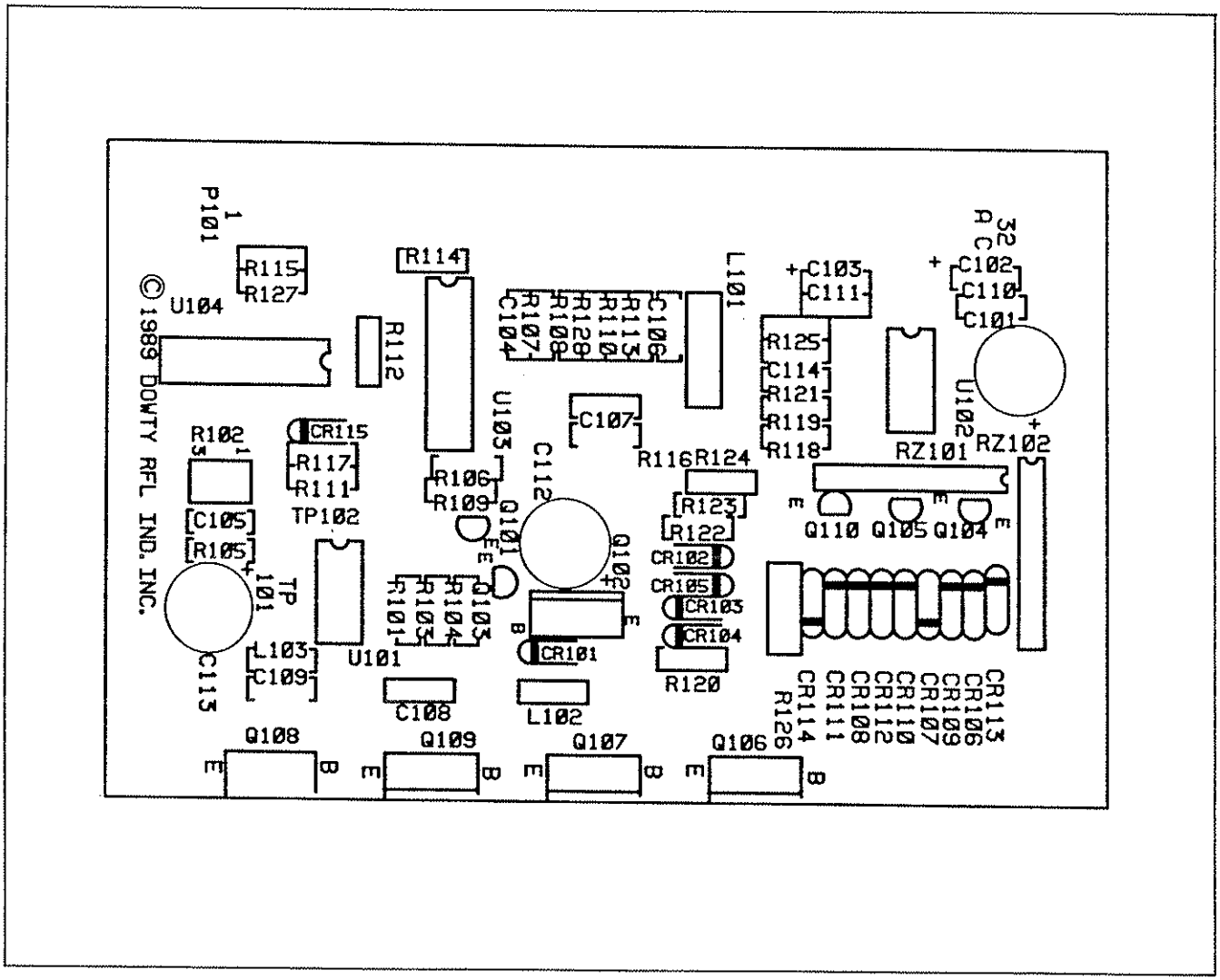


Figure 15-9. Component locator drawing, RFL 97 FO TX-13LS 1300-nm Singlemode Laser Fiber Optic Emitter Head (Assembly No. 101505; Drawing No. C-101508, Rev. B)

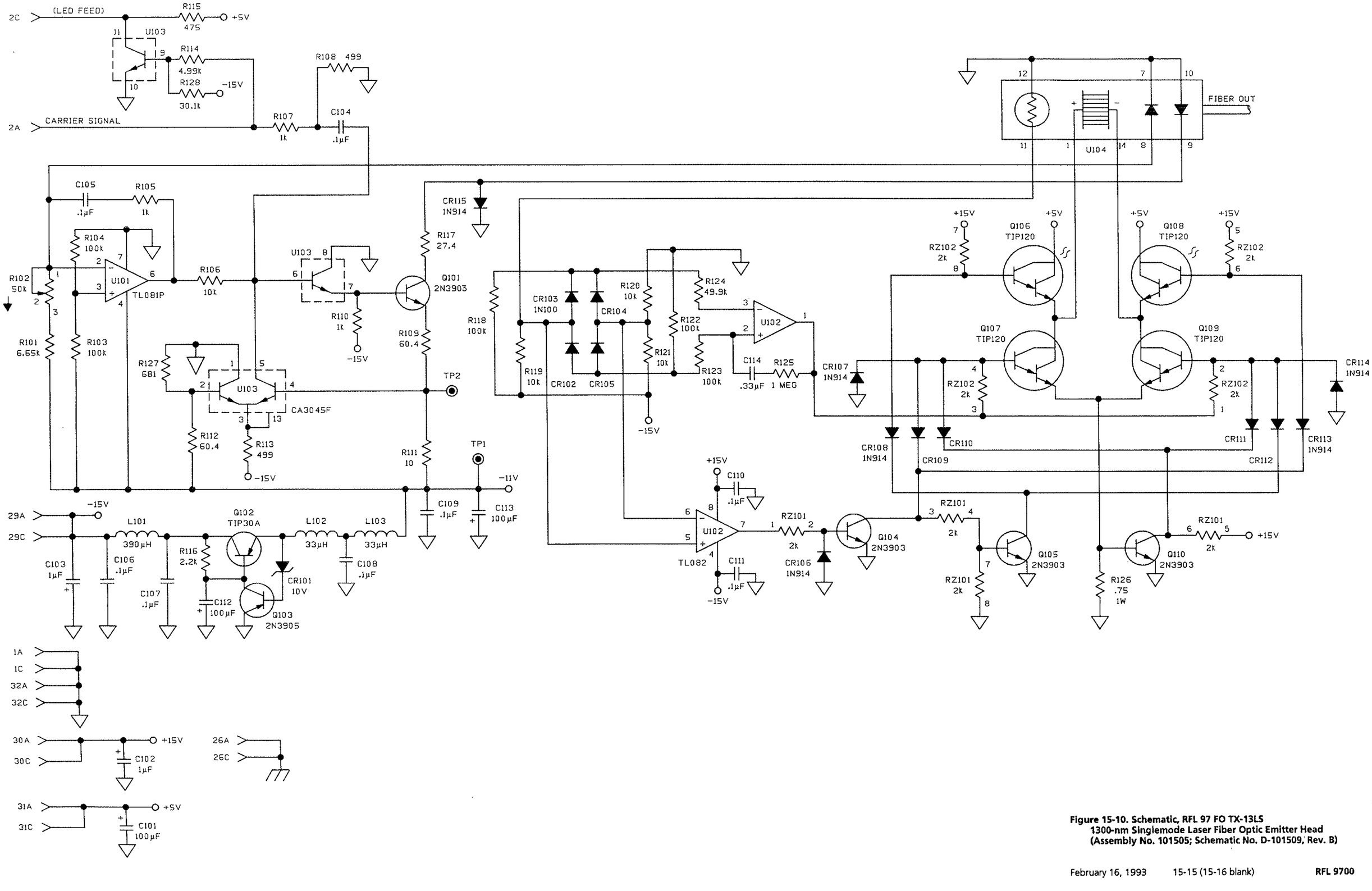


Figure 15-10. Schematic, RFL 97 FO TX-13LS 1300-nm Singlemode Laser Fiber Optic Emitter Head (Assembly No. 101505; Schematic No. D-101509, Rev. B)

15.3. FIBER OPTIC DETECTOR HEADS

15.3.1. Description

Each RFL 9700 fiber optic receiver module uses a fiber optic detector head, which is mounted at the rear of the chassis. This allows the fiber optic receiver module to be removed without drawing the fiber through the chassis. It also allows the user to choose the detector head that matches the type of fiber optic cable being used. A typical fiber optic detector head appears in Figure 15-11.

15.3.2. Specifications

As of the date this manual was published, the following specifications apply to all RFL 9700 fiber optic detector heads, except where indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Light Signal Characteristics: See Table 15-1.

Maximum Permissible Input Signal:
850-nm Heads: No limit.
1300-nm Heads: -30 dBm. If the incoming light level is greater than -30 dBm, attenuation must be added.

Output Signal:
Amplitude: 1.6 to 2.6 Vp-p.
Jitter: Less then 20 percent of the pulse width, or less than 30 ns.

Temperature:
Storage: -40°C to +75°C (-40°F to +167°F)
Operating: -30°C to +65°C (-22°F to +149°F)

Relative Humidity: 95 percent, non-condensing.

Input Power Requirements (from chassis supply):
RFL 97 FO RX-8M:
+5-Volt Supply: 500 mA.
+15-Volt Supply: 50 mA.
-15-Volt Supply: 1 mA.
RFL 97 FO RX-13M And RFL 97 FO RX-13/15S:
+5-Volt Supply: 20 mA.
+15-Volt Supply: 40 mA.
-15-Volt Supply: 10 mA.

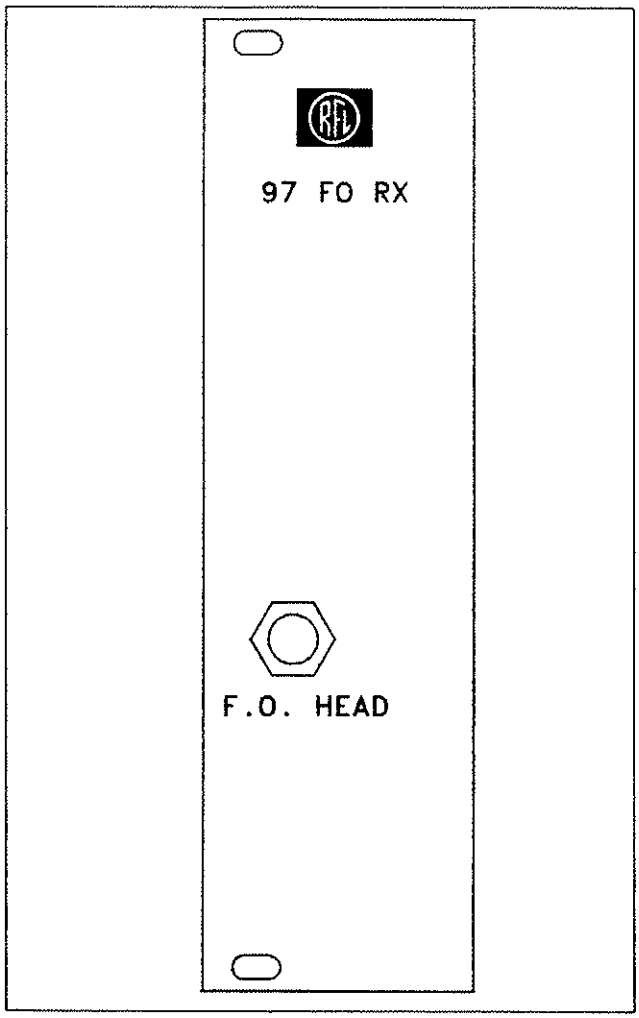


Figure 15-11. Typical fiber optic detector head

Dimensions:
Width (including panel): 1.4 inches (3.6 cm).
Height (including panel): 5 inches (12.7 cm).
Depth (behind panel): 3.3 inches (8.4 cm).

15.3.3. Theory Of Operation

Fiber optic detector heads accept the light signal sent over the fiber optic cable and convert it into an amplitude-modulated signal for input to the fiber optic receiver module (Section 14). Because each uses a different method to perform this function, theories or operation are provided for all detector heads.

15.3.3.1. RFL 97 FO RX-8M 850-nm Fiber Optic Detector Head

The RFL 97 FO RX-8M accepts 850-nm light signals that were sent over multimode fiber optic cables. A block diagram of the RFL 97 FO RX-8M appears in Figure 15-12.

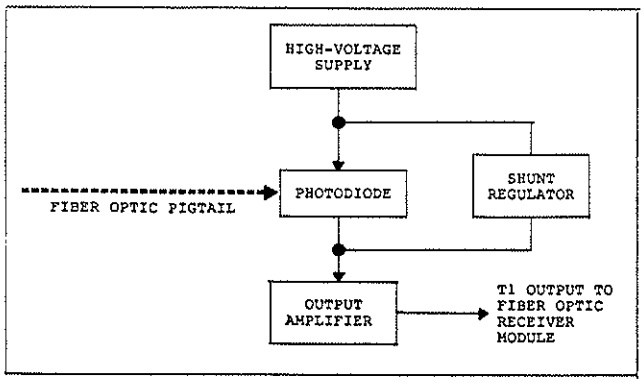


Figure 15-12. Block diagram, RFL 97 FO RX-8M 850-nm multimode fiber optic detector head

a. Photodiode. CR8 is an avalanche photodiode (APD), used to detect incoming light signals. For maximum sensitivity, CR8 has a high reverse bias voltage and a strictly regulated dc reverse bias current. CR8's photomultiplication factor is within 5 percent over the entire operating temperature range, when operated in a constant-current arrangement. This eliminates the need for a temperature compensation circuit.

b. High-Voltage Supply. Inductor L4 and capacitors C28 through C31 form an LC tank circuit, which is resonated by the oscillator formed from transistor Q2 and its associated components. This produces a sine wave that is rectified by diodes CR2 through CR7 and filtered by resistors R12 and R13 and capacitors C22 and C23. The output of this circuit is used to power CR8; this voltage can be measured at test point TP1.

c. Shunt Regulator. Operational amplifier U4, transistor Q1, and their associated components form a shunt regulator, which is used to regulate the current through CR8. The voltage across resistor R3 reflects the bias current through CR8. This is compared to a reference voltage set by potentiometer R9, which is adjusted at the factory to keep the current through CR8 within its optimum operating region. U4 accepts these voltages and acts as a differential amplifier, causing Q1 to shunt the excess current and regulate the current through CR8.

(4) Output Amplifier. Once properly biased, the current through CR8 will vary according to the light signal applied to it. This current is used to drive U1, which is a low-noise operational amplifier. The output of U1 drives a two-stage amplifier circuit formed from linear i.f. amplifiers U2 and U3, and their associated components. The output of U3 is coupled to edge connector terminal 2A through capacitor C20. This signal is passed through the chassis to the fiber optic receiver module (Section 14).

15.3.3.2. RFL 97 FO RX-13M And RFL 97 FO RX-13/15S Fiber Optic Detector Heads

The RFL 97 FO RX-13M accepts 1300-nm light signals that were sent over multimode fiber optic cables; the RFL 97 FO RX-13/15S accepts 1300-nm or 1500-nm light signals that were sent over singlemode fiber optic cables. Figure 15-13 is a block diagram for these 1300-nm fiber optic detector heads.

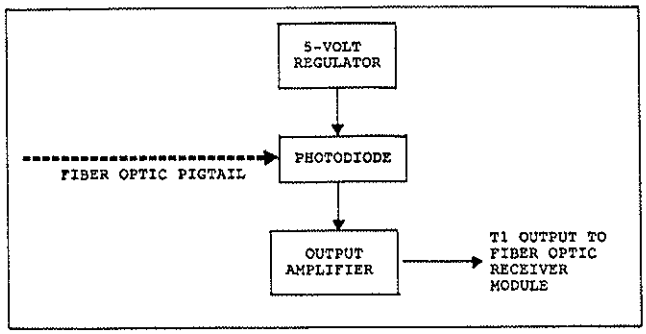


Figure 15-13. Block diagram, 1300-nm and 1500-nm fiber optic detector heads

U101 is a PINFET fiber optic detector, which converts the incoming light signal into an output voltage. Because the signal levels it works at are very small, it requires its own highly-regulated supply voltage; this is provided by linear regulator U104 and its associated components.

The output from U101 is used to drive a two-stage amplifier circuit formed from linear i.f. amplifiers U102 and U103, and their associated components. The output of U103 is coupled to edge connector terminal 2A through capacitor C124; this signal is passed through the chassis to the fiber optic receiver module (Section 14).

Table 15-5. Replaceable parts, RFL 97 FO RX-8M 850-nm multimode fiber optic detector head Assembly No. 101515

Circuit Symbol (Figs. 15-14 & 15-15)	Description	Part Number
C1-5,13-15,17,20,32	Capacitor,X7R ceramic,0.01μF,10%,100V,Kemet C320C103K1R5EA or equiv.	1007 1390
C6,7,9,11,12,16,19, 24,27	Capacitor,dipped ceramic,0.1μF,10%,50V,AVX SR205C104KAA or equiv.	1007 1667
C8,10,33,34	Capacitor,tantalum,1μF,20%,35V,Kemet T322B105M035AS or equiv.	1007 496
C18	Capacitor,ceramic,0.0018μF,5%,100V,AVX SA301A182JAA or equiv.	0125 11825
C21	Capacitor,ceramic disc,220pF,10%,500V,Erie 831-000-X5FO-221K or equiv.	1007 493
C22,23,25,26	Capacitor,Z5U ceramic,0.01μF,20%,500V,Erie 811000Z5U0103M or equiv.	1007 83
C28-31	Capacitor,ceramic,470pF,5%,100V,AVX SA101A471JAA or equiv.	0125 14715
CR1-7	Diode,silicon,1N914B or 1N4448	26482
CR8	Fiber optic detector,photodiode,850-mn,Mitsubishi PD1005 or equiv.	30258
L1-3	Inductor,rf,molded,100μH,10%,Gowanda 10/103 or equiv.	32505 1
L4	Inductor,molded,1000μH,5%,Stanwyck 410000M or equiv.	26529
L5	Choke,subminiature rf,18mH,J.W. Miller 70F182AI	21371
L6	Inductor,rf,molded,180μH,10%,Gowanda 10/183 or equiv.	32505 2
R1,10	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
R2,5,14,16	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R3	Resistor,metal film,49.9KΩ,1%,1/4W, Type RN1/4	0410 1451
R4,7,12,13	Resistor,metal film,499KΩ,1%,1/4W, Type RN1/4	0410 1547
R6	Resistor,metal film,100KΩ,1%,1/4W, Type RN1/4	0410 1480
R8	Resistor,metal film,100Ω,1%,1/4W, Type RN1/4	0410 1192
R9	Resistor,variable,18-turn cermet,1KΩ,10%,1/2W,Beckman Helipot 68WR1K or equiv.	49995
R11	Resistor,metal film,64.9KΩ,1%,1/2W, Type RN1/2	0410 2462
R15	Resistor,metal film,511Ω,1%,1/2W, Type RN1/2	0410 2260
R17,20	Resistor,metal film,182Ω,1%,1/4W, Type RN1/4	0410 1217
R18,19,21,22	Resistor,metal film,475Ω,1%,1/4W, Type RN1/4	0410 1257
Q1	Transistor,NPN,TO-18 case,2N6431	30504
Q2	Transistor,NPN,TO-92 case,2N5551	39484
U1	Hybrid amplifier,broad-band/low-noise,dc-400 MHz,Motorola MWA110 or equiv.	30505
U2,3	Linear i.f. amplifier,8-pin DIP,Motorola MC1350P or equiv.	0620 251
U4	Linear operational amplifier,JFET input,8-pin DIP,Texas Instruments TL081IP or equiv.	0620 228

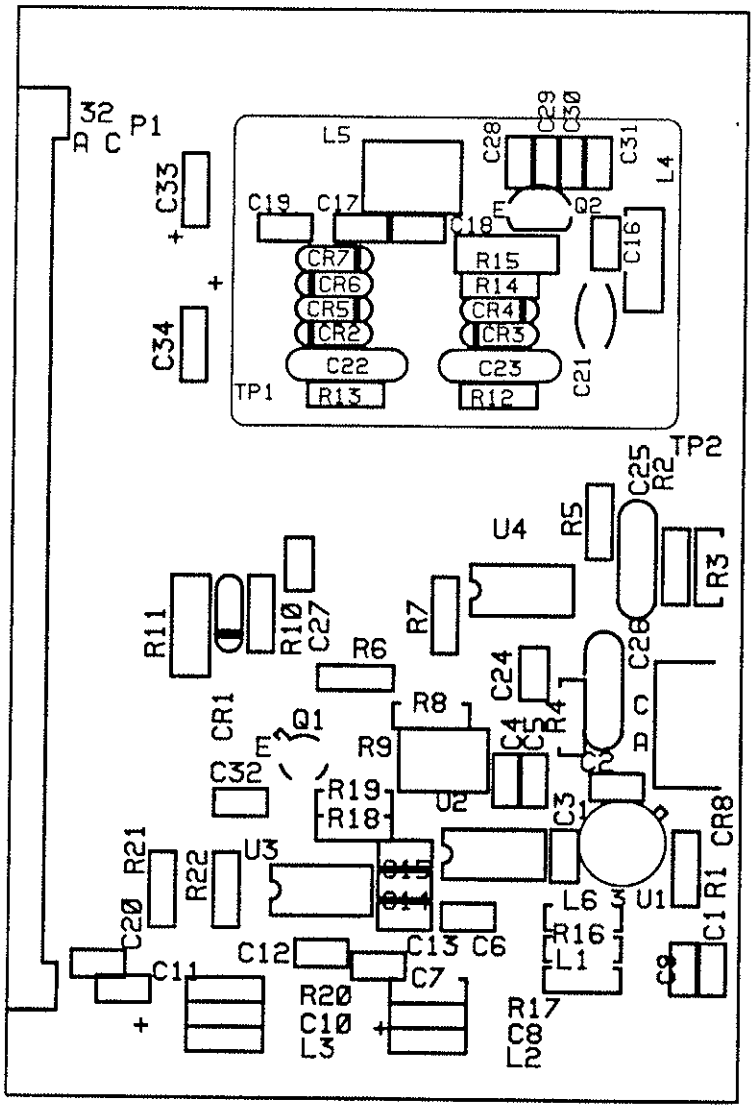


Figure 15-14. Component locator drawing, RFL 97 FO RX-8M 850-nm Multimode Fiber Optic Detector Head (Assembly No. 101515; Drawing No. C-101518, Rev. C)

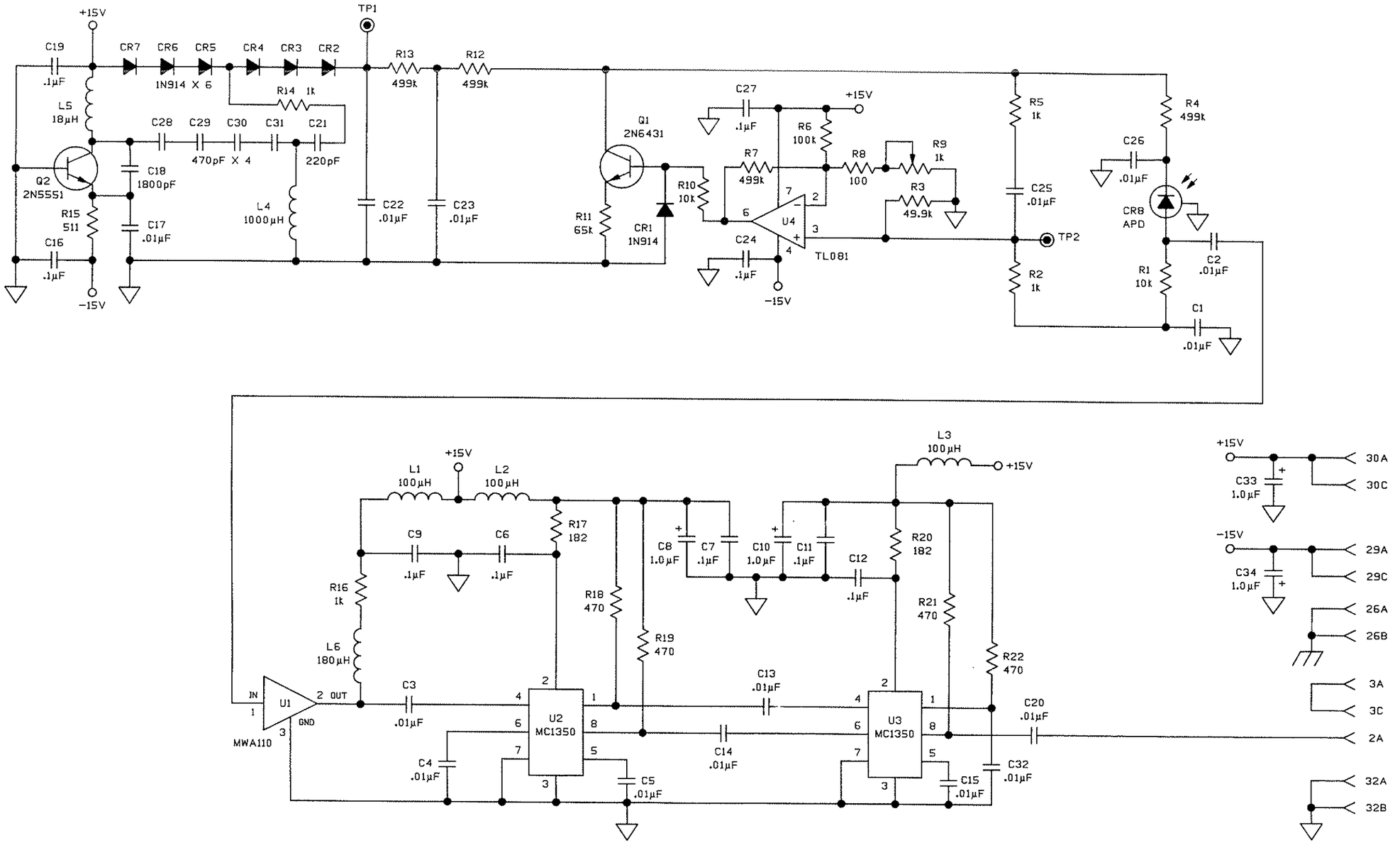


Figure 15-15. Schematic, RFL 97 FO RX-8M 850-nm Multimode Fiber Optic Detector Head (Assembly No. 101515; Schematic No. D-101519, Rev. C)

Table 15-6. Replaceable parts, 1300-nm and 1500-nm fiber optic detector heads
RFL 97 FO RX-13M (1300-nm Multimode) - Assembly No. 101520-1
RFL 97 FO RX13/15S (1300/1500-nm Singlemode) - Assembly No. 101520-2

Circuit Symbol (Figs. 15-16 & 15-17)	Description	Part Number
C101-104,107,109,114 120	Capacitor,X7R ceramic,0.1µF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C105,110,115,121	Capacitor,tantalum,1µF,20%,35V,Kemet T322B105M035AS or equiv.	1007 496
C106,111,112, 116-118,122-124	Capacitor,X7R ceramic,0.01µF,10%,100V,Kemet C320C103K1R5EA or equiv.	1007 1390
C108,113,119	Capacitor,ceramic,0.1µF,20%,50V,Centralab CZ20C104M or equiv.	1007 1574
L101,103,104,105	Inductor,rf,molded,100µH,10%,Gowanda 10/103 or equiv.	32505 1
L102	Inductor,molded,33µH,10%,130mA,ferrite core,Jeffers Electronics Type 09 1326-1K or equiv.	32868
R101	Resistor,metal film,33.2Ω,1%,1/8W,Type RN55D	1510 1433
R102,105	Resistor,metal film,182Ω,1%,1/4W, Type RN1/4	0410 1217
R103,104,106,107	Resistor,metal film,475Ω,1%,1/4W, Type RN1/4	0410 1257
U101	Fiber optic detector,PINFET,1300 to 1500 nm,14-pin DIP w/optic fiber pigtail, device type and connector type dependent upon model: RFL 97 FO RX-13M: SMA connector, Lasertron QDFT-015-001 or equiv. RFL 97 FO RX-13/15S: ST connector, Lasertron QDFT-015-003 or equiv.	 98466 99112
U102,103	Linear i.f. amplifier,8-pin DIP,Motorola MC1350P or equiv.	0620 251
U104	Linear voltage regulator,-5-volt,3-pin TO-92 case,Motorola MC79L05CP or equiv.	0620 267

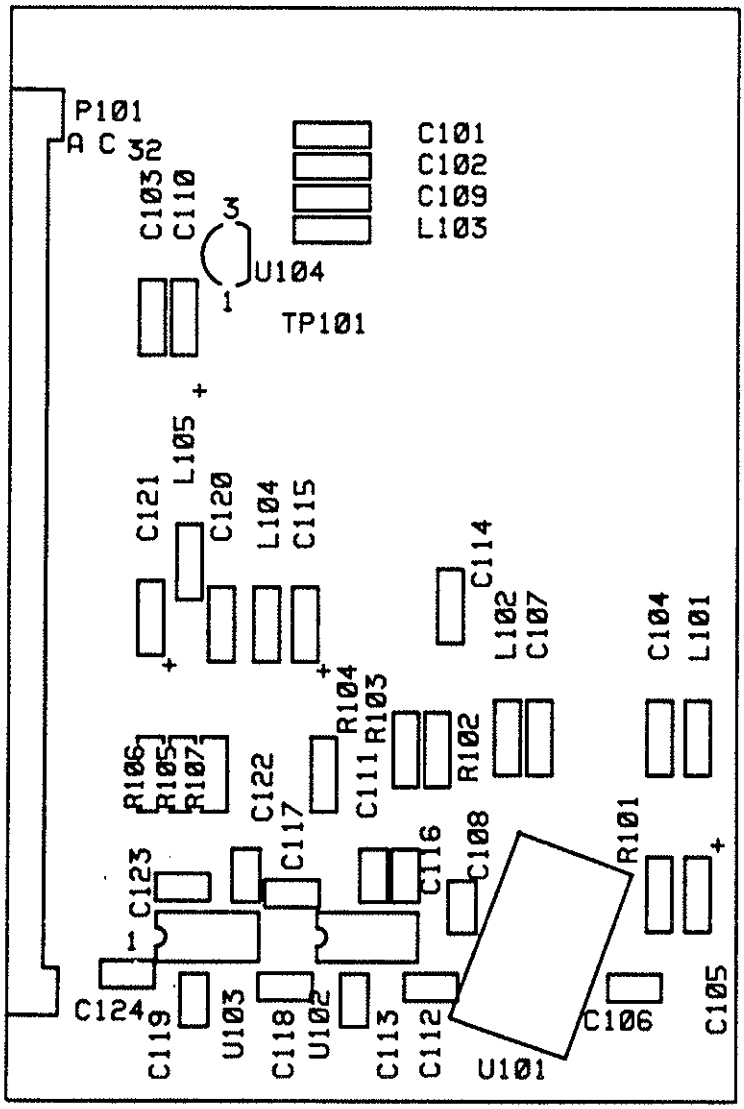
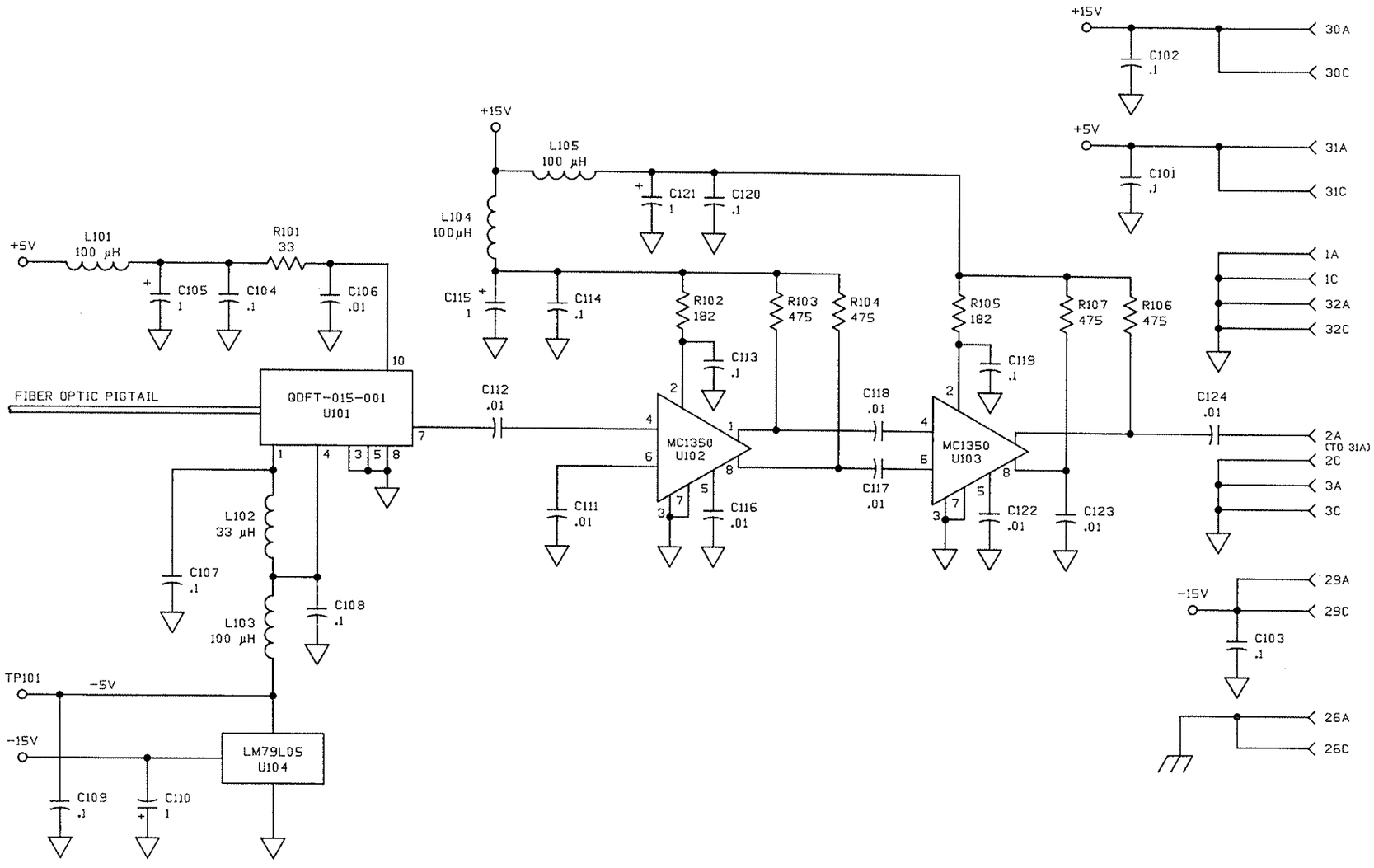


Figure 15-16. Component locator drawing, 1300-nm and 1500-nm fiber optic detector heads (Assembly No. 101520-X; Drawing No. C-101523, Rev. A)



ALL CAPACITORS ARE IN MICROFARADS
ALL RESISTORS ARE IN OHMS 1/4W, 1%
UNLESS OTHERWISE SPECIFIED

Figure 15-17. Schematic, 1300-nm and 1500-nm fiber optic detector heads (Assembly No. 101520-X; Schematic No. D-101524, Rev. A)

Section 16. POWER SUPPLIES

16.1. DESCRIPTION

RFL 9150 50-Watt Power Supply Modules are used to supply regulated dc power to the RFL 9700 Digital Protection Channel. These supplies provide three regulated outputs: +5, +15, and -15 volts. Switching regulators are used for high efficiency. All outputs have overvoltage protection and short circuit protection; in addition, the entire power supply will shut down if the ambient temperature exceeds a preestablished limit. A typical RFL 9150 power supply is shown in Figure 16-1.

The RFL 9150 is available in a wide range of ac and dc input voltages to suit virtually all applications. Table 16-1 summarizes the differences between the various models; model numbers appear on the module handle on the front panel.

16.2. SPECIFICATIONS

As of the date this manual was published, the following specifications apply to all RFL 9150 power supply modules, except where indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Voltage: See Table 16-1.

Output Voltages And Currents:
+5-Volt Supply: +4.75 to +5.25 volts @ 6 A
+15-Volt Supply: +14.25 to +15.75 volts @ 1.5 A
-15-Volt Supply: -14.25 to -15.75 volts @ 1.5 A

Output voltage variations given are over the specified temperature range of the supply, with the load current varied between 10 percent and 100 percent of the full-load rating.

Total Output Power: 50 watts maximum.

Minimum Loading Requirement: 5 percent.

Efficiency: Greater than 65 percent at full load.

Output Ripple:
5-Volt Supply: 0.1 Vp-p maximum.
15-Volt Supplies: 0.4 Vp-p maximum.

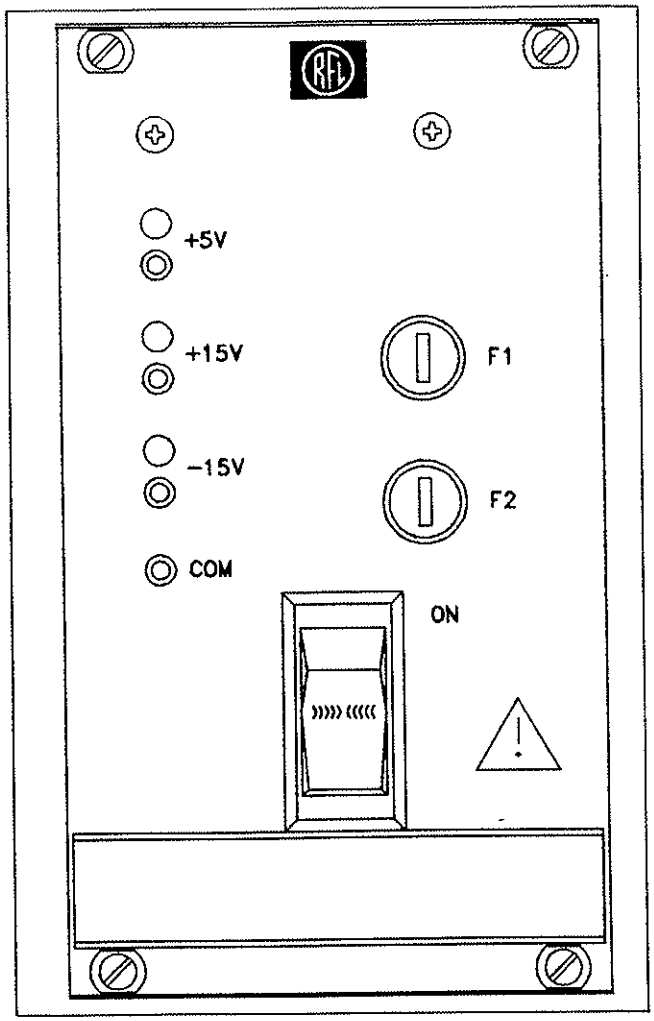


Figure 16-1. Typical RFL 9150 50-watt power supply module

Temperature Protection:
Input Converter: Shutdown will occur between +90°C and +105°C (+194°F and +221°F).
Output Converter: Shutdown will occur between +100°C and +110°C (+212°F and +230°F).

Undervoltage Protection: Supply will not be damaged by input voltages below the minimum specified; the supply may or may not operate.

Overvoltage Protection: Supply will shut down if the 5-volt output rises to +7 volts, or if either 15-volt output rises to 20 volts. To restart, main power switch must be manually cycled.

Table 16-1. Differences between RFL 9150 50-Watt Power Supply Modules

Model Number	Assembly Number	Output Converter Board	Input Converter Board	Input Voltage Range	Maximum Input Current *
9150A 24 DC	101980-1	101991	101993-1	19.2 to 28.8 Vdc	4.5 A
9150B 48 DC	101980-2	101991	101993-2	38.4 to 57.6 Vdc	2.2 A
9150B 125 DC	101980-3	101991	101993-3	100 to 150 Vdc	840 mA
9150A 250 DC	101980-4	101991	101993-4	200 to 300 Vdc	420 mA
9150B 110 AC	101985-1	101991	101993-9	99 to 121 Vac	800 mA
9150A 220 AC	101985-2	101991	101993-6	198 to 242 Vac	400 mA

* - Maximum current is drawn when power supply module is operating at full load with minimum voltage present at its input terminals.

Overload Protection: Supply will shut down if load currents exceed the following limits:

+5-Volt Supply: 11 amperes maximum.
+15-Volt Supply: 9 amperes maximum.
-15-Volt Supply: 6 amperes maximum.

To reset, main power switch must be manually cycled.

Isolation: Circuit common is isolated from chassis ground by at least 2500 Vdc.

Surge Withstand Capability: Meets the requirements of ANSI/IEEE C37.90.1.198X.

Environmental Requirements:

Temperature:
Operating: -30°C to +70°C (-22°F to +158°F).
Storage: -40°C to +70°C (-40°F to +158°F).
Survival: -40°C to +70°C (-40°F to +158°F); supply may not meet specifications, but it must not suffer damage while operating over this range.
Relative Humidity: 95 percent maximum (non-condensing), for up to 96 hours at temperatures up to +56°C (+133°F).
Altitude: 10,000 feet (3050 meters).

Dimensions: 5.1 inches x 2.8 inches x 8.8 inches (130 mm x 71 mm x 225 mm; occupies twelve horizontal positions (12E) in a Single-Euro chassis.

16.3. THEORY OF OPERATION

RFL 9150 50-Watt Power Supply Modules convert the available ac or dc input power into three dc voltages: +5, +15, and -15. Each module contains input protection circuits, an input converter that produces the +15-volt output, a +5-volt dc/dc converter, a -15-volt dc/dc converter, and additional circuits for thermal and overvoltage protection. A block diagram appears in Figure 16-2.

NOTE

RFL 9150 power supply modules are equipped with several protection circuits. These circuits will cause the module to shut down if its voltage, current, or temperature limits are exceeded. If the RFL 9150 has shut down, it can be reset by placing power switch S1 in the OFF position, and then placing it back in the ON position. If it shuts down again, troubleshoot the RFL 9700's chassis to make sure that nothing external to the RFL 9150 is causing it to shut down. If nothing is found in the rest of the chassis and the RFL 9150 is still shutting down, the RFL 9150 may be defective, and should be serviced.

16.3.1. Input Protection Circuits

All RFL 9150 power supply modules accept input power between edge connector pins 15 through 17 and 23 through 25 on the input converter board. Input surge protection is provided by transient suppressor CR1, capacitors C27 and C28, and inductors L1 and L2. Fuses F1 and F2 limit the input current, and rocker switch S1 serves as the main power switch for the entire module. Transient suppressor CR16 provides additional surge protection.

Jumpers A through E route the voltage through the input protection circuits, according to its level and type. In dc-powered modules, jumpers D and E are in place so the voltage across CR16 passes directly to the input converter, bypassing the rest of the input protection circuits.

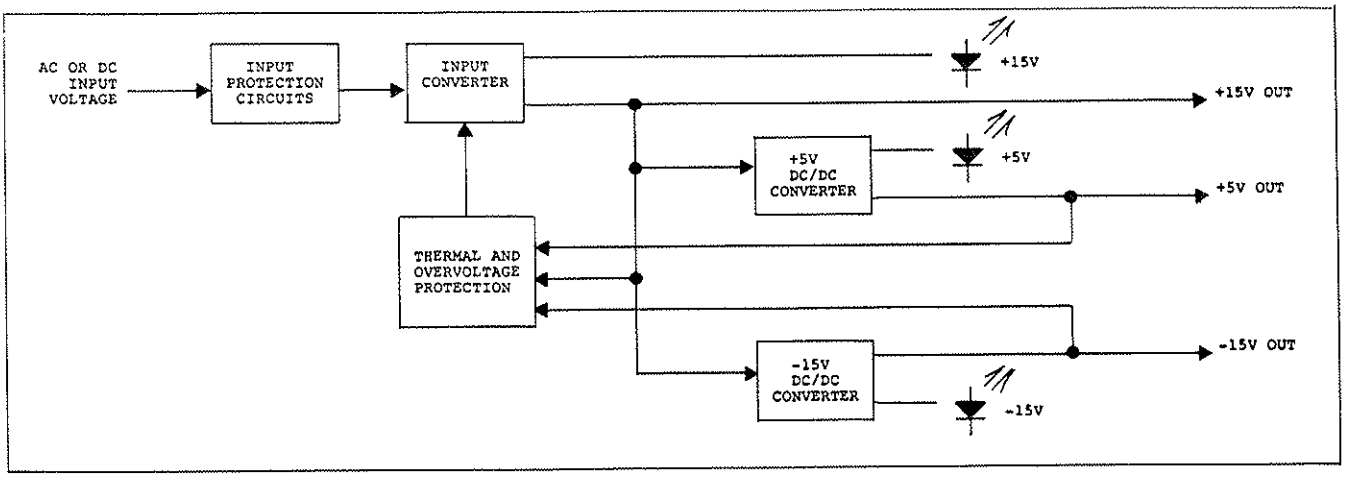


Figure 16-2. Block diagram, RFL 9150 50-Watt Power Supply Modules

In ac-powered modules, D and E are omitted so the voltage across CR16 is passed through thermistors RT1 and RT2 to bridge rectifier A2, where it is rectified.

Capacitors C1, C2, and C30 serve as an output filter for the input protection circuits. The exact configuration of this filter is determined by the presence of C1 and C30, and the placement of jumpers A, B, and C.

16.3.2. Input Converter

The output of the input protection circuits is applied to the Vin+ and Vin- terminals of converter module A1. A1 produces a +15-volt output at its +Vo and -Vo terminals. This voltage is fed out through L3 as the +15-volt output of the power supply. It is also fed to the +5-volt and -15-volt dc/dc converters.

16.3.3. +5-Volt Dc/dc Converter

The first dc/dc converter changes the +15-volt output produced by the input converter into +5 volts. This converter consists of converter U2, translator U3, and transformer T1. U2 is a switch mode integrated circuit, which operates in the current mode. When the current reaches a programmed level, the transistor between U2-4 and U2-1 is opened; at currents below the programmed level, this transistor is closed or shorted.

The output of U2 is pulse-width modulated at a constant 40-kHz switching frequency, and provides a switched current which is integrated across capacitor C19; a constant output of +5 volts results.

U2-2 is the reference input. When the voltage on U2-2 is 1.24 volts higher than the voltage on U2-3, U2 starts to modulate pulse widths, reducing the amount of current before turning off. In this way, the +5-volt output level is regulated and maintained.

U3 is used to convert the +5-volt output of U2 into 6.24 volts. The voltages on U2-2 and U2-3 provide the feedback voltage which determines the regulation point of the switch mode regulator.

Resistor R11, diode CR9, and capacitor C13 form a snubber circuit, which limits the amount of voltage on U2-4. This voltage is created by the leakage inductance of T1. During the portion of the cycle when U2 is off, additional current is provided through T1, which then operates in a fly-back mode. Current is provided to the 5-volt output at all times, whether U2 is on or T1 is discharging into capacitor C19. This circuit acts as a current multiplier, and allows the 5-volt supply's output current to exceed the limit of U2, which is 5 amperes.

16.3.4. -15-Volt Dc/dc Converter

The -15-volt dc/dc converter changes the +15-volt output of the input converter to -15 volts. Converter U4 and inductor L6 perform this conversion. When the voltage on U4-2 is less than 1.24 volts higher than the voltage on U2-3, a switching transistor inside U4 turns on, causing a current to flow through L6. U4 functions as a pulse width modulated switching converter, turning on and off at a 40-kHz rate. When U4 turns off, a negative potential is generated by the continued current flow through L6. This negative voltage is rectified by diode CR11 and capacitor C23; as a result, the

voltage across C23 is equal to the -15-volt excursions across L6. This voltage is divided down through resistors R19 and R20 to provide the reference point for U4-2.

When the reference voltage is more than 1.24 volts higher than the voltage on U4-3, the on time for the switching transistor inside U4 will be reduced. This is how U4 regulates the -15-volt output.

Diode CR12 and capacitors C29 and C26 create a constant operating bias between U4-3 and U4-5. The negative pulse train created by U4 and L6 is rectified by diode CR7 and filtered by capacitor C11, and presented at edge connector pin 9 as a steady, regulated -15 volts.

16.3.5. Thermal And Overvoltage Protection

U1 supervises the thermal and overvoltage protection of the entire power supply. U1-2 is its SENSE terminal. If the voltage at U1-2 exceeds 2.6 volts, a comparator inside U1 will turn on, triggering silicon-controlled rectifier Q1. This will short out the output of converter module A1, disabling the other dc-dc converters. At the same time, a transistor between U1-6 and U1-7 will turn on, shutting down A1.

Resistors R23 and R24 form a voltage divider across the output of the +5-volt dc/dc converter. As long as the output of the +5-volt converter does not exceed 5.5 volts, the voltage produced by the voltage divider will be less than 2.6 volts and U1 will not be tripped. Resistors R4 and R5 perform the same function for the -15-volt converter. Thermal sensor RT3 is a thermistor mounted on the same heat sink as U2, U4, diode CR6, and Q1. It forms a voltage divider along with resistors R30 and R31. RT3's resistance is about 100Ω at temperatures below +100°C; this keeps the output of the voltage divider below 2.6 volts. If the temperature goes above +100°C, RT3's resistance will double, causing the voltage divider's output to go above 2.6 volts.

Diodes CR2, CR3, and CR4 form a 3-input OR gate, which combines the voltage divider outputs. The output of the OR gate drives U1-2, so any voltage divider output above 2.6 volts will trip U1.

Transistor Q2 is used to trip U1 if the voltage at the output of the -15-volt supply (edge connector pin 9) becomes more negative than -15 volts. The base of Q2 is a current summing node; during normal operation, current is injected into the base of Q2, and Q2 is turned on. If Q2 turns off or the voltage at the base of Q2 falls below +0.6 volts, U1-5 will be pulled up through resistor R37, shutting down the converter.

Resistors R6 and R38 and Zener diode CR18 bias the base of Q2; current is drawn from this node through resistor R28 by the -15-volt supply. If the output of the -15-volt dc/dc converter exceeds its set limit, more and more current will be drawn from the base of Q2. If the output of the -15-volt dc/dc converter reaches -20 volts, enough current will be drawn through R28 to turn off Q2.

All outputs are current limited by the maximum capacities of A1, U2, and U4. A1 also contains its own internal thermal protection circuit; thermal shutdown of A1 will occur somewhere between +90°C and +100°C.

Table 16-2. Replaceable parts, RFL 9150 50-watt Power Supply Modules
(See Table 16-1 for assembly numbers.)

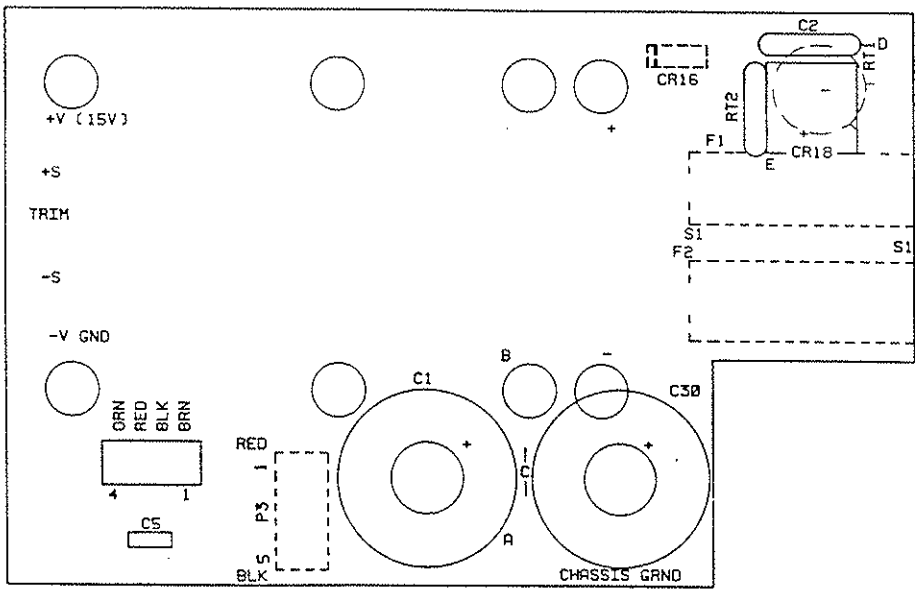
Circuit Symbol (See Figs. 16-3 thru 16-5.)	Description	Part Number
	CAPACITORS	
C1	Capacitor,electrolytic,value dependent upon model: RFL 9150A 24 DC, RFL 9150B 48 DC, and RFL 9150B 125 DC: Not used. All Others: Same as C30.	
C2-4,27,28	Capacitor,ceramic disc,0.005µF,20%,3kV,Centralab DD30-502 or equiv.	1007 1264
C5,9,15,22,24	Capacitor,Z5U ceramic,0.33µF,+80/-20%,50V,Murata RPA3025U334Z50V or equiv.	0135 53348
C6,18,20,29,33	Capacitor,X7R ceramic,0.1µF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C7,31	Capacitor,tantalum,1µF,20%,35V,Kemet T322B105M035AS or equiv.	1007 496
C8,11	Capacitor,electrolytic,2700µF,+30/-10%,25V,Sprague 80D272P025HA5 or equiv.	1007 1678
C10	Capacitor,tantalum,15µF,20%,20V,Kemet T322D156M020AS or equiv.	1007 716
C12	Capacitor,ceramic,0.0018µF,5%,100V,AVX SA301A182JAA or equiv.	0125 11825
C13	Capacitor,metallized polycarbonate,0.285µF,2%,100V,Wesco 32MPC or equiv.	1007 1423
C14,16	Capacitor,X7R ceramic,0.01µF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C17	Capacitor,ceramic,220pF,5%,100V,AVX SA101A221JAA or equiv.	0125 12215
C19	Capacitor,electrolytic,5600µF,+30/-10%,10V,Sprague 80D562P010HA5 or equiv.	1007 1679
C21	Capacitor,tantalum,220µF,20%,10V,Kemet T350L227M010AS or equiv.	1007 1684
C23	Capacitor,tantalum,1µF,10%,35V,Kemet T362A105K035AS or equiv.	1007 1566
C25	Capacitor,electrolytic,100µF,20%,50V,Nichicon ULB1H101M or equiv.	1007 1513
C26	Capacitor,tantalum,4.7µF,20%,20V,Kemet T322B475M020AS or equiv.	1007 711
C30	Capacitor,electrolytic,radial leads,value dependent upon model: Ac Models: 220µF,+30/-10%,200V;Sprague 80D221P200KA5 or equiv. Dc Models: 22µF,20%,250V;Illinois Capacitor 226RMR250M or equiv.	 1007 1676 1007 1726
C32	Capacitor,ceramic,0.1µF,GMV,50V,Centralab CY20C104P or equiv.	1007 1563
	RESISTORS	
R1	Not used.	
R2,31	Resistor,metal film,100Ω,1%,1/4W, Type RN1/4	0410 1192
R3,14,15	Resistor,metal film,4.99KΩ,1%,1/4W, Type RN1/4	0410 1355
R4	Resistor,metal film,200Ω,1%,1/4W, Type RN1/4	0410 1221
R5	Resistor,metal film,845Ω,1%,1/4W, Type RN1/4	0410 1281
R6	Resistor,metal film,2.21KΩ,1%,1/4W, Type RN1/4	0410 1321
R7,13,20,21,24,32-34	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R8,25	Resistor,metal film,221Ω,1%,1/4W, Type RN1/4	0410 1225
R9	Resistor,metal film,1KΩ,1%,1/2W, Type RN1/2	0410 2288
R10,22	Resistor,composition,470Ω,10%,1W,Allen-Bradley GB Series or equiv.	1009 662

Table 16-2. Replaceable parts, RFL 9150 50-watt Power Supply Modules - continued.

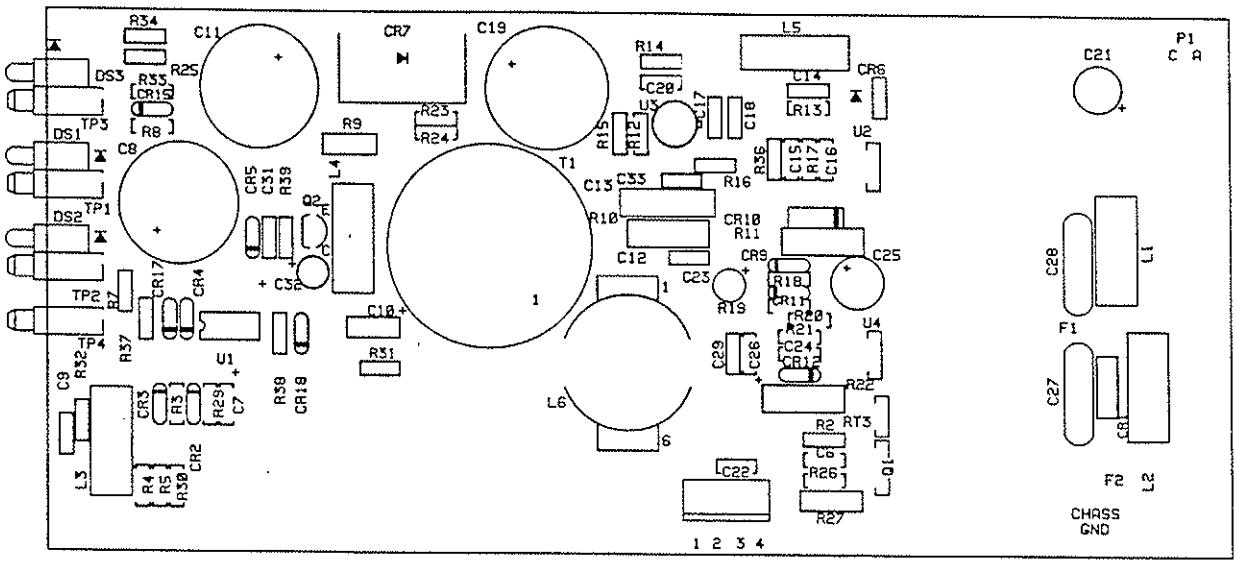
Circuit Symbol (See Figs. 16-3 thru 16-5.)	Description	Part Number
	RESISTORS - continued.	
R11	Resistor,wirewound,500Ω,5%,3.25W,Ohmite 4411 Style 995-3A or equiv.	1100 308
R12,16	Resistor,metal film,1.18KΩ,1%,1/4W, Type RN1/4	0410 1295
R17	Resistor,metal film,681Ω,1%,1/4W, Type RN1/4	0410 1272
R18,26,39	Resistor,metal film,49.9Ω,1%,1/4W, Type RN1/4	0410 1163
R19	Resistor,metal film,11KΩ,1%,1/4W, Type RN1/4	0410 1388
R23	Resistor,metal film,866Ω,1%,1/4W, Type RN1/4	0410 1282
R27	Resistor,composition,1Ω,5%,1/2W, Allen-Bradley EB Series or equiv.	1009 978
R28	Diode,Zener,3.9V,10%,500mW,1N5228A	32607
R29,36	Resistor,metal film,100KΩ,1%,1/4W, Type RN1/4	0410 1480
R30	Resistor,metal film,1.37KΩ,1%,1/4W, Type RN1/4	0410 1301
R37	Resistor,metal film,301KΩ,1%,1/4W, Type RN1/4	0410 1526
R38	Resistor,metal film,1.24KΩ,1%,1/4W, Type RN1/4	0410 1297
RT1,2	Thermistor,value dependent upon model: Ac Models: 5Ω @ +25°C,6A steady-state current, Keystone CL-40 or equiv. Dc Models: Not used.	30438
RT3	Thermistor,positive temperature coefficient,Keystone RL2006-100-100-30PTI or equiv.	30439
	SEMICONDUCTORS	
A2	Bridge rectifier,type dependent upon model: Ac Models: 400V,6A,Varo VH448 or equiv. Dc Models: Not used.	48731
CR1	Transient suppressor,bi-directional,380- to 420-volt breakdown, General Semiconductor 1.5KE400CA or equiv.	30442
CR2-4,11,17	Diode,silicon,1N914B or 1N4448	26482
CR5	Diode,silicon,200 PIV,1N4003	30769
CR6,7	Diode,Schottky,45V,7A,TO-220 case,Motorola MBR745 or equiv.	30435
CR9,12	Diode,Schottky,60V,1A,DO-41 case,International Rectifier 11DQ06 or equiv.	96365
CR10	Diode,rectifier,200V,3A,Motorola MR502 or equiv.	90912
CR15	Diode,Zener,10V,5%,400mW,1N961B	34874
CR16	Input protection device; type and voltage ratings dependent upon supply input voltage: RFL 9150 24 DC: Transient suppressor,31.4- to 34.7-volt breakdown, General Semiconductor 1.5KE33A or equiv. RFL 9150 48 DC: Transient suppressor,64.6- to 71.4-volt breakdown, General Semiconductor 1.5KE68A or equiv. RFL 9150 125 DC: Transient suppressor,190- to 210-volt breakdown, General Semiconductor 1.5KE200A or equiv. RFL 9150 250 DC: Diode,fast recovery,400V,2A,General Electric A114D or equiv. RFL 9150 110 AC: Transient suppressor,190- to 210-volt breakdown, General Semiconductor 1.5KE200CA or equiv. RFL 9150 220 AC: Not used.	30447 30448 30449 47659 30266

Table 16-2. Replaceable parts, RFL 9150 50-watt Power Supply Modules - continued.

Circuit Symbol (See Figs. 16-3 thru 16-5.)	Description	Part Number
	SEMICONDUCTORS - continued.	
CR18	Diode,Zener,18V,10%,500mW,1N4746A	29757
DS1-3	Light-emitting diode,green,right-angle panel mount,Schroff 69004.122 or equiv.	30472
Q1	Diode,rectifier,50V,8A,TO-220AB case,General Electric C122F or equiv.	41073
Q2	Transistor,NPN,TO-92 case,2N3903	21562
U1	Linear overvoltage sensing circuit,8-pin ceramic DIP,Motorola MC3523V or equiv.	0620 310
U2	Linear switching regulator,+75-volt output @ 5 amperes,5-pin TO-220 plastic package, Linear Technology LT1070HVCT	0620 317
U3	Linear operational amplifier,8-pin TO-5 case,National Semiconductor LM208H or equiv.	0620 146
U4	Linear switching regulator,5-pin TO-220 package,Linear Technology LT1070CT or equiv.	0620 309
	MISCELLANEOUS COMPONENTS	
A1	Dc-dc converter module,+15-volt output, input voltage and output power dependent upon model:	
	RFL 9150 24 DC: 24-volt input,100W,Vicor VI-212-IW or equiv.	30589
	RFL 9150 48 DC: 48-volt input,100W,Vicor VI-232-IW or equiv.	30590
	RFL 9150 125 DC and 9150 110 AC: 150-volt input,100W,Vicor VI-252-IW or equiv.	30591
	RFL 9150 250 DC and 9150 220 AC: 300-volt input,100W,Vicor VI-262-IW or equiv.	30592
F1,2	Input fuse,250V,current rating and blow characteristics dependent upon model:	
	RFL 9150 24 DC: Fuse,3AG normal-blow,8A,250V,Littelfuse 312008 or equiv.	44395 008
	RFL 9150 48 DC: 3AG slow-blow,4A;Littelfuse 313 004 or equiv.	91935
	RFL 9150 125 DC and 9150 110 AC: 3AG slow-blow,2A;Littelfuse 313 002 or equiv.	7549
	RFL 9150 250 DC: 3AG slow-blow,1A;Littelfuse 313 001 or equiv.	6645
	RFL 9150 220 AC: Type T (5 x 20 mm) slow-blow,1A;Littelfuse 213 001 or equiv.	30457
L1-5	Choke,high-current,12µH,4.5A,10%,40 MHz series resonant frequency,Caddell-Burns 6860-02 or equiv.	30436
L6	Inductor,high-power/high-frequency	101983
SW1	Switch,rocker,SPST,16A,marked,high inrush current	30441 1
T1	Transformer,flyback	101979 2

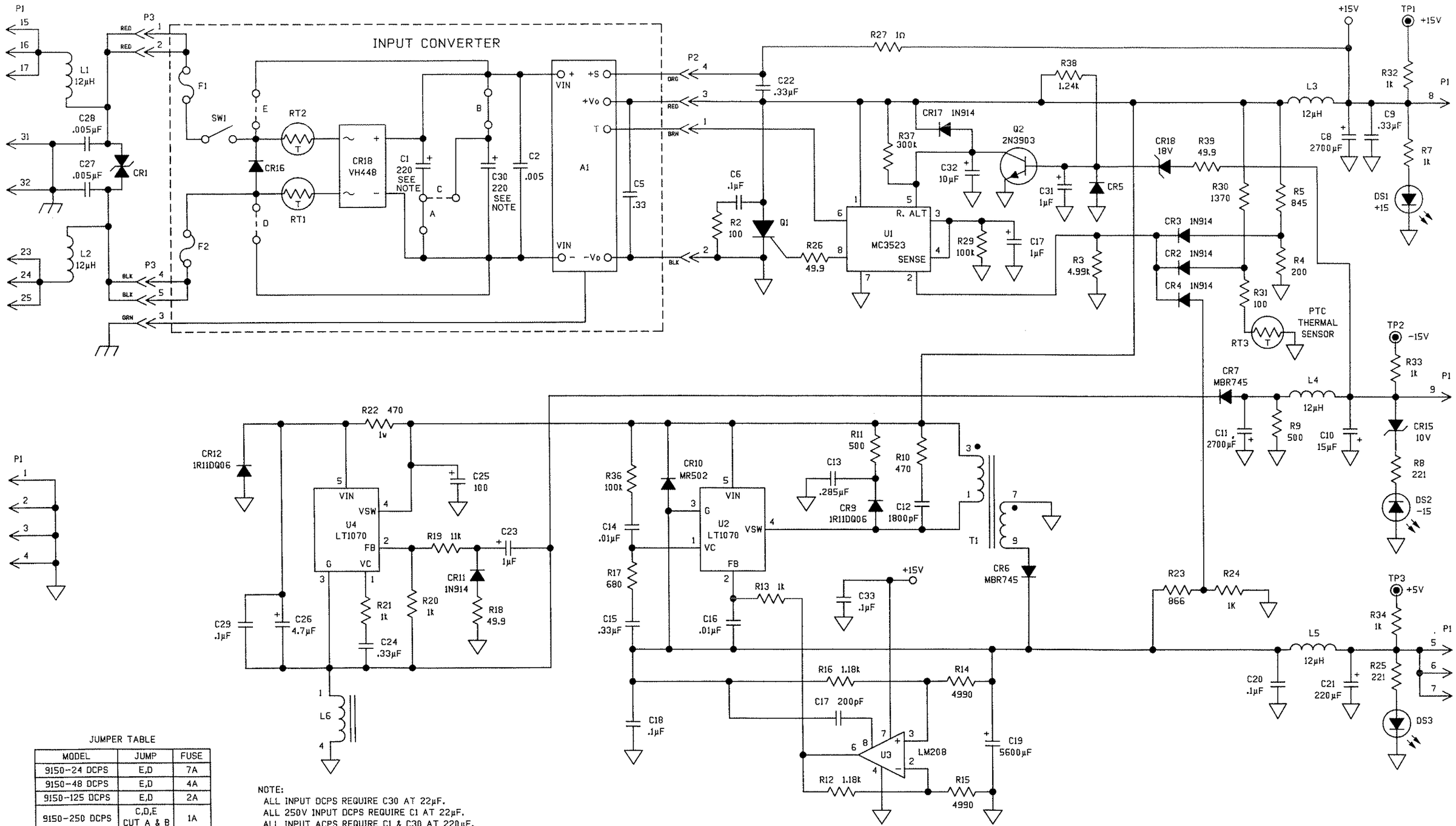


a. Input converter board (Assembly No. 101993-X; Drawing No. D-103998, Rev. A)



b. Output converter board (Assembly No. 101991; Drawing No. D-101973, Rev. G)

Figure 16-3. Component locator drawings, RFL 9150 50-watt power supply modules



JUMPER TABLE

MODEL	JUMP	FUSE
9150-24 DCPS	E,D	7A
9150-48 DCPS	E,D	4A
9150-125 DCPS	E,D	2A
9150-250 DCPS	C,D,E CUT A & B	1A
9150-110 ACPS	NONE	2A
9150-220 ACPS	C CUT A & B	1A

NOTE:
ALL INPUT DCPS REQUIRE C30 AT 22µF.
ALL 250V INPUT DCPS REQUIRE C1 AT 22µF.
ALL INPUT ACPS REQUIRE C1 & C30 AT 220µF.

Figure 16-4. Schematic, RFL 9150 50-watt power supply modules (Schematic No. D-101984, Rev. D)

Section 17. CHASSIS

17.1. INTRODUCTION

This section contains information on the assemblies that make up the RFL 9700's chassis. Paragraph 17.1 covers the chassis itself, and paragraph 17.2 describes the interconnect motherboard that provides all electrical connections between RFL 9700 modules. Paragraph 17.3 provides information on the RFL 97 449 INTER RS-449 Interface Panel, that is used in 56-Kbps RFL 9700 terminals not equipped with fiber optic modules. Paragraph 17.4 covers the RFL 97 X.21 INTER RS-449 Interface Panel, that is used in 64-Kbps RFL 9700 terminals.

17.2. RFL 97 CHAS SINGLE-EURO CHASSIS

The RFL 97 CHAS Single-Euro Chassis serves as the main enclosure for the RFL 9700 Digital Protection Channel. It provides a means of housing and interconnecting all the RFL 9700 modules. The RFL 97 CHAS can be mounted in any standard EIA 19-inch rack or cabinet, or it can be used as a standalone desk-mount cabinet. When rack-mounted, it occupies three vertical rack mounting spaces, or 5.25 inches of vertical panel space (13.34 cm). Adjustable mounting ears allow the chassis to be mounted so that its front panel is either flush with the rack or protruding out the front of the rack.

The RFL 97 CHAS's dimensions are as follows:

Overall Width: 19 inches (48.3 cm), including mounting ears.

Overall Height: 5.25 inches (13.3 cm).

Overall Depth: 14 inches (35.6 cm), from front of chassis to protective cover over rear-panel terminal blocks.

17.3. RFL 97 INTER INTERCONNECT MOTHERBOARD

Interconnections between all RFL 9700 circuit card modules are made through the RFL 97 INTER Interconnect Motherboard, which is mounted toward the rear of the chassis. Figure 17-1 is a component locator drawing for the RFL 97 INTER interconnect board, which is the motherboard for the RFL 97 CHAS chassis. A schematic for the RFL 97 INTER appears in Figure 17-2.

a. Power Supply Filtering. Capacitors C1 through C6 form filters for the three power supplies in the RFL 9150 50-Watt Power Supply Module (Section 16). These filters work along with the filters inside the RFL 9150 to provide a further reduction of ripple and transients.

b. Ground Coupling. Capacitors C13 through C21 couple the circuit common bus to chassis ground. These capacitors are bypassed if the "A" jumper is installed, because the circuit common bus is then connected directly to chassis ground.

c. Alarm Output Relays. Relays K1 and K2 serve as alarm output relays for the RFL 9700. K1's coil is connected through resistor R1 to edge connector J7-a7, which is the NON-FATAL ALARM output from the RFL 97A IND/OUT module (Section 12). Resistor R12 connects K2's coil to edge connector J7-a8, which is the FATAL ALARM output of the RFL 97A IND/OUT.

Inductors L1 through L6 and capacitors C9 through C12 filter out any switching spikes that may be generated as the relays change state. The relay contacts are wired to terminal block TB9 through connector J18.

Table 17-1. Replaceable parts, RFL 97 INTER Interconnect Motherboard Assembly No. 101580-5

Circuit Symbol (Figs. 17-1 & 17-2)	Description	Part Number
C1,3,5	Capacitor,tantalum,22µF,20%,35V,Corning CCZ-035-226-20 or equiv.	1007 657
C2,4,6	Capacitor,X7R ceramic,0.01µF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C7-21	Capacitor,ceramic disc,0.005µF,20%,3kV,Centralab DD30-502 or equiv.	1007 1264
K1,2	Relay,SPDT,pc-mount,12-volt/270Ω high-isolation coil,10A contacts (24 Vdc or 240 Vac), AMF/Potter & Brumfield RKA-5DG-12 or equiv.	101236
L1-6	Inductor,rf,10µH,5%,J.W. Miller 4622 or equiv.	30285
R1,2	Resistor,zero-ohm,1/4-watt size,Corning OMA07 or equiv.	1510 2217
---	Shorting bar,single,Molex 90059-0009 or equiv.	98306

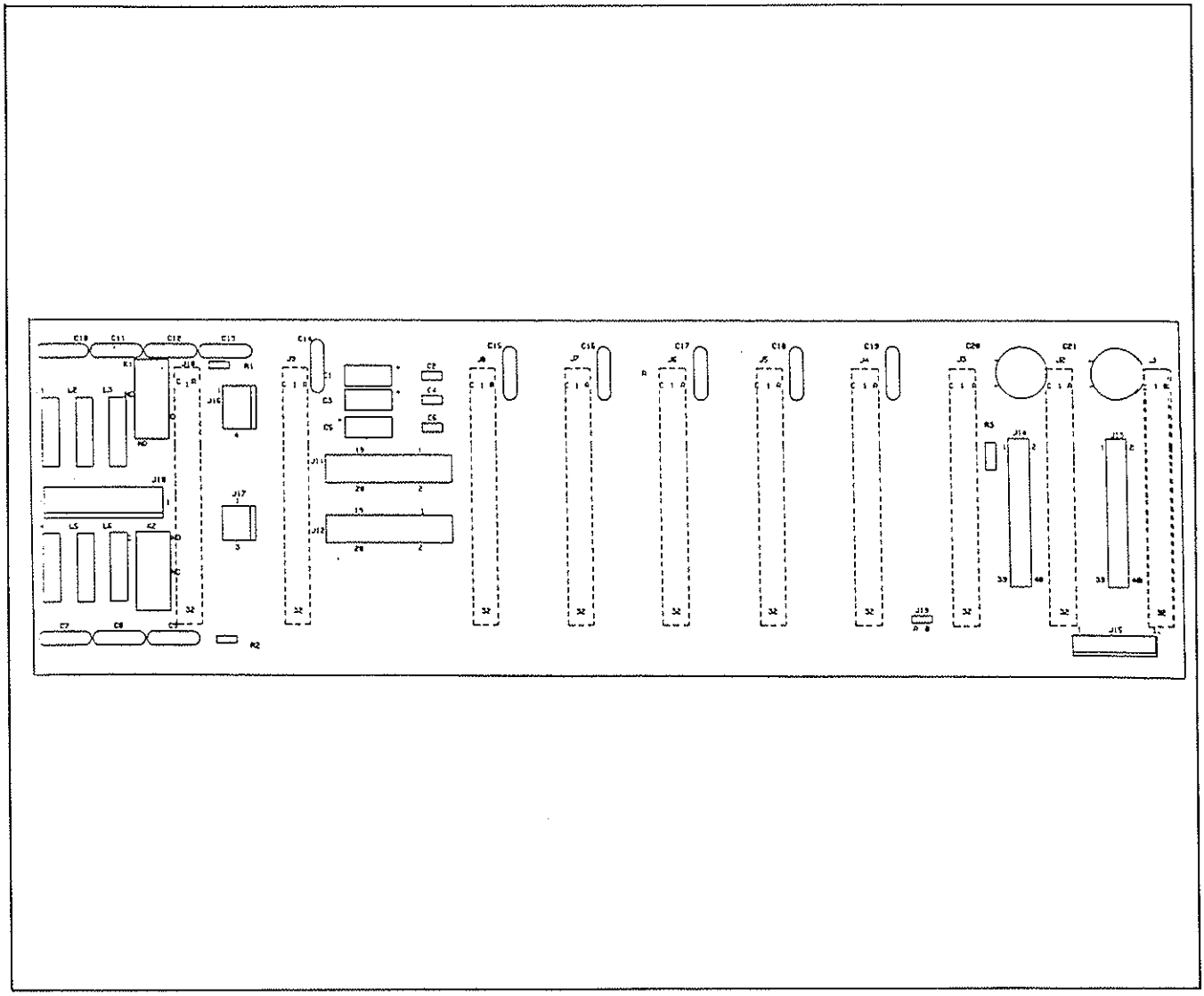
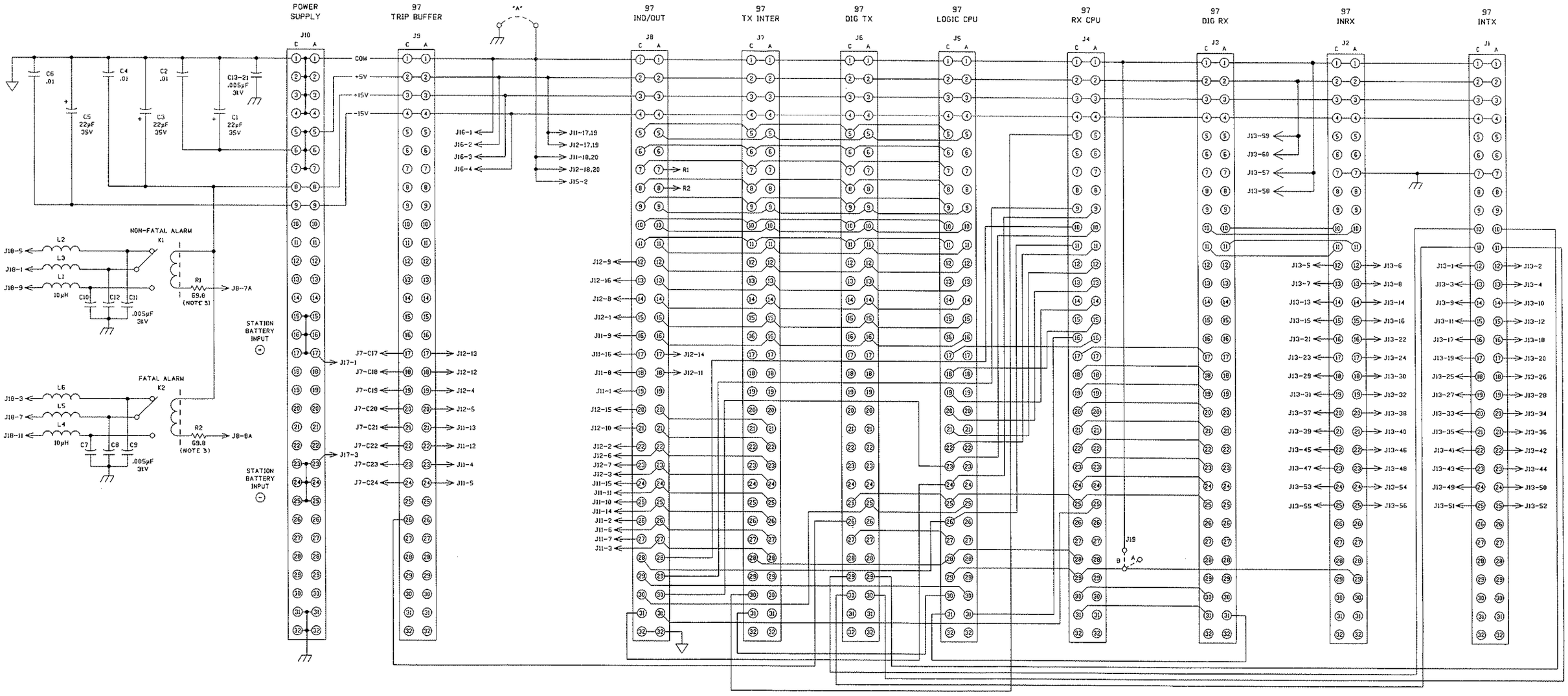


Figure 17-1. Component locator drawing, RFL 97 INTER Interconnect Motherboard (Assembly No. 101580-5; Drawing No. D-101583, Rev. C)



NOTES:

1. CHASSIS GROUND CONNECTION IS MADE THROUGH 97 INTER MOUNTING SCREWS.
2. J19 IS IN POSITION "A" IN FIBER OPTIC SYSTEMS ONLY.
3. R1 & R2 MAY BE ZERO OHMS IF RELAY WITH 275 OHM COIL IS USED.

Figure 17-2. Schematic, RFL 97 INTER Interconnect Motherboard (Assembly No. 101580-5; Schematic No. D-101584-5, Rev. B)

17.4. RFL 97 449 INTER RS-449 INTERFACE PANEL

The RFL 97 449 INTER RS-449 Interface Panel (Fig. 17-3) is used in 56-Kbps RFL 9700 terminals that are not equipped with fiber optic modules or heads. It allows the RFL 97A DIG TX 56 Digital Transmitter Module and the RFL 97A DIG RX 56 Digital Receiver Module to be connected directly to an RS-449 link.

The RFL 97 449 INTER has a male 37-pin D-subminiature connector (DC-37), which mates with any standard female RS-449 connector. It mounts at the rear of the RFL 9700, in the space normally occupied by the fiber optic heads.

A schematic for the RFL 97 449 INTER appears in Figure 17-5.

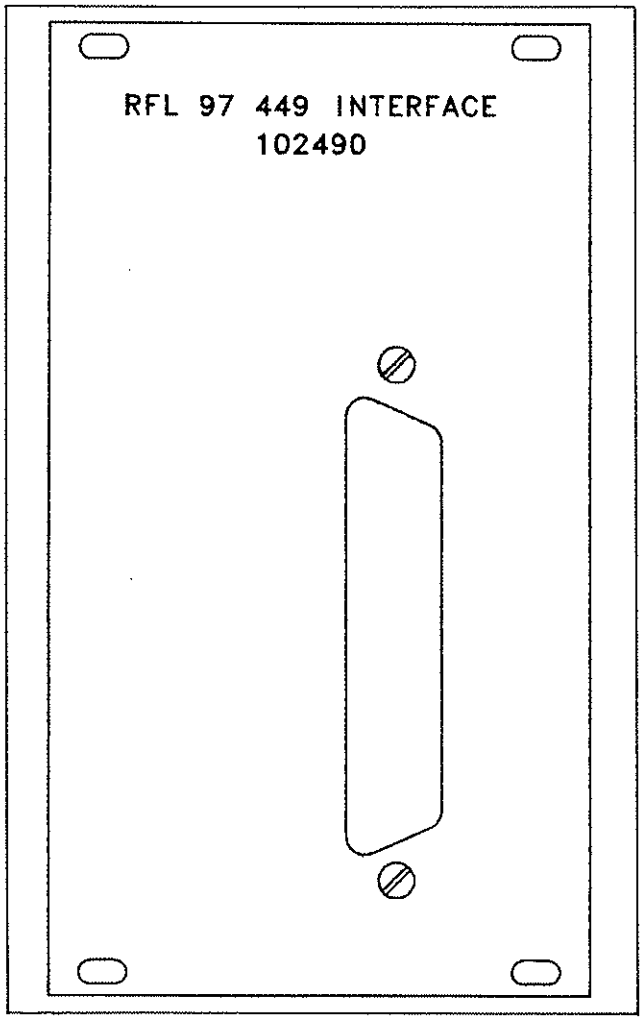


Figure 17-3. RFL 97 449 INTER RS-449 Interface Panel

17.5. RFL 97 X.21 INTER CCITT X.21 INTERFACE PANEL

The RFL 97 X.21 INTER Interface Panel (Fig. 17-4) is used in all 64-Kbps RFL 9700 terminals. It allows the RFL 97A DIG TX 64 Digital Transmitter Module and the RFL 97A DIG RX 64 Digital Receiver Module to be connected directly to a CCITT X.21 link.

The RFL 97 X.21 INTER has a male 15-pin D-subminiature connector (DA-15), which mates with any standard female CCITT X.21 connector. It mounts at the rear of the RFL 9700, in the space normally occupied by the fiber optic heads.

A schematic for the RFL 97 X.21 INTER appears in Figure 17-6.

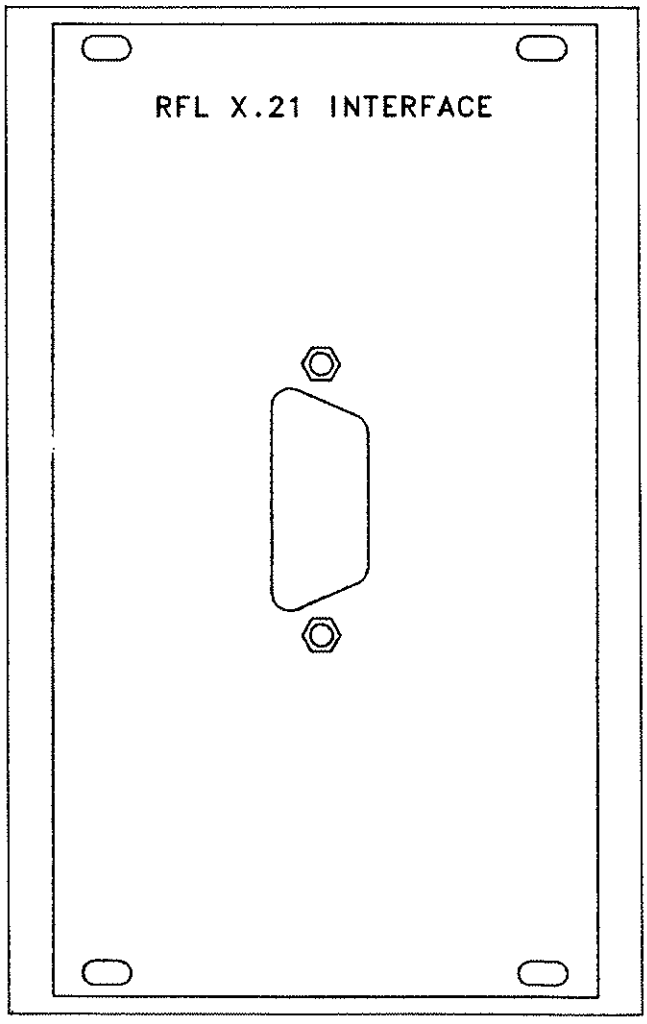


Figure 17-4. RFL 97 X.21 INTER CCITT X.21 Interface Panel

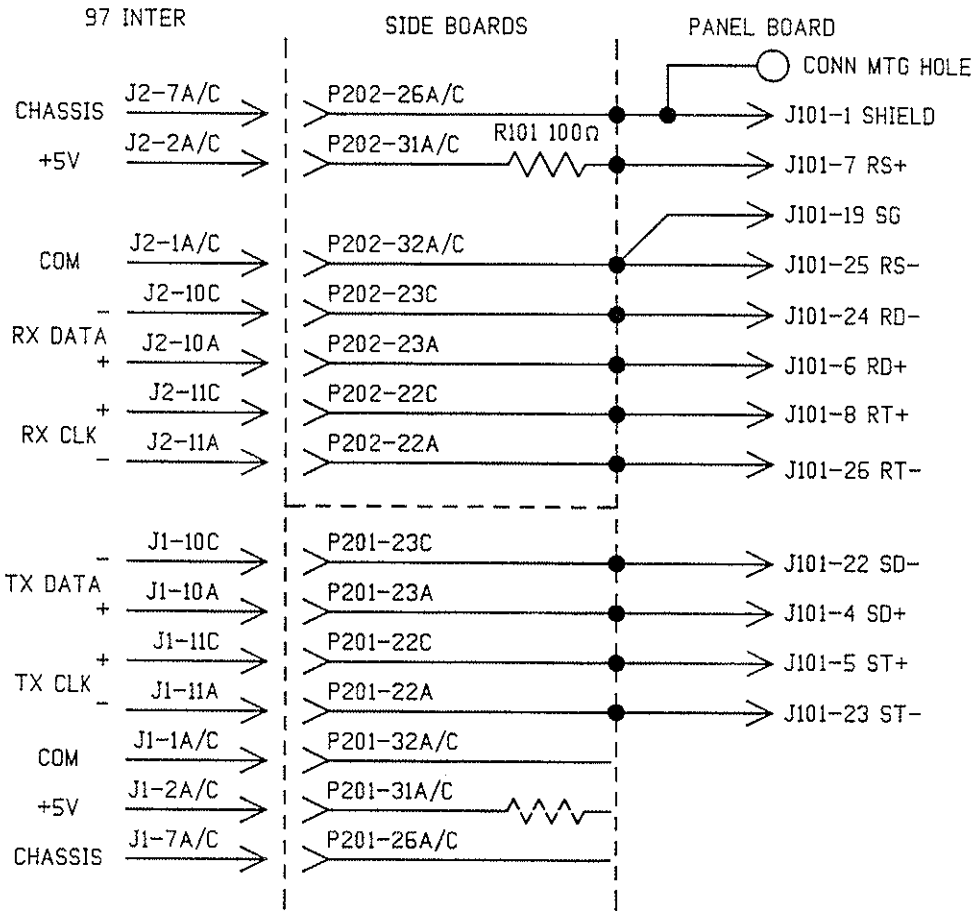
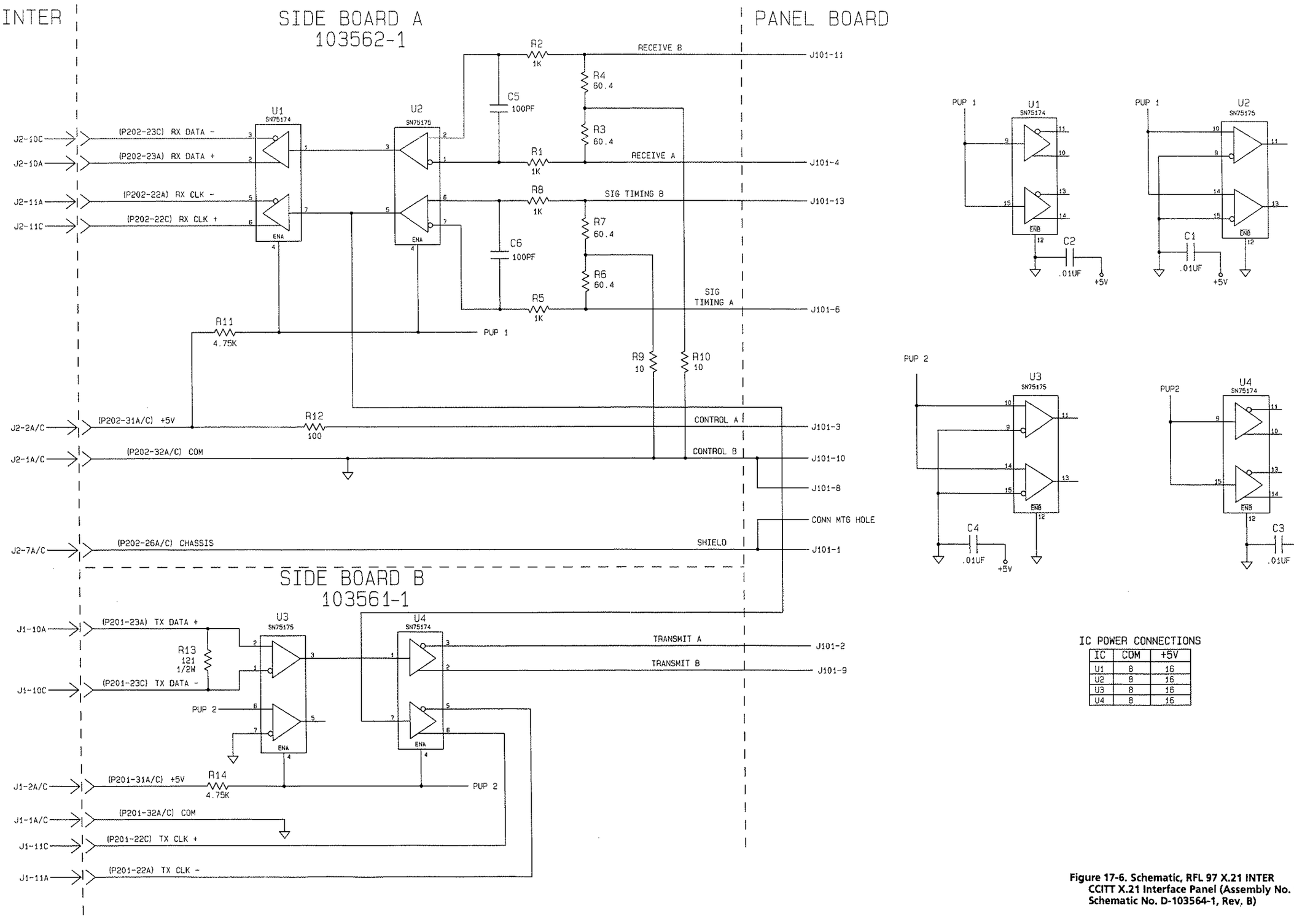


Figure 17-5. Schematic, RFL 97 449 INTER RS-449 Interface Panel (Assembly No. 102490; Schematic No. B-102494, Rev. A)



IC POWER CONNECTIONS

IC	COM	+5V
U1	8	16
U2	8	16
U3	8	16
U4	8	16

Figure 17-6. Schematic, RFL 97 X.21 INTER CCITT X.21 Interface Panel (Assembly No. 103560; Schematic No. D-103564-1, Rev. B)

Section 18. ACCESSORY EQUIPMENT

18.1. INTRODUCTION

This section describes some of the accessory equipment which can be used with the RFL 9700 Digital Protection Channel to perform useful auxiliary functions. If your RFL 9700 system is equipped with any accessory items, additional information for these items will be found later in this section. This may include Instruction data Sheets, schematics, wiring diagrams, or other documents.

18.2. RFL 97 449 MUX RS-449 MULTIPLEXER PANEL

The RFL 97 449 MUX RS-449 Multiplexer Panel is used to connect seven RS-449 devices to the fiber optic transmitter and receiver modules in the RFL 9700. This allows eight RS-449-compatible devices (including the RFL 9700) to communicate over a single fiber optic link.

In order to use the RFL 97 449 MUX, the RFL 9700 must be equipped with an RFL 97 FO INTX-1 Eight-Input Fiber Optic Transmitter Module, and an RFL 97 FO INRX-1 Eight-Output Fiber Optic Receiver Module.

18.3. AUXILIARY VOICE/DATA SYSTEM

The Auxiliary Voice/Data System allows voice and RS-232 data signals to be interfaced with the RFL 9700. Paragraphs 18.4.1 through 18.4.3 describe the different parts of the Auxiliary Voice/Data System.

18.3.1. RFL 97 VOICE Voice Module

The RFL 97 VOICE Voice Module converts voice signals into 56-Kbps synchronous RS-422 data. The voice signals can come from a handset or a two-wire or four-wire telephone interface. It can also convert received data back into voice signals at the other end of the communications link. It contains a full-duplex coder/decoder (codec) with built-in filters, signaling circuits for push-to-call or E & M applications, and amplifier circuits for two-wire or four-wire interfacing and sidetone generation.

18.3.2. RFL 97 DATA Data Module

The RFL 97 DATA Data Module can convert one or two channels of RS-232 data to RS-422 signal levels; this will enable this data to be interfaced to the RFL 9700. It will also convert the data back to RS-232 levels at the receiving end. Data can be processed at speeds up to 9600 baud.

18.3.3. RFL 97 1U CHAS Chassis

The RFL 97 1U CHAS is a 1U chassis designed to hold three modules. Any combination of RFL 97 VOICE or RFL 97 DATA modules can be accommodated. It occupies 1.75 inches of vertical rack space, and is connected to the RFL 9700 by a 60-conductor ribbon cable, which provides all power and data connections for the modules housed in the RFL 97 1U CHAS.

18.4. RFL 97 FOS FIBER OPTIC SWITCH

The RFL 97 FOS Fiber Optic Switch allows an RFL 9700 to be simultaneously applied over two different fiber optic cables. Under normal system operation, communications are made through the primary fiber optic cable. If a communication alarm is received from the terminal equipment, the RFL 97 FOS automatically redirects communications onto the standby fiber optic cable. The RFL 97 FOS can also receive SWITCH commands from any remote source.

The RFL 97 FOS is a passive device under normal operating conditions. The transmitter path is passed through a passive splitter, so signals applied at the input will always be present at the two output ports. This is important because if the RFL 97 FOS fails, all that is lost is the ability to redirect the optic signals.

LED indicators are provided for diagnostic purposes. These indicators show which optic path is active. In addition, a Form C relay is provided for remote indication of the active optic path. The standby output indication can be used to signal a remote alarm that the RFL 97 FOS has switched to the standby fiber.

The RFL 97 FOS is a double-Euro module that is normally mounted in a 19-inch wide flat-pack chassis (1.75 inches high, or 1RU).