INSTRUCTION MANUAL

RFL 9300
Charge Comparison System

U.S. Patent Nos. 4,939,617, 5,111,358, and 5,150,270
(Foreign Patents Pending)

NOTICE

The information in this manual is proprietary and confidential to RFL Electronics Inc. Any reproduction or distribution of this manual, in whole or part, is expressly prohibited, unless written permission is given by RFL Electronics Inc.

This manual has been compiled and checked for accuracy. The information in this manual does not constitute a warranty of performance. RFL Electronics Inc. reserves the right to revise this manual and make changes to its contents from time to time. We assume no liability for losses incurred as a result of out-of-date or incorrect information contained in this manual.

RFL Electronics Inc.
353 Powerville Road ● Boonton Twp., NJ 07005-9151 USA
Tel: 973.334.3100 ● Fax: 973.334.3863
Email: sales@rflelect.com ● www.rflelect.com

Publication Number MC9301C
Printed in U.S.A.
Revised September 5, 2007

WARRANTY

The RFL 9300 comes with a ten-year warranty from date of shipment for replacement of any part which fails during normal operation. RFL will repair or, at its option, replace components that prove to be defective at no cost to the Customer. All equipment returned to RFL Electronics Inc. must have an RMA (Return Material Authorization) number, obtained by calling the RFL Customer Service Department. A defective part should be returned to the factory, shipping charges prepaid, for repair or replacement FOB Boonton, N.J.

RFL Electronics Inc. is not responsible for warranty of peripherals, such as printers and external computers. The warranty for such devices is as stated by the original equipment manufacturer. If you have purchased peripheral equipment not manufactured by RFL, follow the written instructions supplied with that equipment for warranty information and how to obtain service.

WARRANTY STATEMENT

The RFL 9300 is warranted against defects in material and workmanship for ten years from the date of shipment. During the warranty period, RFL will repair or, at its option, replace components that prove to be defective at no cost to the customer, except the one-way shipping cost of the failed assembly to the RFL Customer Service facility in Boonton, New Jersey. RFL warrants product repair from the one-year from the date of repair or the balance of the original factory warranty, whichever is longer.

This warranty does not apply if the equipment has been damaged by accident, neglect, misuse, or causes other than performed or authorized by RFL Electronics Inc.

This warranty specifically excludes damage incurred in shipment to or from RFL. In the event an item is received in damaged condition, the carrier should be notified immediately. All claims for such damage should be filed with the carrier.

NOTE

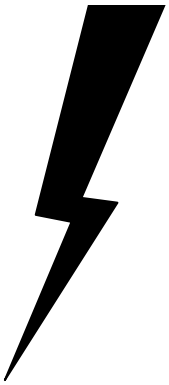
If you do not intend to use the product immediately, it is recommended that it be opened immediately after receiving and inspected for proper operation and signs of impact damage.

This warranty is in lieu of all other warranties, whether expressed, implied or statutory, including but not limited to implied warranties of merchantability and fitness for a particular purpose. In no event shall RFL be liable, whether in contract, in tort, or on any other basis, for any damages sustained by the customer or any other person arising from or related to loss of use, failure or interruption in the operation of any products, or delay in maintenance or for incidental, consequential, indirect, or special damages or liabilities, or for loss of revenue, loss of business, or other financial loss arising out of or in connection with the sale, lease, maintenance, use, performance, failure, or interruption of the products.

CAUTION

FOR YOUR SAFETY

THE INSTALLATION, OPERATION, AND MAINTENANCE OF THIS EQUIPMENT SHOULD ONLY BE PERFORMED BY QUALIFIED PERSONS.



WARNING:

The equipment described in this manual contains high voltage. Exercise due care during operation and servicing. Read the safety summary on the reverse of this page

SAFETY SUMMARY

The following safety precautions must be observed at all times during operation, service, and repair of this equipment. Failure to comply with these precautions, or with specific warnings elsewhere in this manual, violates safety standards of design, manufacture, and intended use of this product. RFL Electronics Inc. assumes no liability for failure to comply with these requirements.

GROUND THE CHASSIS



The chassis must be grounded to reduce shock hazard and allow the equipment to perform properly. Equipment supplied with three-wire ac power cables must be plugged into an approved three-contact electric outlet. All other equipment is provided with a rear-panel ground terminal, which must be connected to a proper electrical ground by suitable cabling. Refer to the wiring diagram for the chassis or cabinet for the location of the ground terminal.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE OR IN WET OR DAMP AREAS

Do not operate the product in the presence of flammable gases or fumes, or in any area that is wet or damp. Operating any electrical equipment under these conditions can result in a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS



Operating personnel should never remove covers. Component replacement and internal adjustments must be done by qualified service personnel. Before attempting any work inside the product, disconnect it from the power source and discharge the circuit by temporarily grounding it. This will remove any dangerous voltages that may still be present after power is removed.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT

Because of the danger of introducing additional hazards, do not install substitute parts or make unauthorized modifications to the equipment. The product may be returned to RFL for service and repair, to ensure that all safety features are maintained.

READ THE MANUAL



Operators should read this manual before attempting to use the equipment, to learn how to use it properly and safely. Service personnel must be properly trained and have the proper tools and equipment before attempting to make adjustments or repairs.

Service personnel must recognize that whenever work is being done on the product, there is a potential electrical shock hazard and appropriate protection measures must be taken. Electrical shock can result in serious injury, because it can cause unconsciousness, cardiac arrest, and brain damage.

Throughout this manual, warnings appear before procedures that are potentially dangerous, and cautions appear before procedures that may result in equipment damage if not performed properly. The instructions contained in these warnings and cautions must be followed exactly.

TABLE OF CONTENTS

TABLE OF CONTENTS v
LIST OF ILLUSTRATIONS ix
LIST OF TABLES xiv

SECTION 1: PRODUCT INFORMATION 1

SECTION 2: SYSTEM OPERATION 1
2.1 INTRODUCTION 1
2.2 SYSTEM INITIALIZATION 1
2.3 COMMUNICATIONS CONTROLLER MODULE 4
2.4 CHANNEL IMPAIRMENT CHARACTERISTICS 6
2.5 SUPERVISOR CONTROLLER 9
2.6 AUXILIARY CURRENT TRANSFORMER (ACT) 12
2.7 PHASE CONTROLLERS 12
2.8 BACKUP MODE OPERATION 25
2.9 DIRECT TRANSFER TRIP (DTT) 26
2.10 DISPLAY CONTROLLER 26
2.11 OSCILLOGRAPHY BOARD 30
2.12 IRIG-B 30
2.13 DIAGNOSTICS 30

SECTION 3: APPLICATIONS 1
3.1 INTRODUCTION 1
3.2 SERIES COMPENSATED LINES 1
3.3 VERY SHORT LINES 3
3.4 EFFECT OF INFEED/OUTFEED 4
3.5 STRONG BUS TIE 4
3.6 HIGH-RESISTANCE GROUND FAULT 5
3.7 PREFAULT LOAD SUBTRACTION 6
3.8 ULTRA HIGH-SPEED TRIPPING 9
3.9 SATURATED MAIN CURRENT TRANSFORMERS 11
3.10 WEAK INFEED APPLICATIONS 15
3.11 RECLOSE BLOCKING FOR THREE-PHASE FAULTS 16
3.12 UNDERGROUND CABLES 16
3.13 STUB-BUS PROTECTION 18
3.14 TAPPED LOAD 20
3.15 OPEN CONDUCTOR WITH SINGLE LINE-TO-GROUND FAULT 25
3.16 OPEN CONDUCTOR WITHOUT SINGLE LINE-TO-GROUND FAULT 29

SECTION 4: SETTING GUIDELINES 1
4.1 INTRODUCTION 1
4.2 PROGRAMMABLE PARAMETERS 1

SECTION 5: INSTALLATION 1
5.1 INTRODUCTION 1
5.2 UNPACKING 1
5.3 MOUNTING 2
5.4 VENTILATION 5
5.5 ELECTRICAL CONNECTIONS 5
5.6 MODEM CONNECTIONS 10
5.7 FIBER OPTIC CONNECTIONS 11
5.8 DIRECT DIGITAL CONNECTIONS 11
5.9 IRIG-B CLOCK CONNECTIONS 11

SECTION 6: FAMILIARIZATION 1
6.1 INTRODUCTION 1
6.2 CONTROLS AND INDICATORS 1
6.3 START-UP PROCEDURES 1
6.4 DISPLAY MODES 14
6.5 ACCESSING THE RFL 9300 FROM A PC OR TERMINAL 32
6.6 RFL 9300 ADDRESSING 61
6.7 DESCRIPTION OF INSTANTANEOUS OVERCURRENT BACKUP TRIP ALGORITHM and INVERSE TIME OVERCURRENT BACKUP TRIP ALGORITHM 64
6.8 TIME-OVERCURRENT CURVE EQUATIONS 67

SECTION 7: LABORATORY ACCEPTANCE TESTS 1
7.1 INTRODUCTION 1
7.2 EQUIPMENT REQUIREMENTS 1
7.3 SYSTEM SETUP 2
7.4 TEST PROCEDURES 4

SECTION 8: FIELD COMMISSIONING 1
8.1 INTRODUCTION 2
8.2 SINGLE-RELAY TESTS (optional) 2
8.3 VERIFICATION OF END-TO-END COMMUNICATIONS 18
8.4 STARTUP MODE 22
8.5 FINAL COMMISSIONING 38

SECTION 9: DISPLAY MODULE 1
9.1 INTRODUCTION 1
9.2 DISPLAY CONTROLLER BOARD 1
9.3 OSCILLOGRAPHY BOARD 6
9.4 FRONT PANEL 9

SECTION 10: SUPERVISOR CONTROLLER MODULE 1
10.1 DESCRIPTION 1
10.2 CONTROLS AND INDICATORS 1
10.3 THEORY OF OPERATION 3

SECTION 11: AUXILIARY CURRENT TRANSFORMER I/O MODULE 1
11.1 DESCRIPTION 1
11.2 CONTROLS AND INDICATORS 1
11.3 THEORY OF OPERATION 2

SECTION 12: PHASE CONTROLLER MODULE 1
12.1 DESCRIPTION 1
12.2 CONTROLS AND INDICATORS 1
12.3 THEORY OF OPERATION 3

SECTION 13: COMMUNICATIONS CONTROLLER MODULE 1
13.1 DESCRIPTION 1
13.2 CONTROLS AND INDICATORS 1
13.3 THEORY OF OPERATION 3

SECTION 14: MODEM MODULE 1
14.1 DESCRIPTION 1
14.2 CONTROLS AND INDICATORS 1
14.3 THEORY OF OPERATION 3

SECTION 15: LINE COUPLER I/O MODULE 1
15.1 DESCRIPTION 1
15.2 CONTROLS AND INDICATORS 1
15.3 THEORY OF OPERATION 2

SECTION 16: DIRECT DIGITAL INTERFACE I/O MODULE 1
16.1 DESCRIPTION 1
16.2 CONTROLS AND INDICATORS 1
16.3 THEORY OF OPERATION 3

SECTION 17: SINGLE WIDTH FIBER OPTIC TRANSCEIVER MODULE 1
17.1 INTRODUCTION 1
17.2 DESCRIPTION 2
17.3 SPECIFICATIONS 2
17.4 CONTROLS AND INDICATORS 4
17.5 THEORY OF OPERATION 6

SECTION 18: SINGLE WIDTH FIBER OPTIC I/O MODULE 1
18.1 INTRODUCTION 2
18.2 DESCRIPTION 3
18.3 SPECIFICATIONS 3
18.4 CONTROLS AND INDICATORS 4
18.5 THEORY OF OPERATION 7

SECTION 19: POWER SUPPLY MODULE 1
19.1 DESCRIPTION 1
19.2 SPECIFICATIONS 2
19.3 THEORY OF OPERATION 3

SECTION 20: RELAY I/O MODULE 1
20.1 DESCRIPTION 1
20.2 CONTROLS AND INDICATORS 1
20.3 THEORY OF OPERATION 5

SECTION 21. ALARM I/O MODULE 1
21.1 DESCRIPTION 1
21.2 CONTROLS AND INDICATORS 1
21.3 THEORY OF OPERATION 4

SECTION 22. SHORT HAUL FIBER INTERFACE MODULE AND FIBER SERVICE UNIT 1
22.1 INTRODUCTION 2
22.2 SHORT HAUL FIBER INTERFACE MODULE 3
22.3 FIBER SERVICE UNIT 5

SECTION 23: G.703 INTERFACE I/O MODULE 1
23.1 DESCRIPTION 1
23.2 CONTROLS AND INDICATORS 1
23.3 THEORY OF OPERATION 3

SECTION 24: SINGLE POLE CHASSIS 1
24.1 DESCRIPTION 1
24.2 CONROLS AND INDICATORS 1
24.3 THEORY OF OPERATION - HARDWARE 6
24.4 THEORY OF OPERATION - SOFTWARE 8

SECTION 25. CHASSIS AND FRONT PANEL RS-232 MODULE 1
25.1 DESCRIPTION 1
25.2 FRONT PANEL RS-232 INTERFACE MODULE 2

SECTION 26: EXPANSION CHASSIS 1

SECTION 27. PROTOCOL CONVERTERS 1
27.1 DESCRIPTION 1
27.2 CONFIGURATIONS 1
27.3 CONVERTER OPERATION 2
27.4 9300 SETUP 2
27.5 CONVERTER ADDRESS SELECTION 2
27.6 SPECIFICATIONS 2
27.7 CONNECTIONS 3
27.8 CABLES 3
27.9 TERMINAL BLOCK PINOUTS 3
27.10 BLOCK DIAGRAM 4
27.11 MODBUS MAP (Version A3, M13, 9/12/01) 5
27.12 DNP PROFILE DOCUMENT 10
27.13 DNP POINT LIST (Version A1,M13,8/3/01) 12

SECTION 28. MAINTENANCE 1
28.1 INTRODUCTION 1
28.2 ALARM CODES 1
28.3 REMOVAL AND REPLACEMENT 3
28.4 FUSE REPLACEMENT 5
28.5 CORRECTIVE MAINTENANCE 6
28.6 HOW TO ARRANGE FOR SERVICING 6
28.7 INSTRUCTIONS FOR CONVERTING A 3-TERMINAL 9300 TO A 2-TERMINAL 9300 7

SECTION 29: MODEM APPLICATION INFORMATION 1
29.1 INTRODUCTION 1
29.2 TRANSMITTER LEVELS AND WIRING 1
29.3 RECEIVER LEVELS AND WIRING 1
29.4 S/N RATIO VS DEPENDABILITY 1
29.5 TELEPHONE SERVICE REQUIREMENTS 3
29.6 MICROWAVE, RADIO, AND T1 ANALOG CHANNELS 3
29.7 CHANNEL ROUTING VS DEPENDABILITY 3
29.8 MODEM SECURITY 3
29.9 SQUELCH RULES 3
29.10 CHANNEL DELAY LIMITS 6
29.11 TEST POINTS 7

SECTION 30: GLOSSARY OF TERMS 1

SECTION 31: INDEX 1

SECTION 32: SCHEMATICS 1

Application Notes

LIST OF ILLUSTRATIONS

Figure 2-1. Block diagram, RFL 9300 Charge Comparison System (two terminal) 2
Figure 2-2. Logic diagram, composite fault detector 14
Figure 2-3. Logic diagram, strong-feed trips (for 2- and 3- terminal systems) 15
Figure 2-4. Differential Characteristics for 9300 in 2- and 3- terminal modes 16
Figure 2-5. Logic diagram, weak-feed trip (for 2- and 3- terminal systems) 18
Figure 2-6. Logic diagram, switch-into-fault with communications (2- and 3- terminal systems) 19
Figure 2-7. Logic diagram, ultra high-speed trip 20
Figure 2-8. Logic diagram for open conductor and loss of load algorithm 21
Figure 2-9. Logic diagram, stub-bus applications 23
Figure 2-10. Logic diagram, switch-into-fault without communications 25
Figure 2-11. Logic diagram, trip seal-in 28
Figure 2-12. Logic diagram, DTT trip seal-in 29

Figure 3-1. Voltage inversion 2
Figure 3-2. Phase unbalance 2
Figure 3-3. High source-to-line impedance ratio 3
Figure 3-4. Effect of infeed/outfeed 4
Figure 3-5. Strong bus tie 4
Figure 3-6. High-resistance ground fault with heavy through-load, causing an outfeed condition 5
Figure 3-7. Polar diagram, ... 5
Figure 3-8. Prefault load subtraction eliminates generator angles 7
Figure 3-9. Currents before pre-fault subtraction 8
Figure 3-10. Currents after pre-fault subtraction 8
Figure 3- 11. Operation of the RFL 9300's UHS circuit during an internal fault 10
Figure 3-12. Operation of the RFL 9300's UHS circuit during and external fault 10
Figure 3-13. Saturated main current transformers during close-in internal fault 11
Figure 3-14. External fault with very severe CT saturation at one end 13
Figure 3-15. Weak infeed application 15
Figure 3-16. Double line-to-ground (DLG) fault 17
Figure 3-17. Sub-bus protection 19
Figure 3-18. Typical tapped line application 20
Figure 3-19. Transformer in-rush 21
Figure 3-20. Zero-sequence current flows through transformer 22
Figure 3-21. Typical tapped line application 22
Figure 3-22. Open conductor with two single-line-to-ground faults (OC/2-SLG) 25
Figure 3-23. Open conductor with one single-line-to-ground fault (OC/SLG) 26
Figure 3-24. Phasor analysis of ground strong-feed operation, based on a load current of 0.5 amperes or more, with the SLG fault occurring on the load sending end side of the open conductor 27
Figure 3-25. Phasor analysis of ground strong-feed operation, based on a load current of 0.5 amperes or more, with the SLG fault occurring on the load receiving end side of the open conductor 28
Figure 3-26. Open conductor without single-line-to-ground fault 29
Figure 3-27. Possible miscoordination of loss-of-load plus Zone 2 timer 30

Figure 5-1. Mounting dimensions of RFL 9300 chassis without single pole option 3
Figure 5-2. Mounting dimensions of RFL 9300 chassis with single pole option 4
Figure 5-3. Rear view, typical RFL 9300 Charge Comparison System 6
Figure 5-4. Electrical connections between RFL 9300 and current transformers on protected line 7
Figure 5-5. Electrical connections between RFL 9300 with optional test switch chassis and current transformers on protected line 8
Figure 5-6. Overview of a typical 9300 two-terminal installation 9
Figure 5-7. Overview of a typical RFL 9300 three-terminal installation 9

Figure 6-1. Controls and indicators, typical three-terminal RFL 9300 Charge Comparison System 2
Figure 6-2. The RFL 9300 keypad 4
Figure 6-3. RFL 9300 module position numbers 6
Figure 6-4. Front Panel RS-232 cable connections. 32
Figure 6-5. Cable connections between RFL 9300 and PC or terminal using XON/XOFF handshaking 33
Figure 6-6. APRIL commands for use with RFL 9300 (for two-terminal and three-terminal mode) 35
Figure 6-7. Typical alarm display for two-terminal mode 36
Figure 6-8. Typical alarm display for three-terminal mode 37
Figure 6-9. Typical values display for two-terminal mode 39
Figure 6-10. Typical values display for three-terminal mode 39
Figure 6-11. Typical read settings menu for two-terminal single-pole mode 41
Figure 6-12. Typical read settings menu for two-terminal three-pole mode 42
Figure 6-13. Typical read settings menu for three-terminal single-pole mode 43
Figure 6-14. Typical read settings menu for three-terminal three-pole mode 43
Figure 6-15. Typical configuration and software version display for two-terminal and three-terminal systems 44
Figure 6-16. Typical Remote Parameters Display for a two-terminal single-pole system 45
Figure 6-17. Typical Remote Parameters Display for a two-terminal three-pole system 45
Figure 6-18. Typical Remote Parameters Display for a three-terminal single-pole system 46
Figure 6-19. Typical Remote Parameters Display for a three-terminal three-pole system 47
Figure 6-20. Typical UPDATE screen for a two-terminal system 51
Figure 6-21. Typical UPDATE screen for a three-terminal system 51
Figure 6- 22. Sequence of events menu 52
Figure 6-23. Typical alarm sequence of events display – page 1 53
Figure 6-24. Typical alarm sequence of events display – page 2 53
Figure 6-25. Typical trip sequence of events display – page 1 54
Figure 6-26. Typical Oscillography data table 54
Figure 6-27. A typical oscillography data plot 56
Figure 6-28. Typical programming menu 57
Figure 6-29. Typical parameter settings list for a three-terminal system 58
Figure 6-30. A typical two-terminal installation where addressing is required 61
Figure 6-31. A typical two-terminal installation where addressing is not required 62
Figure 6-32. Typical RFL 9300 three-terminal addressing scheme 63
Figure 6-33. Time Curve USA 1 69
Figure 6-34. Time Curve USA 2 70
Figure 6-35. Time Curve USA 3 71
Figure 6-36. Time Curve USA 4 72
Figure 6-37. Time Curve IEC 1 73
Figure 6-38. Time Curve IEC 2 74
Figure 6-39. Time Curve IEC 3 75
Figure 6-40. Time Curve IEC 4 76

Figure 7-1. Back-to-back relay, test setups 3
Figure 7-2. Test connections simulating an external A-G fault 8
Figure 7-3. Test connections simulating an external A-B fault 10
Figure 7-4. Test connections simulating an external three-phase fault 10
Figure 7-5. Phasor diagram, single-phase test simulation of an external three-phase fault 11
Figure 7-6. Phasor diagram, real external three-phase fault 11
Figure 7-7. Test connections simulating an internal A-G fault 12
Figure 7-8. Test connections simulating an internal A-B fault 15
Figure 7-9. Test connections simulating an internal three-phase fault 16
Figure 7-10. Test connections simulating an internal A-G fault with weak infeed at the right terminal 17
Figure 7-11. Test connections simulating an internal A-G fault with breaker open at the right terminal 19
Figure 7-12. Test connections for oscillography test 21
Figure 7-13. Oscillography Test data plot 22

Figure 8-1. Single relay test setups 4
Figure 8-2. Test connections simulating an internal A-G fault 12
Figure 8-3. Test connections simulating an internal A-B fault 15
Figure 8-4. Test connections simulating an internal three-phase fault 16
Figure 8-5. Electrical connections between RFL 9300 and current transformers on protected line 27
Figure 8-6. Correctly wired two-terminal system 31
Figure 8-7. Phase inversion at remote 1 relay 31
Figure 8-8. Phase inversion at local relay 32
Figure 8-9. Correctly wired three-terminal system 33
Figure 8-10. Phase inversion at remote 2 34
Figure 8-11. Phase inversion at remote 1 35
Figure 8-12. Phase inversion at local station 36

Figure 9-1. RFL 9300 display module for horizontal chassis 1
Figure 9-2. Controls and indicators for display controller board, used in RFL 9300 display module 3
Figure 9-3. Controls and indicators for oscillography board, used in RFL 93B DISPLAY module 7
Figure 9-4. Component locator drawing for display controller board, used in RFL 9300 display module 12
Figure 9-5. Component locator drawing for oscillography board, used in RFL 9300 display module 15
Figure 9-6. Component locator drawing for front panel assembly, used in RFL 9300 display module 17
Figure 9-7. Oscillography Board, part of RFL 9300 display module (Assembly No. 106330; Schematic No. D-106764-A) Sheets 1 of 5 through 5 of 5 18

Figure 10-1. RFL 9300 supervisor controller module 1
Figure 10-2. Controls and indicators, RFL 9300 supervisor controller module 2
Figure 10-3. Component locator drawing, supervisor controller modules for RFL 9300 12
Figure 10-4. Supervisor Controller module for RFL 9300 Charge Comparison System(Assembly No. 106300; Schematic No. D-106304-1-B) Sheets 1 of 2 and 2 of 2 13

Figure 11-1. RFL 93B ACT I/O Auxiliary Current Transformer I/O Module 1
Figure 11-2. Controls and indicators, RFL 93B ACT I/O Auxiliary Current Transformer I/O Module 2
Figure 11-3. Block diagram, RFL 93B ACT I/O Auxiliary Current Transformer I/O Module 3
Figure 11-4. Component locator drawing, RFL 93B ACT-5 5-Ampere Auxiliary Current Transformer I/O Module 6
Figure 11-5. RFL 93B ACT-5 5-Ampere Auxiliary Current Transformer I/O Module (Assembly No. 106345; Schematic No. D-105814, Rev. C) 7

Figure 12-1. RFL 9300 phase controller module 1
Figure 12-2. Controls and indicators, RFL 9300 phase controller modules 2
Figure 12-3. Component locator drawing, phase controller modules for RFL 9300 Charge Comparison System 7
Figure 12-4. Phase Controller modules for RFL 9300 Charge Comparison System (Assembly No. 106370; Schematic No. D-103819, Rev. D) Sheets 1 of 2 an 2 of 2 8

Figure 13-1. RFL 9300 communications controller module 1
Figure 13-2. Controls and indicators, RFL 9300 communications controller module 2
Figure 13-3. Block diagram, RFL 9300 communications controller module 4
Figure 13-4. Transmitter timing diagram, RFL 9300 communications controller module 7
Figure 13-5. Receiver timing diagram, RFL 9300 communications controller module 8
Figure 13-6. Logic diagram for programmable logic device U24 10
Figure 13-7. Component locator drawing, communications controller module for RFL 9300 13
Figure 13-8. Communications Controller modules for RFL 9300 Charge Comparison System (Assembly No. 106365; Schematic No. D-103824, Rev. A) Sheets 1 of 2 and 2 and 2 14

Figure 14-1. RFL 9300 modem module 1
Figure 14-2. Controls and indicators, RFL 9300 modem module 2
Figure 14-3. Component locator drawing, modem module for RFL 9300 Charge Comparison System 8
Figure 14-4. Modem module for RFL 9300 Charge Comparison System (Assembly No. 106355; Schematic No. D-103829, Rev. B) 9

Figure 15-1. RFL 93 LC I/O Line Couple I/O Module 1
Figure 15-2. Component locator drawing, RFL 93 LC I/O Line Couple I/O Module 3
Figure 15-3. RFL 93 LC I/O Line Coupler I/O Module 4

Figure 16-1. RFL 93 DD I/O Direct Digital Interface I/O Module 1
Figure 16-2. Controls and indicators, RFL 93 DD Direct Digital I/O Module 2
Figure 16-3. Component locator drawing, RFL 93 DD I/O Direct Digital I/O Module 5
Figure 16-4. RFL 93 DD I/O Direct Digital I/O Module (Assembly No. 103830-1; Schematic No. D-103834-1, Rev. A) .. 6

Figure 17-1. RFL 93 B FT/FR Single width fiber optic transceiver module 1
Figure 17-2. Controls and indicators, RFL 93B FT/FR single width fiber optic transceiver mode 5
Figure 17-3. Block diagram, RFL 93B FT/FR single width fiber optic transceiver module 7
Figure 17-4. RFL 9300 Fiber Optics Hot Standby Signal Routing Diagram 8
Figure 17-5. Component locator drawing, RFL 93B FT/FR single width fiber optic transceiver module 11
Figure 17-6. RFL 93 FT/FR Singlewidth Fiber Optic Transceiver Module (Assembly No. 106360; Schematic No. D-105849, Rev. B) 12

Figure 18-1. Typical RFL 93 FT/FR single width fiber optic I/O module 2
Figure 18-2. Controls and indicators, RFL 93 FT/FR I/O-8M single width fiber optic I/O module 4
Figure 18-3. Controls and indicators, RFL 93 FT/FR I/O-13S and 13 M single width fiber optic I/O modules 5
Figure 18-4. Controls and indicators, RFL 93 FT/FR I/O-13SL and 15SL single width fiber optic I/O modules 6
Figure 18-5. Block diagram, RFL 93 FT/FR I/O-8M 850 nm Multimode Fiber Optic I/O Module 7
Figure 18-6. Block diagram, RFL 93 FT/FR-13M (Multimode) and RFL 93 FT/FR-S (Singlemode) 1300-nm Fiber Optic I/O Module 9
Figure 18-7. Block diagram, RFL 93 FT/FR 13SL (1300-nm Singlemode) and RFL 93 FT/FR 15SL (1550-nm Singlemode) 11
Figure 18-8. Component locator drawing, RFL 93 FT/FR I/O-8M 850-nm Multimode Singlewidth Fiber Optic I/O Module (Assembly No. 105850; Drawing No. 105853-A) 15
Figure 18-9. RFL 93 FT/FR Singlewidth Fiber Optic I/O Module -8M (Assembly No. 105850; Schematic No. D-105854, Rev. D) 16
Figure 18-10. Component locator drawing, RFL 93 FT/FR I/O-3M and RFL 93 FT/FR I/O-13S 19
Figure 18-11. RFL 93 FT/FR Singlewidth Fiber Optic I/O Modules, -13M (Assembly No. 105855; Schematic No. D-105864, Rev. A), -13S (Assembly No. 105860; Schematic No. D-105864, Rev. A) 20
Figure 18-12. Component locator drawing, RFL 93 FT/FR I/O-13SL and RFL 93 FT/FR I/O-15SL 23
Figure 18-13. RFL 93 FT/FR Singlewidth Fiber Optic I/O Modules, -13SL (Assembly No. 105865; Schematic No. D-105869, Rev. A), -15SL (Assembly No. 105870; Schematic No. D-105869, Rev. A) 24

Figure 19-1. Typical RFL 9300 power supply module 1
Figure 19-2. Component locator drawings, 50-watt power supply module 6
Figure 19-3. 9300 PS 48/125 DC power supply module for RFL 9300 Charge Comparison System, (Assembly No. 106715-1; Schematic No. 106719-E) 7

Figure 20-1. RFL 93B Relay I/O Module, rear panel 1
Figure 20-2. Rear panel connectors and terminal blocks, RFL 93B Relay I/O Module 2
Figure 20-3. Controls and indicators, power/RF-232 board for RFL 93B Relay I/O Module 3
Figure 20-4. Component locator drawing, RFL 93B Relay I/O module, Power/RS-232 board 8
Figure 20-5. Component locator drawing, RFL 93B Relay I/O module, Current Sense Board 10
Figure 20-6. Component locator drawing, RFL 93B Relay I/O module, Relay Output board 12
Figure 20-7. RFL 93B RELAY I/O module, Power/RS-232 board (Assembly No. 106388-1; Schematic No. D-106389, Rev. D) Sheets 1 of 3 through 3 of 3 13

Figure 21-1. RFL 93 Alarm I/O Module 1
Figure 21-2. Controls and indicators, RFL 93 Alarm I/O Module 2
Figure 21-3. Component locator drawing, RFL 93 Alarm I/O Module, ... 8

Figure 22-1. Front panel view of RFL 93 SH FIBER short haul interface module and RFL FSU fiber service unit 2
Figure 22-2. Controls and indicators, RFL 93 SHFI short haul fiber interface module 4
Figure 22-3. Typical Fiber Service Unit Installation 5
Figure 22-4. Component locator drawing, RFL 93 short haul fiber interface module (Assembly No. 107500) 8
Figure 22-5. Schematic, RFL 93 Short Haul Fiber Module (3 sheets) (Assembly No. 107500; Schematic No. D-107504-C) 9

Figure 23-1. RFL 93 G.703 Interface I/O Module 1
Figure 23-2. Controls and indicators, RFL 93 G.703 Interface I/O Module 2
Figure 23-3. Setting J5 for Normal or Loops Operation 4
Figure 23-4. Component locator drawing, RFL 93 G. 703 Interface I/O Module 8
Figure 23-5. Schematic, RFL 93 G.703 module (Assembly No. 106730; Drawing No. D-106734-B) 9

Figure 24-1. Typical RFL 9300 Single Pole Chassis, front panel view 1
Figure 24-2. Typical RFL 9300 Single Pole Chassis, front panel view showing LED indicators 2
Figure 24-3. Typical RFL 9300 Single Pole Chassis, rear panel view 3
Figure 24-4. Target Message Word sent from the Display Controller to the Single-Pole Chassis 8
Figure 24-5. 16-bit Status messages transmitted by the Single-Pole logic to the Supervisor at 250ms intervals 9
Figure 24-6. Component locator drawing, RFL 9300 single pole chassis, main circuit board 13
Figure 24-7. Schematic, 9300 Single Pole Chassis (Drawing No. D-106714-B) Sheet 1 of 2 14
Figure 24-8. Component locator drawing, RFL 9300 single pole chassis, rear panel 16
Figure 24-9. Schematic, 9300 Single Pole Chassis, Rear Panel (Drawing No. D-106709-C) 17

Figure 25-1. Typical RFL 9300 chassis 1
Figure 25-2. Block diagram of RS-232 front board 2
Figure 25-3. Component locator drawing, RFL 93 INTER Interconnect Motherboard 4
Figure 25-4. RFL 93 INTER Interconnect Motherboard (Assembly No. 103905-1; Schematic No. D-103909-1-D) 5
Figure 25-5. Component locator drawing, RFL 9300 front panel RS-232 module 6
Figure 25-6. RS-232 Front Panel Interface (Assembly No. 106755; Schematic No. C-106759-B) 7

Figure 26-1. Typical RFL 9300 Expansion Chassis, rear view 1
Figure 26-2. Component locator drawing, RFL 9300 expansion chassis power supply (Assembly No. 106350) 2
Figure 26-3. Schematic, Power Converter I/O – 250 Vdc, For RFL 9300 Charge Comparison System 3

Figure 27-1. Protocol converter block diagram 4

Figure 29-1. RFL 9300 modem dependability versus S/N ratio (measured) 2
Figure 29-2. RFL 9300 probability of passing false words (theoretical) 4
Figure 29-3. RFL 9300 modem security (theoretical) 5

LIST OF TABLES

Table 2-1. Valid Hot-Standby Configurations 6

Table 4-1. Programmable parameters, RFL 9300 Two-Terminal Charge Comparison System 2
Table 4-2. Programmable parameters, RFL 9300 Three-Terminal Charge Comparison System..... 3

Table 5-1. Pin assignment for DC-37 connector on RFL 93 DD I/O Direct Digital I/O Module..... 12

Table 6-1. Controls and indicators, typical three-terminal RFL 9300 Charge Comparison System..... 3
Table 6-2. Keypad functions, RFL 9300 Charge Comparison System 4
Table 6-3. RFL 9300 Module, General Information 5
Table 6-4. Alarm codes for Two-Terminal and Three-Terminal RFL 9300 Charge Comparison System 15
Table 6-5. READ mode parameters for RFL 9300 Two-Terminal Charge Comparison Systems..... 19
Table 6-6. READ mode parameters for RFL 9300 Three-Terminal Charge Comparison Systems..... 21
Table 6-7. STARTUP mode parameters for RFL 9300 Two-Terminal Charge Comparison Systems 26
Table 6-8. STARTUP mode parameters for RFL 9300 Three-Terminal Charge Comparison Systems 26
Table 6-9. Programmable parameters, RFL 9300 Two-Terminal Charge Comparison System 28
Table 6-10. Programmable parameters, RFL 9300 Three-Terminal Charge Comparison System..... 29

Table 8-1. Programmable parameters, RFL 9300 Two-Terminal Charge Comparison System 8
Table 8-2. Programmable parameters, RFL 9300 Three-Terminal Charge Comparison System..... 9
Table 8-3. Acceptable received fiber optic power levels, RFL 9300 Charge Comparison System 20
Table 8-4. STARTUP mode parameters for RFL 9300 Two-Terminal Charge Comparison Systems 25
Table 8-5. STARTUP mode parameters for RFL 300 Three-Terminal Charge Comparison Systems 25

Table 9-1. RFL 93B Display Module, general information 2
Table 9-2. Replaceable parts for display controller board, used in RFL 9300 display module. (Assembly No. 106325-2). 10
Table 9-3. Replaceable parts for oscillography board, used in RFL 9300 display modules (Assembly No. 106330)..... 13
Table 9-4. Replaceable parts for front panel assembly, used in RFL 9300 display module (Assembly No. 106335)..... 16

Table 10-1. Replaceable parts, supervisor controller module for RFL 9300 10

Table 11-1. Replaceable parts, RFL 93B ACT-5 5-Ampere Auxiliary Current Transformer to I/O Module..... 4

Table 12-1. Replaceable parts, phase controller modules for RFL 9300 Charge Comparison System..... 5

Table 13-1. Replaceable parts, communications controller modules for RFL 9300 Charge Comparison System 11

Table 14-1. Replaceable parts, modem modules for RFL 9300 Charge Comparison System 6

Table 15-1. Replaceable parts, RFL 93 LC I/O Line Coupler I/O Module..... 2

Table 16-1. Replaceable parts, RFL 93 DD I/O Direct Digital Interface I/O Module..... 4

Table 17-1. Replaceable parts, RFL 93B FT/FR single width fiber optic transceiver module. 9

Table 18-1. Differences between Single Width Fiber Optic I/O Modules..... 3
Table 18-2. Replaceable parts, RFL 93 FT/FR I/O-8M Singlewidth fiber optic I/O module 13
Table 18-3. Replaceable parts, RFL 93 FT/FR I/O Singlewidth fiber optic I/O modules 17
Table 18-4. Replaceable parts, Singlewidth fiber optic I/O modules..... 21

Table 19-1. 9300 Power Supply Specifications 2
Table 19-2. Replaceable parts, 50-watt power supply module for RFL 9300 Charge Comparison System 4

Table 20-1. Replaceable parts, RFL 93B Relay I/O, Power/RS-232 board 7
Table 20-2. Replaceable parts, RFL 93 Relay I/O module, Current Sense board 9
Table 20-3. Replaceable parts, RFL 93 Relay I/O module, Relay Output board 11

Table 21-1. Replaceable parts, RFL 93 Alarm I/O Module. 5
Table 21-2. Replaceable parts, RFL 93 Alarm I/O Module. 6

Table 22-1. General Information, Short Haul Fiber Interface Module 3
Table 22-2. Replaceable parts, RFL 93 SHFI short haul fiber interface module 6

Table 23-1. Replaceable parts, RFL 93 G.703 Interface I/O Module 6

Table 24-1. RFL 9300 Single Pole Chassis, General Information 1
Table 24-2. Replaceable parts, RFL 9300 single pole chassis 12
Table 24-3. Replaceable parts, RFL 9300 single pole chassis, rear panel assembly 15

Table 25-1. Replaceable parts, RFL 93 INTER Interconnected Motherboard 3
Table 25-2. Replaceable parts, RFL 9300 front panel RS-232 interface module 6

Table 26-1. Expansion Chassis, General Information 1
Table 26-2. Replaceable parts, RFL 9300 expansion chassis power supply 2

Table 27-1. Protocol Converters currently available 1
Table 27-2. Modbus Map 5
Table 27-3. Modbus RTU Format Table 9
Table 27-4. POINT LIST FOR: 16 bit Analog without Flag (Object 30 Var 4) 12
Table 27-5. POINT LIST FOR: Binary Input Change with Tim (Object 02 Var 2) 13
Table 27-6. POINT LIST FOR: 16 bit Analog With Time (Object 32 Var 4) 14
Table 27-7. POINT LIST FOR: 16 bit Analog Output Status (Object 40 Var 2) 14
Table 27-8. Format Table 15

Table 28-1. Fuse replacement data, RFL 9300 power supply module 6

LIST OF EFFECTIVE PAGES

When revisions are made to the RFL 9300 Instruction Manual, the entire section where revisions were made is replaced. For the edition of this manual dated September 5, 2007, the sections are dated as follows:

Front Matter	September 5, 2007
Section 1	June, 2002
Section 2	October 29, 2001
Section 3	August 25, 2000
Section 4	August 9, 2001
Section 5	October 20, 2004
Section 6	January 30, 2002
Section 7	October 20, 2004
Section 8	October 20, 2004
Section 9	August 9, 2001
Section 10	October 29, 2001
Section 11	March 26, 1999
Section 12	March 26, 1999
Section 13	February 7, 2000
Section 14	May 1, 1998
Section 15	May 1, 1998
Section 16	May 1, 1998
Section 17	May 1, 1998
Section 18	January 19, 2005
Section 19	May 5, 2002
Section 20	May 5, 2002
Section 21	May 5, 2002
Section 22	October 20, 2004
Section 23	February 7, 2000
Section 24	August 25, 2000
Section 25	May 5, 2002
Section 26	February 7, 2000
Section 27	October 20, 2004
Section 28	May 5, 2002
Section 29	May 5, 2002
Section 30	May 5, 2002
Section 31	May 5, 2002
Section 32	September 5, 2007

REVISION RECORD

Rev	Description	Date	Approval
06-15-97	New Document Release (updated manual to three-terminal operation)	06-15-97	CS
10-01-97	Sections 2, 3 and 4 revised in accordance with new engineering Documentation	10-01-97	CS
12-15-97	Sections 6 and 8 revised in accordance with new engineering documentation, Added time-overcurrent parameters.	12-18-97	CS
04-15-98	Added Time Overcurrent function to Sections 6 and 8. Added warning “to prevent potential mis-operation” to the first page of Section 8.	09-16-98	CS
05-01-98	Added solid front panel, Added new product information sheet (Section 1), Added new relay I/O module, Added ne section on expansion chassis, Deleted sections on double width modules, Deleted all references to vertical mount chassis, Updated glossary, and other miscellaneous corrections.	10-21-98	CS
11-30-98	Added new Section 22 on Short Haul Fiber Interface module and Fiber Service Unit. Shifted existing Sections 22 through 27 up by one section number to Sections 23 through 28.	11-30-98	CS
03-26-99	Revised in accordance with ECO No. 9300-160 as follows: Added new pre-fault buffer switching algorithm, added new stub-bus function, synchronized clock to line frequency, and revised trip release algorithm to improve security.	04-03-99	CS
02-07-00	Revised in accordance with ECO No. 9300-208 (200ms limit, revised Section 2). Revised in accordance with RFA No. 6569 (Updated Section 22). Added new Section 23 (G.703 Interface I/O), added new Section 24 (Single Pole Tripping) and shifted existing Sections 23 through 28 up by two section numbers to Sections 25 to 30. Added Table 2-1, Valid Hot-Standby Configurations.	05-17-00	CS
08-25-00	Revised Sections 0, 1, 2, 3, 4, 6, 8, 9, 10, 24 and 25 in accordance with new software documentation. Revised in accordance with ECO Nos. 9300-220, -225 and –226.	08-25-00	CS
10-27-00	Revised Sections 0, 6, 7, 8, 9, and 27 in accordance with new engineering documentation.	10-27-00	CS

8-9-01	Added RS-232 connector to front panel in accordance with ECO No. 9300-253. Revised the following sections: 0, 4, 5, 6, 7, 9 and 25.	8-9-01	CS
10-29-01	Revised in accordance with new engineering documentation as follows: Revised Hot-Standby Configurations Table (Table 2-1), in Section 2, added new schematic to Section 10, revised parts list in Section 10.	11-2-001	CS
1-30-02	Revised in accordance with ECO No. 9300-266: added 24 Volt version of 93 Alarm I/O to Section 21. Revised the following Section: 0, 6, 21. Revised in accordance with CAR # C9300-0061: deleted RTS/CTS references from Section 6.	3-12-02	CS
5-5-02	Added new Section on Protocol Converters. Changed existing sections 27 to 30 to new section numbers 28 to 31. Revised Section 5 in accordance with ECO No. 9300-260. Revised Section 19 (new schematic revision). Revised Section 20 in accordance with CAR# C9300-0056 Revised Section 21 in accordance with ECO No. 9300-254 & 272. Revised Section 22 in accordance with ECO No. 9300-276 & 279. (deleted old and added new SHFI and FSU). Revised Section 25 (new motherboard schematic and assy. no.) Revised Section 28 in accordance with CAR# C9300-0083 (added 3T to 2T conversion instructions).	5-5-02	CS
12-15-02	Revised Sections 7 & 8 in accordance with CAR#.C9300-0089. Revised Section 22 in accordance with a note from BH on 1-28-03 (Changed Tx level to –19dBm on page 22-2)	12-15-02	CS
10-20-04	Incorporated Errata sheet MC9301C-001 dated 11-05-03. See CAR# C9300-0122. (Revised Section 27) Incorporated Errata sheet MC9301C-002 dated 11-11-03. See CAR# C9300-0124. (Revised Section 27) Incorporated Errata sheet MC9301C-003 dated 1-29-04. See CAR# C9300-0126. (Revised Sections 7 and 8) Incorporated Errata sheet MC9301C-004 dated 5-10-04. See CAR# C9300-0132. (Revised Section 22) Incorporated Errata sheet MC9301C-005 dated 6-01-04. See ECO No. MISC-505. (Revised Sections 5, 18 and 22) Incorporated Errata sheet MC9301C-006 dated 10-08-04. See CAR# C9300-0089, and note from BH dated 1-28-03. (Revised Sections 7 and 22) **Note: 15 Manuals printed at (10-20-04) incorporating the above changes to meet shipping requirement but manual not released at this date.**	10-20-04	CS

4-25-06	Manual released incorporating all changes from 10-20-04 also changes as per ECO 9300-289 with changes to Section 18, Section 32 (Schematics) added to CD version.	4-25-06	TG
9-5-07	Warranty statement changed.	9-5-07	TG

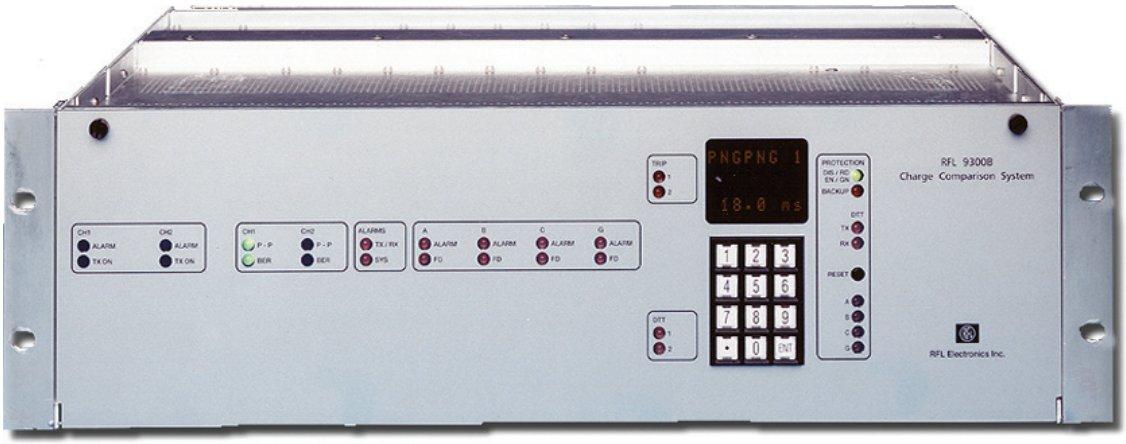
This page intentionally left blank

SECTION 1: PRODUCT INFORMATION

Please see next page.

This page intentionally left blank

RFL 9300



Digital Current Differential Relay

The RFL 9300 Digital Current Differential Relay is a fully-integrated relay/communications terminal, suitable for high-speed protective relaying of overhead or underground AC transmission lines. Lines of all lengths and all voltage levels (with or without series/shunt compensation) are protected. The RFL 9300 Digital Current Differential Relay is applied to two-terminal or three-terminal lines for three-pole or single-pole tripping.

The RFL 9300 does not require any AC line potential, and is unaffected by possible problems associated with the AC source, such as loss of potential due to a blown fuse, or low-potential signals (with a poor S/N ratio).

A typical three-terminal, single channel RFL 9300 system is shown in Figure 2. The major inputs and outputs are shown in this diagram. A block diagram showing all inputs and outputs for a typical RFL 9300 relay is shown in Figure 3.

The RFL 9300 measures the instantaneous value of each phase current and residual (“ground”) current two thousand times per second. The area under the half-cycle current wave is determined by adding these sampled values. The dimension of this area is the “charge”, in ampere-seconds or coulombs. The local and remote charges (for the same half-cycle and for the same phase) are compared, taking poarity into account. If the net charge differs from zero by more than a small threshold level called the “bias”, and internal fault is declared and breaker trip signals are issued. This technique has been patented.

This “Charge Comparison” tripping is called “Strong Feed Trip” or SFT. Two other tripping logic circuits operated in parallel with SFT. These are called “Ultra-High Speed Trip” (UHS) and “Weak Feed Trip” (WFT). UHS and WFT will be described later in this bulletin under “AUXILIARY FUNCTIONS.”

There are two principle advantages of charge comparison compared to current differential relaying:

1. Greatly reduced communications throughput providing enhanced reliability.

2. Precise channel delay compensation is not required, making the RFL 9300 the relay of choice for SDH and SONET applications.

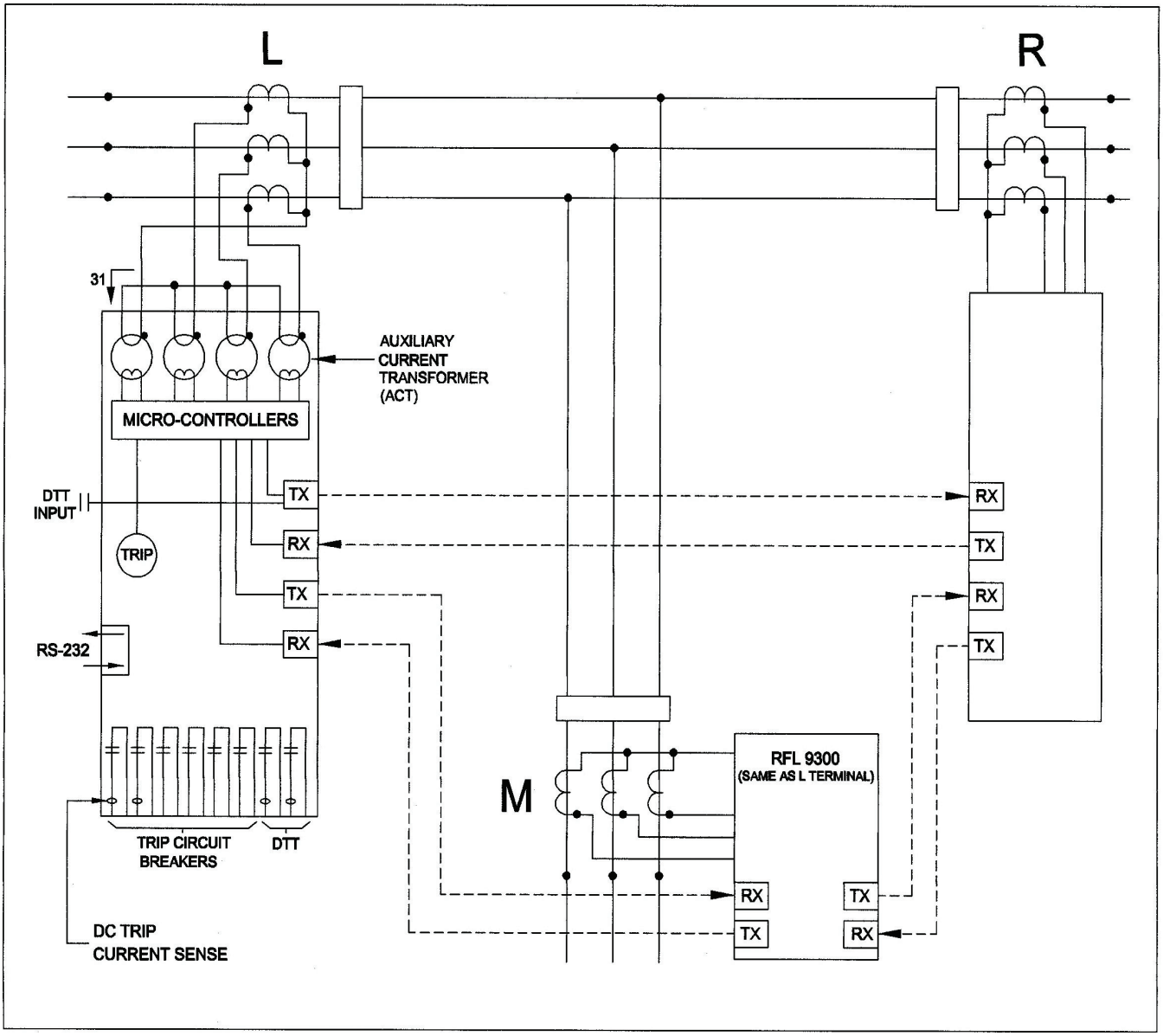


Figure 2. Typical three-terminal (3-pole) RFL 9300 System

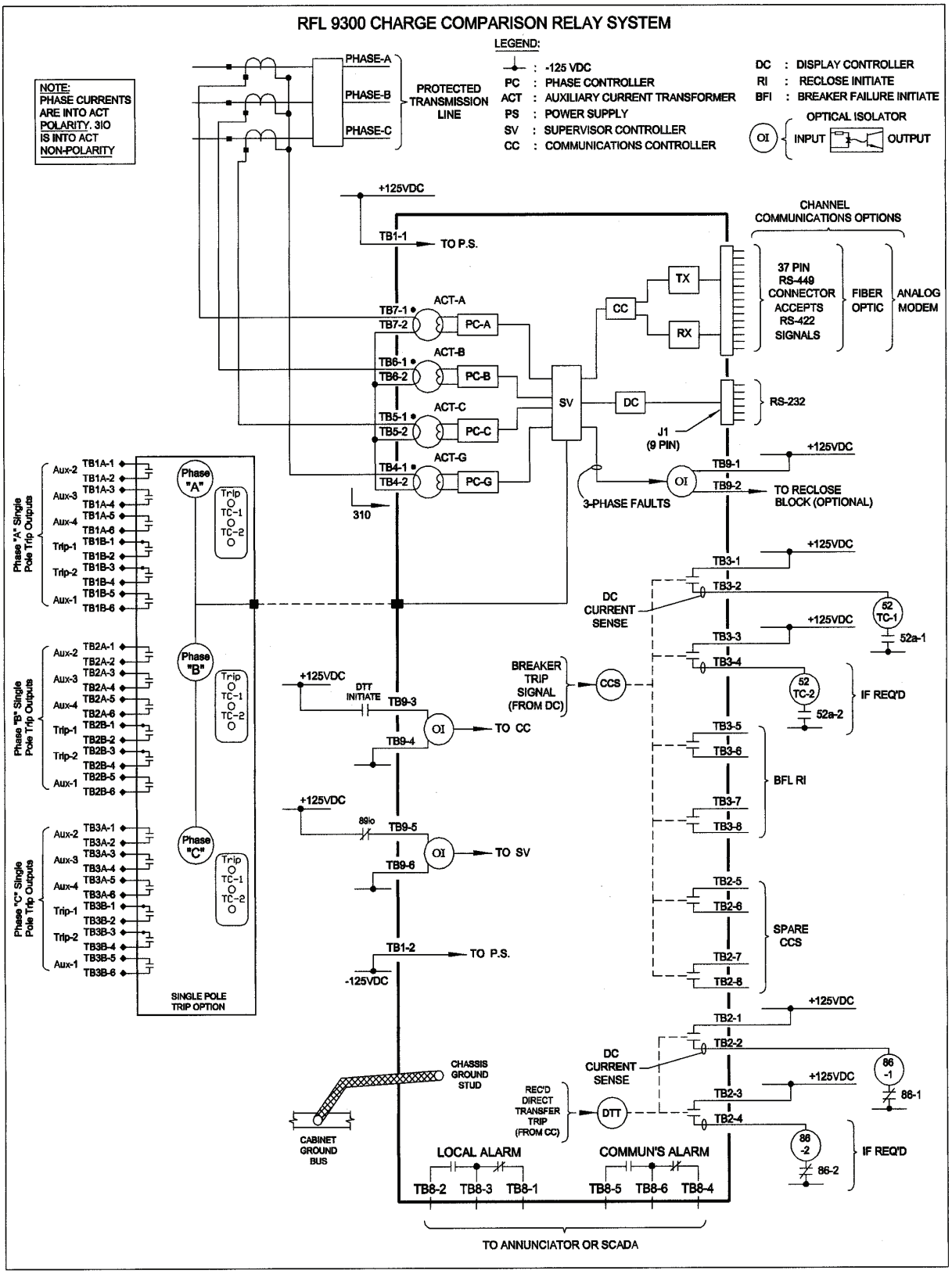


Figure 3. Block diagram, typical (3-pole) RFL 9300 equipped with modem

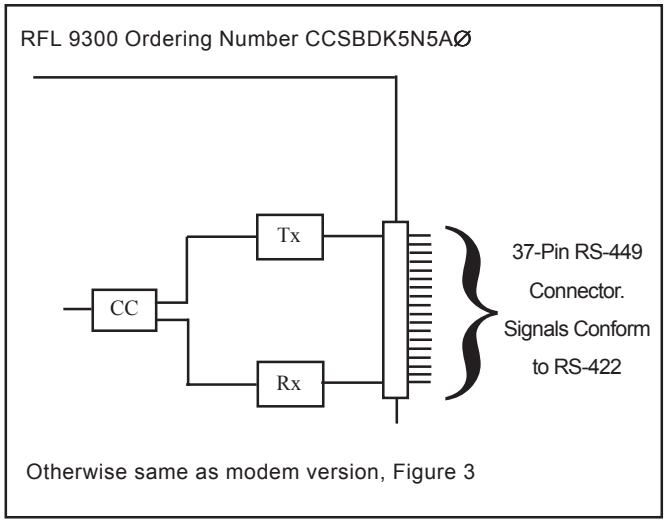


Figure 4. Communication connections for typical RFL 9300 equipped with RS-442 digital interface.

Advantages Per-Phase Protection

The RFL 9300 compares the local current with the remote current on each phase and residual separately. This provides many advantages over the comparison of a single composite quantity:

- Correctly detects the high resistance ground fault with heavy through-load current.
- Provides fault-type identification for targeting.
- Provides optional reclose blocking for three-phase faults.
- Correctly responds to simultaneous faults.
- Redundancy (at least two comparisons sense all internal faults).
- Same phase sensitivity for all fault types.

Single Pole Trip Option

The concept of single pole tripping is to isolate only the faulted phase for single line to ground faults. Combined with single pole reclosing, this relaying technique maintains system stability by retaining synchronization, and reducing the amount of system voltage fluctuation. For persistent single line to ground faults, or multiphase faults, all three poles are tripped.

Because the RFL 9300 Charge Comparison System operates on a per phase basis, it is ideally suited for single pole trip applications. The RFL 9300 correctly identifies the faulted phase by comparing the local, and remote phase currents at both terminals. The faulted phase is tripped locally, and phase specific trip messages are also sent to the opposite terminal.

The relay provides pre phase protection over a single DS0/ 56Kbps synchronous data channel, or a pair of dedicated fiber optic cables. For three terminal line applications, a second communications channel is required. Depending upon the fault conditions, tripping is obtained in 12 to 32 msec. providing almost simultaneous tripping at both terminals.

The single pole trip option is provided in an auxiliary two rack unit chassis that is mounted below the standard RFL 9300 chassis. Six trip rated contacts are provided for each phase, two of which control non-volatile LED trip indicators on the front panel.

Three-Terminal Line Protection

The RFL 9300 is suitable for application on three terminal power lines. The basic operational concepts and setup parameters are largely unchanged for three terminal operation. The practice of prefault load subtraction has been added to enhance the operation under wide generator angles and communication delay compensation errors. Two terminal operation is unchanged from previous versions. Existing relays can be upgraded in the field from two to three terminal capability with an available upgrade kit.

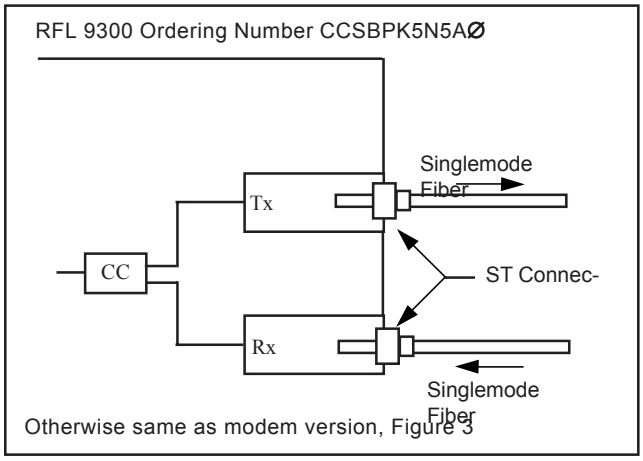


Figure 5. Communication connections for typical

Communication Media

The RFL 9300 is designed to work over the following types of communication links:

- VF channel using a 7200-bps modem. (3-pole model only)
- Direct digital, at either 56 or 64 Kbps.
  - G.703
  - RS-449
  - V.35
  - X.21
- Fiber Optics:
  - 850-nm multimode
  - 1300-nm multimode
  - 1300-nm singlemode (LED or laser)
  - 1550-nm singlemode (laser)
  - 850-nm Short Haul Fiber Interface(ANSI C37.94)

Easy Upgrade from "Voice Frequency to Digital"

The relaying logic software for the modem version (3-pole) is identical to the relaying logic for the wideband versions (Direct Digital or Fiber Optics). The communications logic software is similar, except the wideband versions send each message three times consectutively, and two-out-ofthree voting is done at the receiver terminal to enhance both security and dependability. Since the relaying logic is the same, a field upgrade from modem to wideband is easily accomplished.

Channel Delay Measurement and Compensation

The RFL 9300 continually measures round-trip channel delay time and automatically updates the channel delay compensation. This channel delay compensation and the natural insensitivity of the charge comparison principle to time delays, allows the RFL 9300 Digital Current Differential Relay to tolerate "differential delays" and sudden delay transitions better than other schemes. This is becoming highly desirable with the application of switched ring topology PDH and SDH or SONET systems which can introduce sudden unpredictable delay transactions and or differential delays.

Redundant Communications

In case of channel failure, "hot standby communication" channels ensure continuity of current differential protection. There are two different arrangements for two-terminal lines: single-channel and dual-channel.

TWO-TERMINAL LINE, SINGLE CHANNEL

In the event of a channel failure in one direction, the terminal receiving good information trips on charge comparison. The terminal receiving corrupted information (or no information) trips sequentially on loss-of-load. (This is one of the backup modes described on page 9 of this Product Information Sheet.)

TWO-TERMINAL LINE, DUAL CHANNEL

Figure 6 shows a dual-channel configuration that includes a hot-standby channel. This channel is switched intoservice if the primary channel fails. This transfer does not occur during a fault. Analog channels can not be combined with Digital or Fiber Channels in a Dual Configuration.

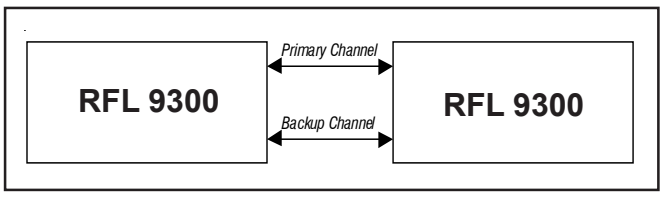


Figure 6. Dual-channel configuration (Analog, Digital, Fiber)

THREE-TERMINAL LINE, SINGLE CHANNEL

Figure 7 shows a three-terminal single channel configuration. In the event of a channel failure, the relay without a comms alarm has sufficient information to send trip signals to the other two, under fault conditions. Communication channel options VF Channel, 56/64 Kbps RS-422, G.703, V.35, X.21 or direct fiber optics in a closed delta path. Leased analog channels cannot be combined with digital, or fiber optic communication channels.

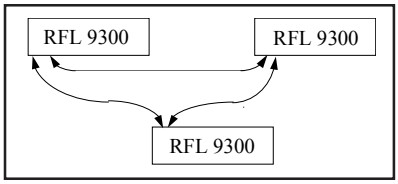


Figure 7. Three-Terminal Line Channel Configuration (Analog, Digital, Fiber)

Flux-Cancellation Auxiliary Current Transformer (ACT)

The phase and residual currents are applied to the RFL 9300 auxiliary current transformers (ACTs) operating at almost zero flux. The ACTs are designed to virtually cancel the core flux (U.S. Patent No. 5,150,270; foreign patents pending).

The RFL 9300's ACTs provide several advantages over conventional ACTs:

1. Very small core size.
2. Virtually no burden presented to the main current transformers (CTs).
3. Totally free of saturation, even for full current offset and very long dc time constant.

This provides extremely high accuracy of transformation over a very wide dynamic range. Figure 8 shows the ACT acting as a "perfect" transformer, even when subjected to repeated tests with the dc offset in the same direction.The ACT is mounted on the ACT I/O Module, shown in Figure 9. A heavy-duty terminal block is provided on the rear of this I/O module for the main CT secondary current connections.

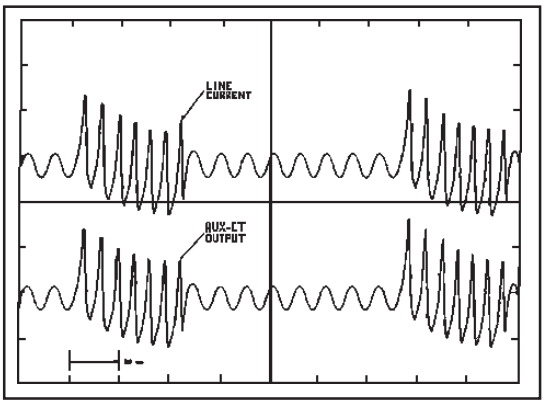


Figure 8. ACT test with full dc offset

System Configuration

The RFL 9300's completely modular design permits several configuration choices. It can be equipped with a direct digital interface, fiber optic modules, or modems for VF channel applications. The RFL 9300 can be configured to operate with 1 AMP or 5 AMP current transformers at line frequencies of either 50 Hz or 60 Hz. For single-pole relaying applications an optional 2 RU chassis is added to the existing RFL 9300. The chassis provides six single-pole Form-A relays.

System configuration can be easily changed or confirmed by viewing the jumpers on the RFL 9300 supervisor controller module. These jumpers can be viewed by lowering the hinged front panel. The available options are 1 AMP or 5 AMP secondary CT ratings, 50 Hz or 60 Hz system frequency, 2 terminal or 3 terminal transmission line, and 3-pole or 1-pole operation.

Operator Interface

A keypad and alphanumeric LED display are provided on the RFL 9300's display module. The operator uses the keyboard and display to read existing settings and measured parameters. By entering a security code, settings can be changed.

LED indicators on the Display Module serve as "targets" to indicate RFL 9300 operations. Non-volatile memory retains the status of these targets in the event of a dc power failure. Remote interrogation is available through an RS-232 port on the rear of the RFL 9300. This port can be connected to any computer with a terminal emulation mode.

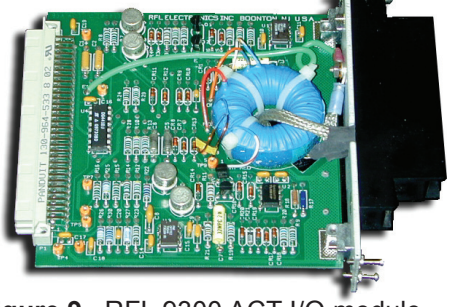


Figure 9. RFL 9300 ACT I/O module

Once connected, our non-proprietary software programming language, Asynchronous Programming and Remote Interrogation Language (APRIL), can be used to read settings, re-program existing settings, or monitor relay target information. A typical APRIL main menu is shown in Figure 11. The RFL 9300's RS-232 port may also be accessed by using the RFL 9660 Digital Switch. For more information about this product, please contact RFL Electronics Inc.

Self-Monitoring

The RFL 9300 continuously performs an 11-point bus test and checks internal communications. It looks for charge differences at trip levels without a resultant fault detector operation. It also checks for abnormal channel behavior, including high bit error rates, improper framing, and incorrect received clock signals. Alarms are issued if a problem is detected.

If a problem affects only one phase (or ground), the affected subsystem is shut down, an alarm is issued, and the RFL 9300 operates on the remaining three subsystems. This arrangement takes maximum advantage of the redundancy that is inherent in the RFL 9300's A/B/C/G configuration.

850nm Short Haul Fiber Interface

In some installations, it may be necessary to install the RFL 9300 relay in a different room, or building, than the communications equipment. To eliminate ground potential rise, and induced voltage interference problems the RFL 9300 can be configured with a Short Haul Fiber Optic Interface. This interface provides a short fiber optic communications path over a pair of dedicated 850 nm multimode fibers. A Fiber Optic Service Unit, mounted at the communications equipment converts the optical signals back into a standard RS-422/ RS-449, V.35,X.21 or G.703 communications signal. See Figure 10.This fiber service unit is compliant to the ANSI C.37.94 specification.

DC Trip Current Sense

The TRIP (breaker trip) and DTT (direct transfer trip) targets only operate if dc trip current is sensed in the output relay contact circuit(s). If the CS+TRIP trip release option is selected, the current sense circuit seals in the CCS trip output contact. The CCS trip contacts remain sealed until the Phase Controlers rescind their trip signal(s) and the DC trip curent is no longer sensed.

If either the TRIP+0 or TRIP+100 trip release options are selected the current sense circuit does not seal-in the CCS trip. Depending on which of these options is selected, the Display Controller will release the trip signal either 0ms or 100ms after the Phase Controller trip signal(s) are no longer detected.The DTT release is not programmable. The Display Controller holds a DTT for a minimum of 100ms after the trip signal ends. The trip is then extednded beyond this point only if the DTT DC trip current is still being sensed.

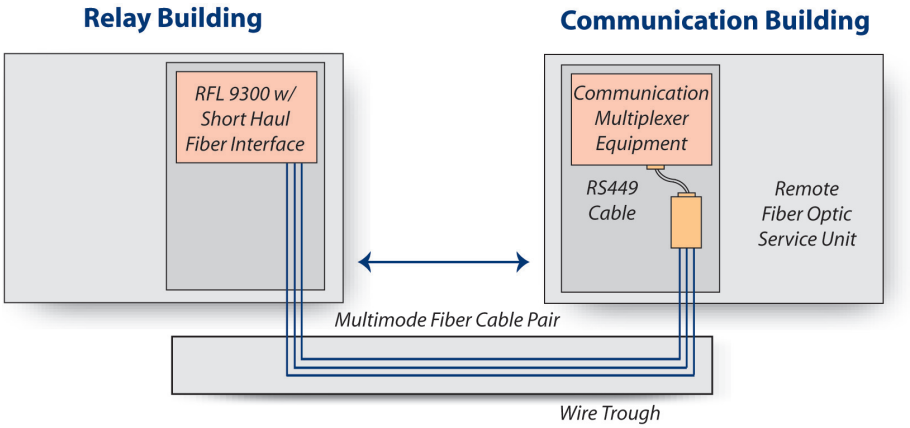


Figure 10. Typical RFL 9300 Short Haul Fiber Optic Application

```
RFL Electronics APRIL (t) Remote Communications, Version 2.1© 1993, 1996
SUBSTATION 12
H    -   Display the main menu
A    -   Go to the alarms display
V    -   Go to the values display
P    -   Go to the programming menu (password required)
D    -   Go to the read settings menu
F    -   Go to the configuration and software version display
K    -   Go to the Remote Parameters display
U    -   Enter the update mode
X    -   Exit the update mode
S    -   Go to sequence-of-events menu
9300>_
```

Figure 11. APRIL commands for use with RFL 9300 (for two-terminal and three-terminal mode)

Oscillography

The oscillography board is an extension of the display controller. It is directly connected to the display controller through an 8-bit bi-directional data bus and additional control lines. When a trip event occurs, the oscillography board will record and store 12 cycles of all four measured currents as well as the trip output signals. Six cycles of pre-trip and six cycles of post trip information will be saved.

The four current signals are read by an 8-bit analog-to-digital converter and kept in a rolling buffer by the controller. In the event of a trip, the buffer is time tagged and a new buffer will be opened. Five buffers are available to store oscillography data for five of the most recent events. Oscillography is displayed on a pc using an external spread sheet such as MS Excel.

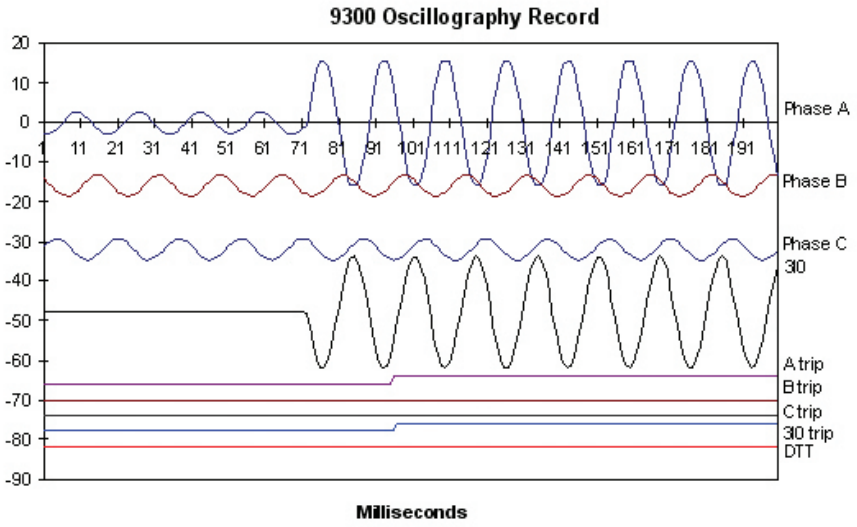


Figure 12. RFL 9300 Oscillography Record.

Auxiliary Functions

The RFL 9300 provides several auxiliary functions, in addition to charge comparison:

ULTRA HIGH-SPEED (UHS) TRIPPING

The UHS signal has priority interrupt whenever the instantaneous current value rises to 170 percent of the nominal current value, and lasts for 2 ms. A received UHS signal provides tripping; unless it is blocked by a local high current value of opposite polarity.

WEAK FEED TRIP (WFT)

This is a logic circuit that looks for a combination of the following:

- A small local current (charge equivalent).
- A moderate or large current (charge equivalent) received from the remote terminal.

An output from this circuit enables local tripping and sends an "echo" permissive signal (called "WFT") to enable tripping at the remote (strong) terminal.

BI-DIRECTIONAL DIRECT TRANSFER TRIP (DTT)

DTT is a high priority signal. The charge comparison function is restored quickly, after a brief interruption by DTT. The DTT signal is maintained with a "refresh" technique that is virtually transparent to the charge comparison. This allows the DTT output to follow the input without interfering with the line protection.

ADDRESSING

Each communication channel in the RFL 9300 is capable of being assigned an unique address. There are 4,063 possible combinations.

FAULT DETECTOR SUPERVISION

Any sudden change in current (such as magnitude or half-cycle duration) will operate a fault detector (FD). Additional steady-state FD's operate based on high current magnitude. Security is enhanced by requiring that at least two Phase Controllers within the system, including the Phase Controller issuing the trip signal, have active fault detectors.

FUNCTIONAL TEST PANEL

The RFL 9300 can be supplied, mounted and wired to a three rack unit functional test panel, part number 104700. The panel is configured with ABB type FT-1 Current and Potential test switches. This provides a convenient means for isolating the relay inputs and outputs as well as measuring system currents during field testing and commissioning.

SEQUENCE-OF-EVENTS LOG

The RFL 9300 Sequence-of-Events Log maintains a list of the last five alarm events and last five trip events. Both the alarm and trip events are time tagged in hours, minutes, seconds and milliseconds. The RFL 9300 contains a real-time battery backed clock, that is automatically synchronized to the IRIG-B signal if it is available.

LOSS-OF-CHANNEL BACK-UP

The following four back-up modes are available:

1. High-Set Overcurrent (selectable option)

This uses separate phase and ground settings that are independent of the charge comparison.

2. Inverse Time Overcurrent (selectable option)

When back-up protection is enabled, the RFL 9300 offers eight totally independent phase and $3I_0$ inverse time overcurrent curves. Eleven different time dial settings are also provided for each of the selected curves.

3. Loss-Of-Load

This provides sequential tripping for all internal faults except three-phase; useful if the channel fails in one direction and not the other.

4. Switch-Into-Fault

This operates when the circuit breaker closes into a faulted line.

Fully Modular Construction

The RFL 9300 is fully modular, front and rear. This provides increased reliability by completely eliminating chassis hand wiring, and makes the RFL 9300 easier to troubleshoot. Spare modules can be stocked instead of the complete relays.

MOUNTING

The 3 pole RFL 9300 is three rack-units high (5.25 inches, or 13.3 cm) and mounts in a standard 19-inch rack or cabinet. The single pole RFL 9300 is five rack-units (8.75 inches, or 22.25 cm) (See Figure 13 for mounting dimensions)

WIRING

Rear views of the RFL 9300 showing terminal assignments for typical systems are shown in Figure 14.

IRIG-B

The RFL 9300 has the ability to synchronize its internal real-time clock with an external IRIG-B clock source. The IRIG-B signal enters the RFL 9300 through a BNC connector on the Relay I/O module. The signal is then routed to the Oscillography Board which demodulates the IRIG-B signal and feeds it to an embedded controller which is also used for the oscillography feature. The controller updates its battery operated real-time clock based on the received IRIG-B signal. In the absence of IRIG-B the APRIL setting of the display clock will be used. The RFL 9300 can accept both modulated and unmodulated IRIG-B signals.

Commissioning Mode Program

Requiring approximately one ampere of load current, the RFL 9300 offers the unique ability to confirm the wiring of the relay.

The program disables all trip outputs, and first confirms that positive phase rotation exists between the currents applied to the “A”, “B” and “C” phase controllers at all terminals.

The second part of the program requires the operator at each terminal to bypass the “A” phase current and produce a $3I_0$ current in the relay. If the $3I_0$ phase controller is correctly wired, a positive phase rotation will be detected between the currents applied to the “B”, “C”, and $3I_0$ phase controllers.

The third and final part of the test, transmits the Charge value of the current in the “A” phase controller between all terminals. Each relay will display the max differential current detected in the system. Correctly wired relays on an untapped transmission line will display zero differential current. Correctly wired relays on a tapped transmission line will display the value of the current drawn by the tap.

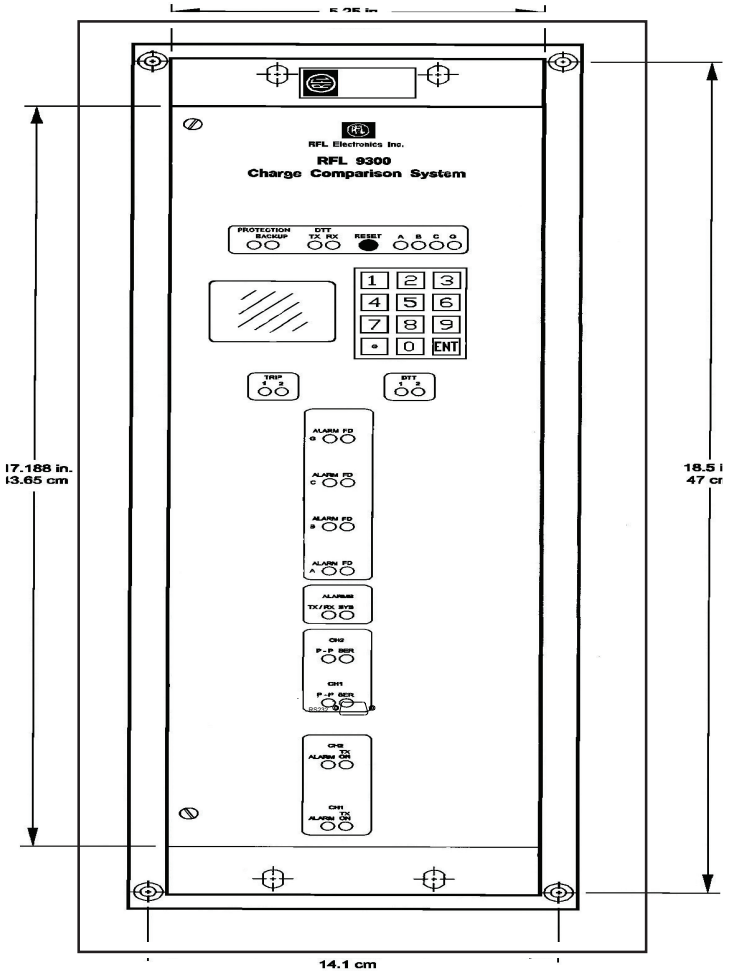


Figure 14. Mounting dimensions, RFL 9300 (3-pole relaying) vertical chassis.

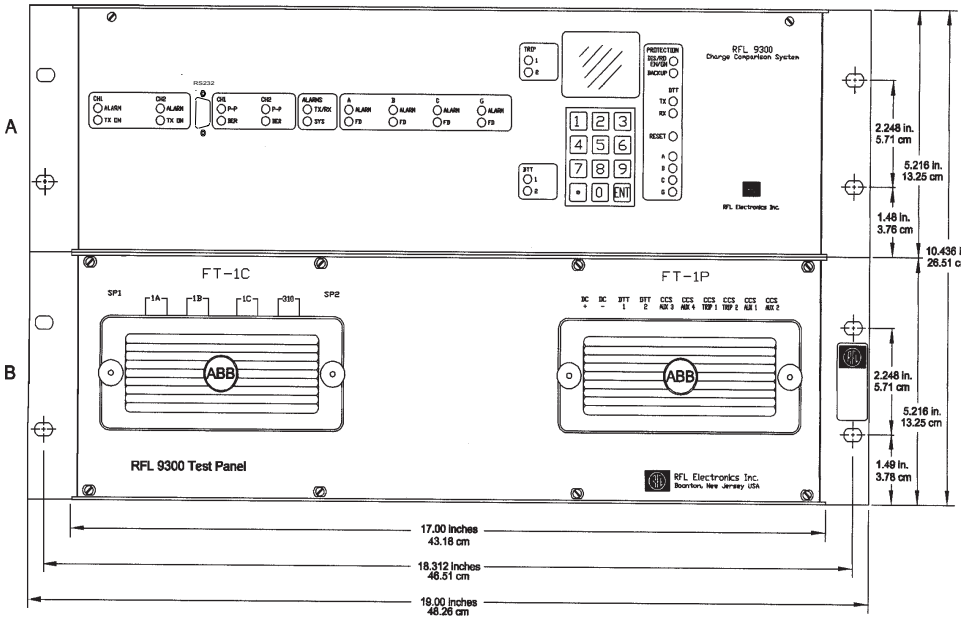


Figure 13. Mounting dimensions, RFL 9300 (3-pole relaying) horizontal chassis with optional functional test panel.

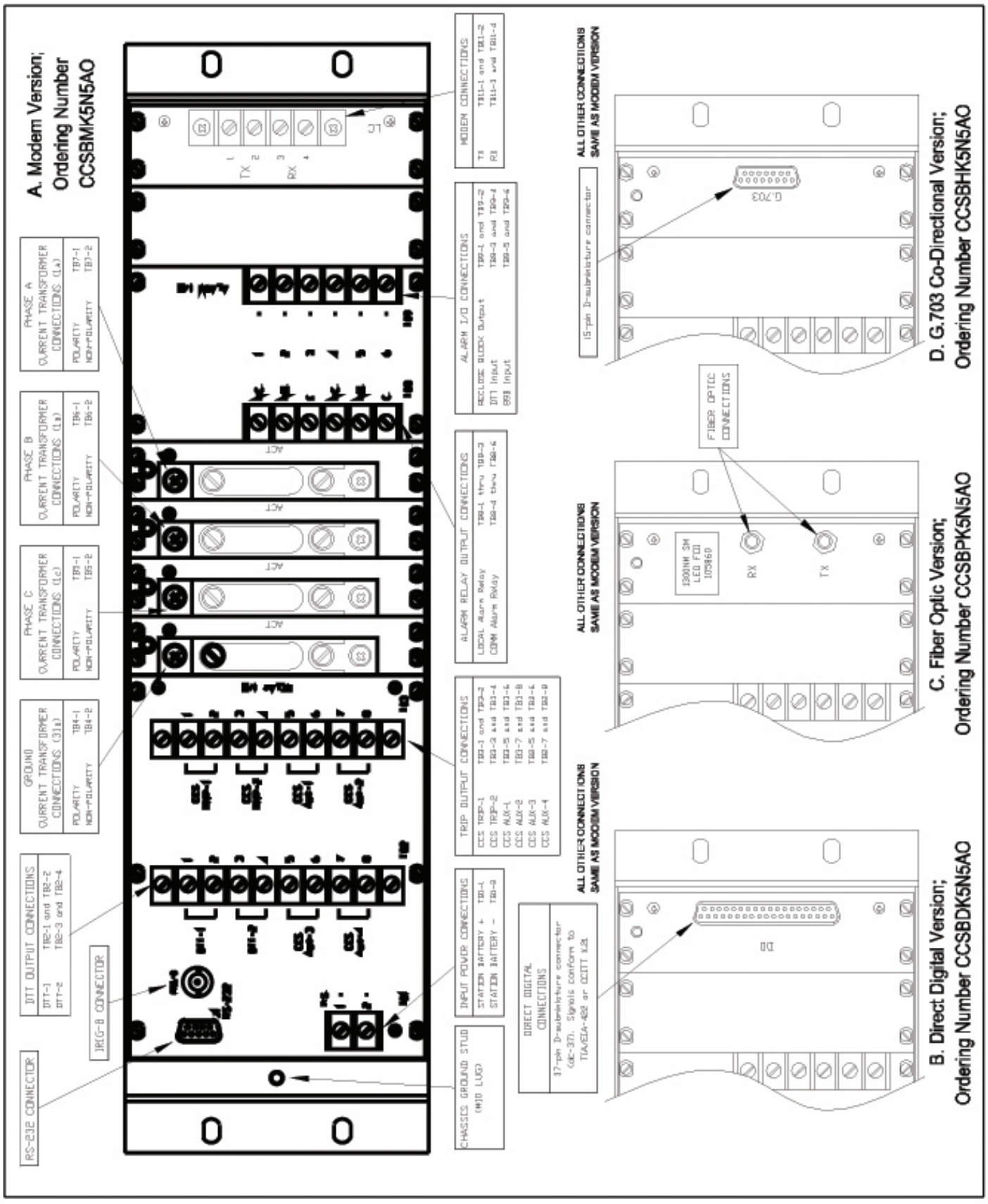


Figure 15. Rear views, typical RFL 9300 terminals

International Compliance Standards

System Configuration
48 to 125 VDC nominal (±20%), with modem, X.21, RS-449, V.35, G.703 (co-directional) and direct fiber optic communications.

1988 IEC 255-22-1
1 MHz burst disturbance tests - Class III. Note that this specification requires insulation tests including impulse withstand tests as specified in IEC 255-5.

1989-10 IEC 255-22-2
Electrostatic discharge test - Class III.

1989-10 IEC 255-22-3
Radiated electromagnetic field disturbance tests - Class III and C37.90.2.

1992-03 IEC 255-22-4
Fast Transient disturbance test - Class III

IEC 255-5 (1977)
Insulation Test (1500 VRMS, 5KV impulse)

IEC 801-5
Lighting Strike (CCS currently meets a similar test)

IEC 255-21-1
Vibration

IEC 255-21-2
Shock

IEC 255-21-3 and C.37.98-1987
Seismic

EN60950
CE Approval

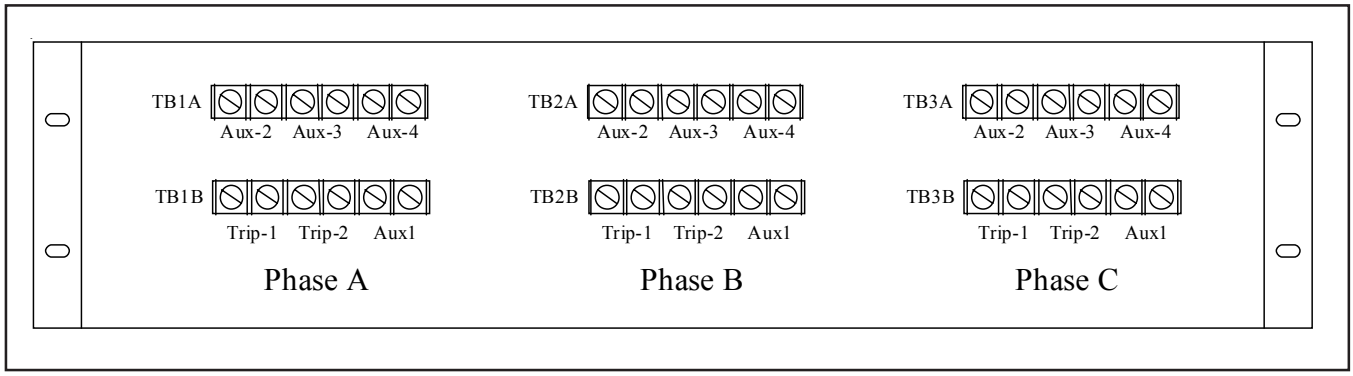


Figure 16. Front View of RFL 9300 Single Pole Chassis Extension.

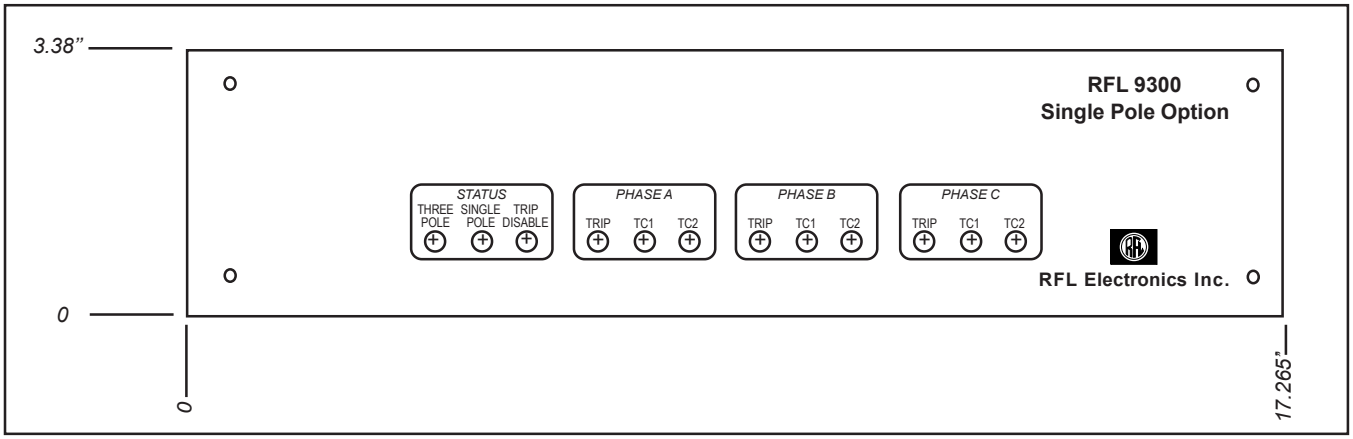


Figure 17. Rear View of RFL 9300 Single Pole Chassis Extension.

Specifications

INPUT:

CT Input Current:
Nominal: 1 or 5 amperes
Continuous: Two-times nominal current
One-Second: Fifty-times nominal current
Frequency: 50 or 60 Hz

DTT and 89B Inputs:
93 Alarm I/O 48 V/125 Vdc (Jumper Selectable)
Input range: **38 Vdc to 58 Vdc**
48 Vdc nominal at 5.5 mA
Input range: **88 Vdc to 150 Vdc**
125 Vdc nominal at 3.9 mA
93 Alarm I/O 250 V:
Input range: **200 Vdc to 288 Vdc**
Nominal: 250 Vdc at 12.6 mA

Burden:
1-Ampere Current Transformers: Less than 0.04W
5-Ampere Current Transformers: Less than 0.002W

OUTPUT:

Output Relays:
BREAKER TRIPPING ("TRIP"): Six sets of N.O. contacts, rated for 5 amperes continuous, 40 amperes for 0.2 seconds.

DTT OUTPUT ("DTT"): Two sets of N.O. contacts, rated for 5 amperes continuous, 40 amperes for 0.2 seconds.

Trip Output Seal In:
CCS or DTT Trip output contact is held closed with >200mA Trip Current detected.

CCS Trip output contact has programmable trip release algorithms.
- Trip plus DC current sense
- Trip plus 100 ms
- Trip plus 0 ms

DTT trip output contact is released when <100mA trip current and not trip signal present for at least 100ms.

Alarm Relays:
Communications Alarm: One set of Form C (SPDT) contacts, rated 0.1 ampere @ 125 Vdc.

System Alarm: One set of Form C (SPDT) contacts, rated 0.1 ampere @ 125 Vdc.

Reclose Block Output:
Optically-isolated phototransistor; operates for internal three-phase faults.
Maximum load: 1A @ 25 deg.C @ 125 Vdc 0.675A @ 65 deg.C @ 125 Vdc
Minimum load current: 0.1A
Minimum load voltage: 0.4 Vdc

GENERAL:

Sensitivity (approximate internal fault current):
1-Ampere Current Transformers: 0.2 ampere total.
5-Ampere Current Transformers: 1.0 ampere total.

Operating Times (typical):
Modem Version: $1^{1/2}$ to $2^{1/2}$ cycles (3 Pole only).
Direct Digital or Fiber Optic Versions: 1/2 to $1^{1/2}$ cycles (3 Pole), 3/4 to 2 cycles (single Pole).
Direct Transfer Trip Operate Times:
Modem: <30 ms
Direct Digital: <16 ms

Modem Communications:
Modulation Scheme: CCITT V.29 QAM
Bit Rate: 7200 bps.
Input/Output Impedance: 600 (ohms).
Typical Application: May be applied to standard voice channel (800 to 2700 Hz). Suitable for use over Type 3002 unconditioned leased lines (Class A line recommended).

Direct Digital Communications:
Interface: Complies with EIA RS-422. 56 or 64 kbps, synchronous, and CCITT G.703, X.21, and V.35

Fiber Communications: See Table 1.

Diagnostic Port:
Meets the requirements of EIA Standard RS-232; equipped with a male 9-pin D-Subminiature (DE-9P).

DNP-3.0 Protocol Interface (Optional)

MODBUS Protocol Interface (Optional)

Dielectric Withstand:
1500 Vrms for one minute, as per IEEE Std. C37.90-1989.

Surge Withstand Capability (SWC):
As per IEEE Std. C.37.90.1-1989 (reaffirmed 1991).

EMI: As per IEEE C37.90.2-1995.

Time Code Port:
Standard IRIG-B either un-modulated or 1 kHz am modulated signal.

IRIG-B:
The display module in the RFL 9300 can be configured to accept either of the following two types of IRIG-B signals:
1. 1 Khz modulated signal, 3.3 Vp-p for logic 1, and 1 Vp-p for logic 0.
2. Unmodulated 0 to +5Vdc TTL signal

Resolution: 1ms

Accuracy:
Free Running: Within 1 minute per month.

Specifications subject to change without notice.

Wavelength and Emitter Type	Fiber Type	Mating Connector Type	Output Level	Receiver Sensitivity	System Gain [1]	Typical Distance (km)[2]	Typical Distance (miles)
850 nm LED	*Multimode*	*ST*	*-18 dBm*	*-43 dBm*	*25 dB*	*8 km*	*5 miles*
1300 nm LED	*Multimode*	*ST*	*-13 dBm*	*-40 dBm*	*27 dB*	*18 km*	*11 miles*
1300 nm LED	*Singlemode*	*ST*	*-17 dBm*	*-40 dBm*	*23 dB*	*29 km*	*18 miles*
1300 nm Laser	*Singlemode*	*ST*	*0 dBm*	*-40 dBm*	*40 dB*	*59 km*	*36.5 miles*
1550 nm Laser	*Singlemode*	*ST*	*-3 dBm*	*-40 dBm*	*37 dB*	*102 km*	*63 miles*
850 nm LED Short Haul	*Multimode*	*ST*	*-19 dBm*	*-32 dBm*	*13 dB*	*1 km*	*.6 miles*

Table 1. RFL 9300 singlewidth fiber optic interface input/output characteristics

Note:
1. System gain is based on power coupled into fiber.
2. Typical distances listed are based on the following assumptions for system loss. As actual losses will vary from one installation to another, the distance covered by your system may vary.

Connector Losses (total of both ends): ST Connectors 2 dB
Fiber Losses:

850-nm Multimode	3dB/km	1300-nm Multimode	1dB/km
300-nm Singlemode	0.5 dB/km	1500-nm Singlemode	.25dB/km

Splice Losses: One splice every 2 km, at .05 db loss per splice.
System Margin: 5 dB additional loss added to calculations to compensate for all other losses.

RFL 9300 Charge Comparison Relay Ordering Guide

BASE SYSTEM:
The RFL 9300 relay is housed in a 19" rack mountable chassis. The chassis is constructed utilizing plug in modules to permit reconfiguring the relay in the field with different communication interfaces or converting from two to three terminal line applications.

SINGLE CHANNEL COMMUNICATIONS OPTIONS:
Select the type of communication interface required. Single pole relays cannot be applied over VF channels.

SECOND CHANNEL COMMUNICATIONS OPTIONS:
Select the type of communication interface required for the second channel. A second channel is required for Dual channel and all three terminal line applications. If a higher data rate communication channel (fiber or direct digital) is selected as the primary channel, a modem interface cannot be combined to operate as the second channel. A dedicated fiber optic channel may be used for the primary channel and a digital channel may be used as the backup or one channel of a three terminal line application.

AC CURRENT:
Select the appropriate value of the secondary CT current that will be applied to the relay.

MIXED CT RATIOS:
The RFL 9300 relay must compare the same magnitudes of current between all terminals. If the turns ratios of the CT's at each terminal are not the same, the current transformers in the RFL 9300 must be modified. Select *Yes* and advise the transformer ratios existing at each terminal.

DC INPUT VOLTAGE:
This defines the power supply input voltage and the direct transfer trip keying input voltage.

CONFIGURATION:
The RFL 9300 can be applied on either two or three terminal lines. Three terminal line configurations require a second communication channel option and a second communications controller module for that channel. Two terminal applications, operating with either a single or redundant communications channels, only require one communications controller module. Converting an existing two terminal RFL 9300 relay for a three terminal application, requires adding a second set of communication modules and a second communications controller module.

RFL 9300 Digital Current Differential Relay Ordering Information

RFL Part Number (fill in blanks):	CCS	
BASE SYSTEM		
Base System - Horizontal Mounting		B
Base System - Vertical Mounting		C
SINGLE CHANNEL COMMUNICATIONS		
Modem (Standard Transformer, 3-Pole Version Only)		M
Modem (UK Transformer, 3-Pole Version Only)		U
Direct Digital RS-449		D
Direct Digital G.703 Co-Directional 64 Kbps		H
Direct Digital V.35 64 kbps		V
Direct Digitral X.21 64 Kbps		X
850-nm Multimode Fiber (LED) (singlewidth/ST)		F
1300-nm Multimode Fiber (LED) (singlewidth/ST)		G
1300-nm Singlemode Fiber (LED (singlewidth/ST)		P
1300-nm Singlemode Fiber (Laser) (singlewidth/ST)		R
1550-nm Singlemode Fiber (Laser) (singlewidth/ST)		J
850-mm Short Haul Fiber Interface (1)		W
SECOND CHANNEL COMMUNICATIONS OPTIONS (2)		
Modem (Standard Transformer, 3-Pole Version Only)		M
Modem (UK Transformer, 3-Pole Version Only)		U
Direct Digital RS-449		D
Direct Digital G.703 Co-Directional 64 Kbps		H
Direct Digital V.35 64 kbps		V
Direct Digitral X.21 64 Kbps		X
850-nm Multimode Fiber (LED) (singlewidth/ST)		F
1300-nm Multimode Fiber (LED) (singlewidth/ST)		G
1300-nm Singlemode Fiber (LED) (singlewidth/ST)		P
1300-nm Singlemode Fiber (Laser) (singlewidth/ST)		R
1550-nm Singlemode Fiber (Laser) (singlewidth/ST)		J
850-mm Short Haul Fiber Interface (1)		W
No second channel		K
AC CURRENT		
1 Ampere		1
5 Ampere		5
MIXED CT RATIO		
Yes (Please specify when ordering)		Y
No		N
DC INPUT VOLTAGE		
38-150 VDC		5
250 Vdc with One Rack Chassis		4
CONFIGURATIONS		
Two Terminal/Three Pole Tripping		A
Three Terminal/Three Pole Tripping		B
Two Terminal/Single Pole Tripping		C
Three Terminal/Single Pole Tripping		D
SUBSTATION COMMUNICATIONS(3)		
None		0
MODBUS		1
DNP 3.0		2
MODBUS with One Rack Unit (1.75") Chassis (4)		3
DNP 3.0 with One Rack Unit (1.75") Chassis (4)		4

NOTES:

(1) If a Fiber Service Unit is required it must be ordered as a stand alone item.
RS-449 FSU (48Vdc) P/N 105075-2, RS-449 FSU (125Vdc) P/N 105075-3, V.35 FSU (48VDC) P/N 105075-4, V.35 FSU (125VDC) P/N 105075-5

(2) Required for dual channel two terminal line applications & all three terminal line applications. Modem communication modules can not be combined with digital or fiber optic communication modules.

(3) Please consult the factory to determine the correct system configuration.

(4) One Rack Chassis required for either three terminal or dual communications applications.

NOTES:



RFL Electronics Inc.

353 Powerville Road
Boonton Twp., NJ 07005-9151
Tel: 973.334.3100
Fax: 973.334.3863
www.rflelect.com
email: sales@rflelect.com



SECTION 2: SYSTEM OPERATION

2.1 INTRODUCTION

This section provides a basic description of how the RFL 9300 Charge Comparison System operates. A block diagram of the RFL 9300 appears in Figure 2-1. After reading this section, refer to Section 24 if your system has the Single Pole Option.

In the description that follows it is understood that if the relay is applied in a 3-terminal system there are two remote stations.

The RFL 9300 Charge Comparison System (CCS) is a protective relaying system for ac power line protection. Its operating principles are similar to those of the more common current differential type of protective relay. Current differential relays compare the total currents entering and leaving the primary protection zone. They will trip the auxiliary relays protecting this zone if the difference between these currents exceeds some pre-defined restraint limit.

For this comparison to be made, the current differential relay at the local station has to know the identical phase current recorded at the remote station(s) for the same interval being considered at the local station. If a single quantity is being compared, its composite phasor must be known. These requirements have always presented problems for the current differential scheme. The exact communications delay between stations must be known in order to make a meaningful comparison. In addition, each recorded current sample must be transmitted to the remote station(s). This requirement places a heavy burden on the communications channel.

The RFL 9300 addresses this problem by comparing local and remote station readings on a half-cycle basis. This drastically reduces the communications channel's throughput requirements. In order to accomplish this, the RFL 9300 is referenced to the zero crossings of the power line current waveform supplied by current transformers at the local station. The RFL 9300 samples the current waveform at a 2-kHz rate (60-Hz systems), integrates all the samples for a half-cycle, and then transmits the result to the remote station(s).

The RFL 9300 has four phase controller modules: one for each phase, and one for ground. Each phase controller has a microcontroller, and there are additional microcontrollers on the display, supervisor, and communications controller modules. A two-terminal RFL 9300 will have seven microcontrollers communicating with one another while executing various control algorithms; a three-terminal RFL 9300 will have eight microcontrollers.

2.2 SYSTEM INITIALIZATION

At turn-on, the local RFL 93B CC Communications Controller Module will attempt to establish contact with the RFL 9300 at the remote station. In order for this to occur, both the local and remote 9300's must be programmed to have compatible transmit addresses. Communications channel delay will be measured once two-way communications are established. To measure the delay, the RFL 9300 measures the round-trip delay of a test (ping-pong) message sent to and returned by the remote RFL 9300. The Communications Controller will not accept the measured channel delay value as being correct until it confirms the measurement with the remote RFL 9300.

Four jumpers on the RFL 93B SV Supervisor Controller Module configure the system. The RFL 9300 uses these jumper settings to configure itself to operate at 50 Hz or 60 Hz, with 1-ampere or 5-ampere auxiliary current transformers (ACT's), as a two- or three-terminal system, or as a three-pole or single-pole system.

Finally, each RFL 9300 confirms that it is configured the same as the other RFL 9300. If the configurations do not match, neither RFL 9300 will exit the initialization mode.

The RFL 93B SV cannot initialize the RFL 93B PC Phase Controller Modules until a valid channel delay compensation (CDC) value is available. During the initialization process, the RFL 93B SV will test all programmed variables stored in its non-volatile memory. These variables control phase/ground bias, phase/ground overcurrent, the fault detector setting, and other variables. If their values are valid, they are passed to the phase controllers. None of the phase controller modules will exit the initialization mode until they have received and acknowledged the CDC values and all programmed variables sent by the RFL 93B SV.

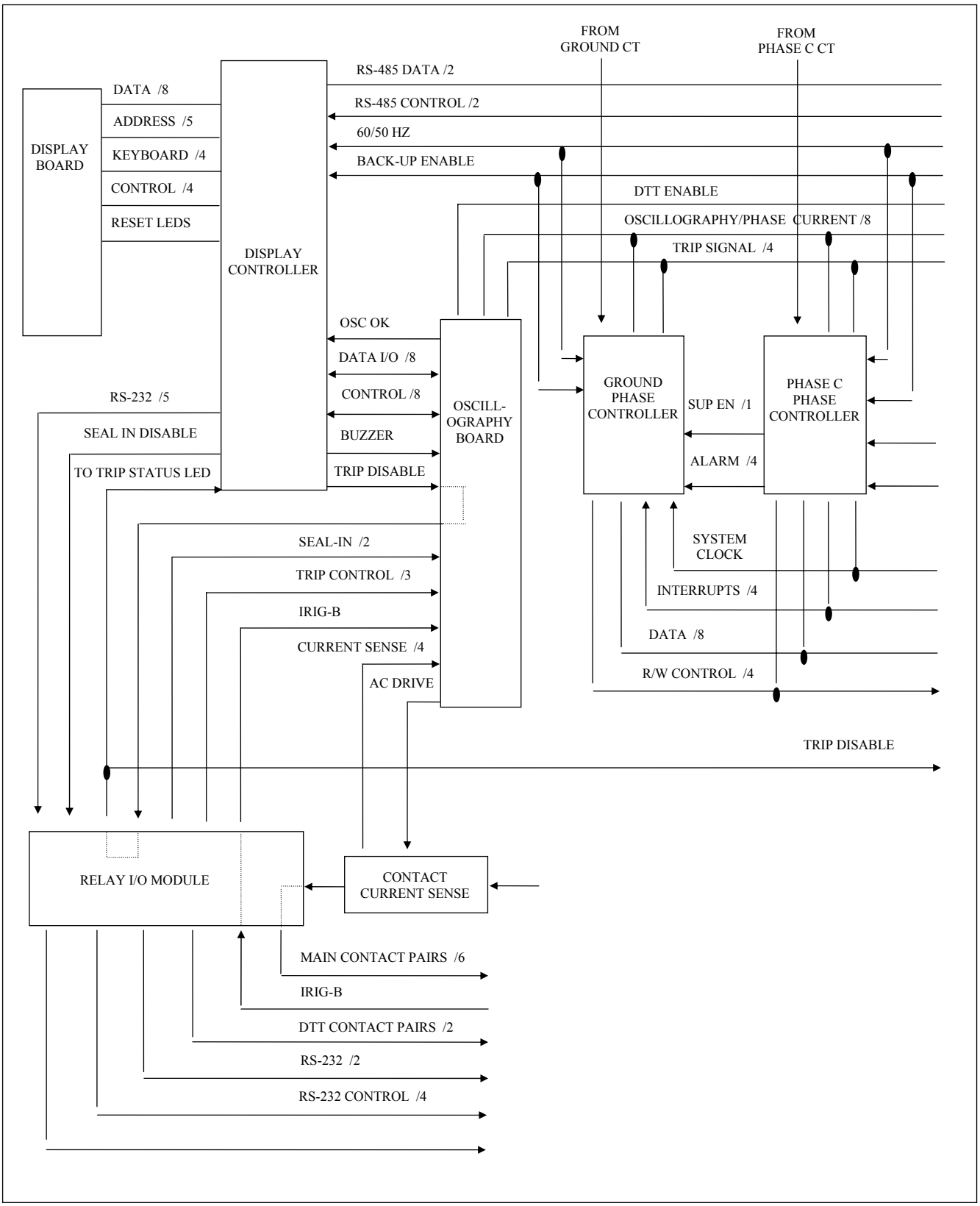
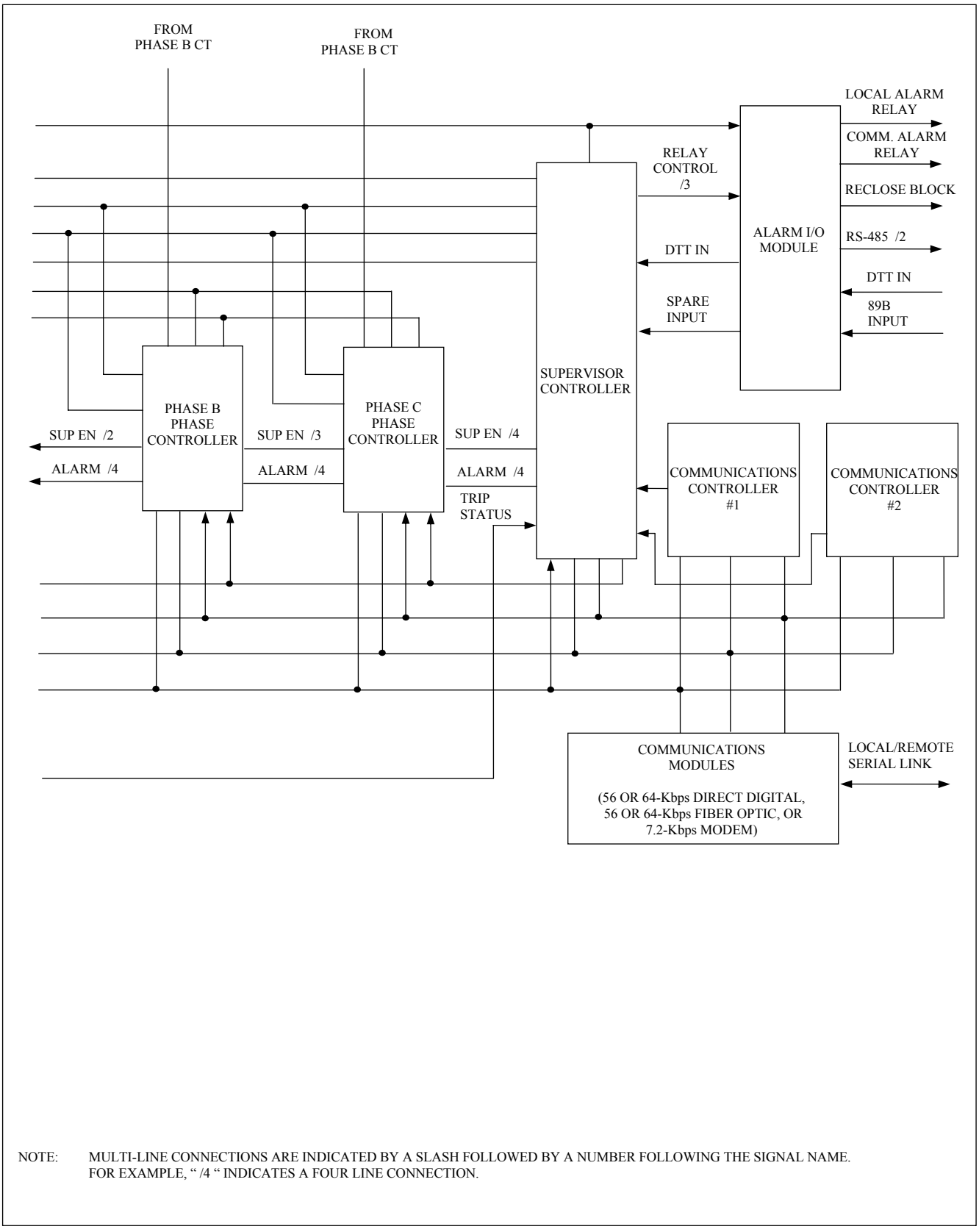


Figure 2-1. Block diagram, RFL 9300 Charge Comparison System (two terminal)



NOTE: MULTI-LINE CONNECTIONS ARE INDICATED BY A SLASH FOLLOWED BY A NUMBER FOLLOWING THE SIGNAL NAME. FOR EXAMPLE, " /4 " INDICATES A FOUR LINE CONNECTION.

Figure 2-1. Block diagram, RFL 9300 Charge Comparison System (two-terminal) - continued

The RFL 93B SV must first establish its interface with the RFL 93B DISPLAY Display Module in order to obtain the transmit address for the communications channel. Once this address is obtained the supervisor will pass it to the RFL 93B CC Communications Controller to trigger the initialization sequence between the two modules.

2.3 COMMUNICATIONS CONTROLLER MODULE

The RFL 93BCC Communications Controller Module controls the formatting, transmission, and reception of all station-to-station messages. Synchronous serial voice-channel and high-speed digital communications options are available. The RFL 93B CC Communications Controller Module supports 7.2 KBPS V.29 data over a leased line and a variety of 56/64 KBPS digital interface modules.

During start-up, the RFL 93B CC "learns" the RFL 9300 's communications configuration by measuring the clock rate and testing the system control lines. It also checks the system configuration data it receives from the RFL 93B SV module. The RFL 93B CC uses this information to determine its internal software path; there are no jumpers to set.

The functions that are common to all configurations and speeds are described below, followed by those that are applicable to more specific applications.

Messages within the 9300 may originate on any controller module. A non-volatile static RAM on the RFL 93B SV serves as the system "mailbox." All messages between the RFL 93B SV and the RFL 93B CC pass through this mailbox over an eight-bit bi-directional data bus. When a new message is read, the communications controller first establishes the message's priority and then stores it in its internal RAM. If the message contains time values, the microcontroller increments the time and discards the message if overflow occurs before the message can be sent. The message with the highest priority is compressed and loaded into the transmitter shift registers, along with CRC bits. The RFL 93B CC module at the remote RFL 9300 uses the CRC bits to test the validity of the transmitted message.

Simple messages consist of single 15-bit words; eight data bits, six CRC bits, and one framing bit. More complicated messages require two 15-bit words. The transmitter logic circuits supply the framing bit to mark the beginning of each word. The framing bit toggles from word to word. A never-ending stream of messages is continuously transmitted to insure that the remote terminal can frame regardless of the state of the transmitting terminal. A null word will be transmitted if there is nothing else to send. The RFL 93B CC at the remote RFL 9300 uses a hardware comparator and EPROM lookup table to test the CRC security of each received word. The security test must be done in hardware because of the high speeds associated with 56-Kbps and 64-Kbps communications. The microcontroller performs the framing function by resetting a 15-state counter when the data, CRC, and frame bits line up. The counter then automatically generates a latch signal for future data reads by the microcontroller. Most messages received from the remote RFL 9300 are passed to the RFL 93B SV module for distribution to other controllers in the system.

2.3.1 SINGLE-CHANNEL MODEM OPERATION

If the first module slot in the RFL 9300 chassis contains a RFL 93B MO Modem Module, the RFL 93B CC initializes and resets the modem through a dedicated 15-bit bus connecting the boards. The RFL 93B MO uses modem control bits to configure it as a CCITT V.29 modem operating at 7.2 KBPS.

Modems occasionally require training from the remote station. This function is initiated by the RFL 93B CC. The words passed between the remote or local modems and their respective RFL 93B CC modules are synchronous and serial.

The squelch rules that define a valid word depend on the communications system. These rules apply to each word as it is received. They determine if an alarm should be issued to the RFL 93B SV Supervisor Controller Module, or if the serial link between the RFL 93B CC and the modem must be re-framed.

2.3.2 HOT STANDBY TWO-CHANNEL MODEM OPERATION

If the second module slot in the RFL 9300 chassis contains another RFL 93B MO Modem Module and the system is not configured for three-terminal operation, the Communications Controller will control both modems. The RFL 93B CC "learns" the configuration while initializing. During normal operation, communications with the remote RFL 9300 are maintained over both channels. The RFL 93B CC monitors the channels and switches to the other channel if the active channel fails. After the switchover, the RFL 9300 sends a message to the remote RFL 9300 , asking that it also switch to the other channel. In all other respects, hot standby operation is identical to single-channel modem operation. Hot standby mode is not available if the relay is configured for 3-terminal operation.

2.3.3 SINGLE-CHANNEL 56/64-Kbps DIGITAL OR FIBER OPTIC OPERATION

The RFL 9300 is equipped with an RFL 93 DD Direct Digital I/O Module, a Fiber Optic transceiver module or a G.703 module when high-speed digital communications are required. The RFL 93B CC will "learn" the system configuration from the received clock rate and strap setting information received from the RFL 93B SV module.

The alarm conditions and squelch rules used during high-speed operation are different from those used during modem operation. Each word is transmitted three times, and the receiver uses a two-out-of-three voting scheme to determine if a received message is valid. Direct digital operation requires a synchronous clock to be supplied by external data communications equipment (DCE), and ports for TX and RX data.

2.3.4 HOT STANDBY TWO-CHANNEL 56/64-Kbps DIRECT DIGITAL OR FIBER OPTIC OPERATION

For two-channel, high-speed, hot standby applications, a pair of RFL 93 DD Direct Digital I/O Modules, a pair of Fiber Optic transceiver modules, or a pair of G.703 modules are plugged into both rear chassis communications slots. The local and remote RFL 93B CC modules "learn" the configuration during initialization, and employ high-bit rate squelch rules to command channel switchover if a channel should fail several frame attempts. Hot standby mode is not available if the relay is configured for 3-terminal operation.

2.3.5 HOT STANDBY CONFIGURATIONS

In 9300 applications that use the hot standby feature, some limitations must be kept in mind if the communication medium at Channel 1 and Channel 2 are different types. The limitations are due to differences in the clock sources used by the communication medium. Refer to Table 2-1 for valid hot standby configurations.

Table 2-1. Valid Hot-Standby Configurations

Communication Channel 1	Communication Channel 2	Synchronous Clock? (Yes/No)[3]	Valid Configuration? (Yes/No)	Rapid Switchover? (YES/No)[1,2]	Reason
93 MO (Modem)	93 MO (Modem)	YES	YES	YES	Channel 2 locks onto Channel 1. The clock source is a local crystal in the Channel 1 modem.
93 MO (Modem)	Any non-modem	N/A	NO	N/A	Wrong clock rate. 7.2 KBS cannot mix with high-speed clocks.
93 DD I/O (RS422)	93 DD I/O (RS422)	YES	YES	YES	Both get clock from the same external source.
93 DD I/O (RS422)	93 DD I/O (RS422)	NO	YES	NO	Clocks from different sources. The clocks should not be different by more than 5 percent.
93 FT/FR (Fiber)	93 FT/FR (Fiber)	YES	YES	YES	Fiber is dark (direct connection from 9300 to 9300). Channel 2 locks onto Channel 1. The clock source comes from a local crystal in Channel 1.
94 G.703	93 G.703	YES	YES	YES	Channel 2 locks onto Channel 1. This is valid if both get clocks from the same external central clock source (E1). This is usually the case.
94 G.703	93 G.703	NO	YES	NO	Two different networks, one for Channel 1 and another for Channel 2. This is not typical.
93 FTFR	93 G.703	NO	YES	NO	The 93 G.703 channel can be over a network.
93 FTFR	93 DD I/O (RS422)	NO	YES	NO	Channel 2 does not lock onto Channel 1. The 93 DD can only get a clock from an external source.
93 G.703	93 FTFR (Fiber)	YES	YES	YES	Channel 1 is locked onto the central clock and shares it with channel 2.
93 DD I/O (RS422)	93 FT/FR (Fiber)	YES	YES	YES	The Channel 1 clock source is the central clock. It will share the clock with Channel 2.
93 DD I/O (RS422)	93 G.703	YES	YES	YES	Only if Channel 1 clock source is the central clock. It will share the clock with Channel 2.
93 DD I/O (RS422)	93 G.703	NO	YES	NO	The 93 G.703 module can be locked to the network. This occurs if the jumper on the 93 G.703 module is set to “NORMAL”.
93 SHFI	93 SHFI	YES	YES	YES	Only if both get the clock from the same external source. The clock source must come from both Fiber Service Units.

Notes:
1. Rapid Switchover is typically 30 ms. Non-rapid switchover is 500 ms to 2 seconds.
2. Switchover is defined as the time it takes to switch from one channel to another in the event of a break in communications.
3. Synchronous clock indicates that Channel 1 and Channel 2 have a common clock source.

2.4 CHANNEL IMPAIRMENT CHARACTERISTICS

RFL 9300 terminals operate with different channel impairment characteristics, depending on how the terminal is configured. The following paragraphs describe the characteristics for direct digital, fiber optic, and single-channel modem interfaces.

2.4.1 TERMINALS EQUIPPED WITH DIRECT DIGITAL OR FIBER OPTIC INTERFACES

2.4.1.1 COMMUNICATIONS CONTROLLER OPERATION

The RFL 93B CC Communications Controller Module controls the RFL 93 DD I/O Direct Digital I/O Module, or the Fiber Optic transceiver module, and receives the incoming serial data. The incoming serial data is framed into words and decoded. If the words are valid, they are passed on to the RFL 93B SV Supervisor Controller Module for distribution to the other modules in the terminal.

A hardware receiver in the RFL 93B CC module counts the bits and tests each word for a valid CRC code and framing bit. In normal operation, the receiver hardware is framed correctly and tests the word at a count of fifteen (8 data bits + 6 CRC bits + 1 frame bit). If the framing is not correct, the microcontroller goes into a special sub-routine that resets the counter after five good words are observed.

After the counter is initialized, the burden of counting the bits and strobing each word into the microcontroller falls on the hardware receiver. When a word is received, the hardware signals the microcontroller and indicates whether the word passed the CRC test. The software in the microcontroller then applies squelch rules. These rules determine if the channel is good enough to give messages formed from the words to the RFL 93B SV module. To enhance security and dependability, a two-out-of-three voting scheme is used. Each word is sent three times; the receiver groups the three word segments and looks for two out of the three word segments to agree. If two segments are identical, the word is accepted as valid.

2.4.1.2 SQUELCH RULES

The microcontroller counts the number of good and bad word segments. It uses this information to decide if the channel is good or bad. The word segments are binary, and the errors that are counted yield a bit error rate (BER) which is a measure of communication quality. The noise on a channel may be long-term average noise, or the noise may come in pulses for a short duration. The RFL 93B CC uses three squelch rules to determine whether communication quality is below that required by the RFL 9300. They are identified as Squelch Rule 1, Squelch Rule 2, and Squelch Rule 3 (SQ1, SQ2, and SQ3):

SQ1 SQ1 blocks messages from going to the RFL 93B SV module, but does not alarm the module. SQ1 is entered if 16 bad word segments in a row are received, and turned off if 32 good word segments in a row are received.

SQ2 SQ2 relates to short error pulses, and is the trigger that frames the local receiver hardware. SQ2 will also alarm the RFL 93B SV module and block messages from being sent to the rest of the terminal. If 30 bad word segments are received out of a total of 250, the RFL 93B CC enters SQ2. It takes 100 good word segments in a row to exit SQ2.

SQ3 Under SQ3, the RFL 93B CC module will squelch the channel if the long-term noise produces a BER of -3 or worse. This represents one bad bit in 1,000 bits. When SQ3 is on, the RFL 93B CC module alarms the RFL 93B SV module and blocks all communication messages from going to the RFL 93B SV module.

To come out of SQ3, the BER must be better than -4 (one bad bit in 10,000). It takes 540 ms to measure the 2000 word segments used to calculate SQ3; a fast exit from SQ3 occurs if 1,000 error-free word segments in a row are received within 270 ms.

To enter SQ3, 30 bad word segments out of a total of 2000 word segments were measured. If 30 bad word segments are received in a row, SQ3 is entered without waiting for the full 2000 word segments. After the RFL 93B CC has entered SQ3, less than 3 bad segments out of 2000 segments are required to drop SQ3.

2.4.1.3 FRAMING

The RFL 93B CC module frames the receiver hardware when SQ2 is entered. If the framing is not successful, another frame attempt is made after two seconds. This continues every two seconds until a successful frame is made. A pin on the RFL 93 DD I/O module's DC-37 connector acts as a remote channel condition input. If the DCE knows that the channel is bad, this pin is held low. When the channel is good and the logic level on the pin is raised, the channel is framed after two seconds.

2.4.2 TERMINALS EQUIPPED WITH SINGLE-CHANNEL MODEM INTERFACES

2.4.2.1 MODEM OPERATION

The RFL 93B MO Modem Module receives voice-band analog signals (300 Hz to 3300 Hz), and converts these signals into a 7.2-Kbps stream. The method used in the conversion is "Quadrature Amplitude Modulation," or "QAM." QAM means that the phase and amplitude are changing. The rate of change is 2400 times a second, and each QAM vector represents three bits. Since the QAM vectors are changing 2400 times a second (baud rate) and each change equals a three-bit value the data rate equals 7,200 bits per second (3 times 2,400).

To decode these vectors, the modem's receiver must equalize the incoming analog signal to compensate for changes in phase and amplitude that could be introduced by the communication path. The reference vector used by the transmitter must also be learned by the receiving modem. A training sequence is sent by the transmitting modem; the receiving modem recognizes this sequence of tones and learns the reference vector while equalizing the line. After training is complete, the serial data bits inputted to the transmitter appear out of the receiver (after a delay).

An automatic gain control (AGC) circuit adjusts the incoming level over a dynamic range of 0 to -37 dBm. An additional measure is available in the modem, since the value of each QAM vector is known. The error from the ideal point can be measured, and the value of error is called EQM (Eye Quality Monitor). This value is read by the RFL 93B CC module if the digital words received are in error.

2.4.2.2 COMMUNICATIONS CONTROLLER OPERATION

The RFL 93B CC module controls the RFL 93B MO Modem Module, and receives its incoming serial data. The incoming serial data is framed into words and decoded. If the words are valid, they are passed on to the RFL 93B SV Supervisor Controller Module for distribution to the other modules in the terminal.

A hardware receiver in the RFL 93B CC module counts the bits and tests each word for a valid CRC code and framing bit. In normal operation, the receiver hardware is framed correctly and tests the word at a count of fifteen (8 data bits + 6 CRC bits + 1 frame bit). If the framing is not correct, the microcontroller goes into a special sub-routine that resets the counter after five good words are observed.

After the counter is initialized, the burden of counting the bits and strobing each word into the microcontroller falls on the hardware receiver. When a word is received, the hardware signals the microcontroller and indicates whether the word passed the CRC test. The software in the microcontroller then applies squelch rules. These rules determine if the channel is good enough to give messages formed from the words to the RFL 93B SV module.

2.4.2.3 SQUELCH RULES

The microcontroller counts the number of good and bad words. It uses this information to decide if the channel is good or bad. The word segments are binary, and the errors that are counted yield a bit error rate (BER) which is a measure of communication quality. The noise on a channel may be long-term average noise, or the noise may come in pulses for a short duration.

The quality of the analog signal received by the modem is expressed as a signal-to-noise (S/N) ratio. If the line coming into the modem is a Type 3002 line, the spectrum is not flat and equalization is required. The link between S/N and BER (Bit Error Rate) changes slightly with added equalization (2 dB). If the S/N is better than 16 dB, the dependability of the relay is 100 percent with a 3002 conditioned line.

The RFL 93B CC uses three squelch rules to determine whether communication quality is below that required by the RFL 9300 . They are identified as Squelch Rule 1, Squelch Rule 2, and Squelch Rule 3 (SQ1, SQ2, and SQ3):

SQ1 SQ1 blocks messages from going to the RFL 93B SV module, but does not alarm the module. SQ1 is entered if two bad words in a row are received, and turned off if three good words in a row are received.

SQ2 SQ2 relates to short error pulses. It is the trigger that frames the local receiver hardware, and sends retrain request messages to the remote terminal. SQ2 will also alarm the RFL 93B SV module and block messages from being sent to the rest of the terminal. If eight bad words are received out of a total of 25, the RFL 93B CC enters SQ2. It takes ten good words in a row to exit SQ2.

If SQ2 is on for 100 ms and the EQM value indicates that the channel is good, the hardware receiver is initialized or framed. If the channel is bad for over 500 ms and SQ2 is on, a request is sent to the remote terminal and the remote terminal sends a training sequence. After the training sequence has been received, the hardware receiver is initialized for framing. For short noise bursts (less than 50 ms), the QAM reference vector is not lost and the channel recovers within 10 words after the noise turns off.

SQ3 Under Squelch Rule 3 (SQ3), the RFL 93B CC module will squelch the channel if the long-term noise produces a BER of -3 or worse. This represents one bad bit in 1,000, and is equivalent to an S/N ratio of about 16 dB. When SQ3 is on, the RFL 93B CC module alarms the RFL 93B SV module and blocks all communication messages from going to the RFL 93B SV module.

To come out of SQ3, 3 the BER must be better than -4 (one bad bit in ten thousand). This is equivalent to an S/N ratio of about 18 dB. It takes over 4 seconds to measure the 2,000 word segments used to calculate SQ3; a fast exit from SQ3 occurs if 1,000 error-free word segments in a row are received within 2 seconds. A fast exit can also occur if the EQM (Eye Quality Monitor) indicates that the S/N is better than 18 dB. The EQM value could return to normal in less than 100 ms if the average noise is not too great.

To enter SQ3, 30 bad word segments out of a total of 2000 word segments were measured. If 30 bad word segments are received in a row, SQ3 is entered without waiting for the full 2000 word segments. After the RFL 93B CC has entered SQ3, less than 3 bad segments out of 2000 segments are required to drop SQ3.

2.5 SUPERVISOR CONTROLLER

The RFL 93B SV Supervisor Controller Module is the hub of all activity at each RFL 9300. The RFL 9300 is a permissive trip system that is heavily dependent on messages passed between stations. Most messages received from the remote RFL 9300 are meant for the phase and display controllers. Messages to and from the display and phase Controllers must pass through the RFL 93B SV as they move to or come from the RFL 93B CC.

The RFL 93B SV executes four main tasks:

1. It controls the turn-on and initialization of the system.

2. It acts as the message control center for all messages to and from the Phase, Communications and Display controllers.

3. It monitors the back panel I/O ports, the system alarm lines, single-pole logic status, and the system configuration straps.

4. It generates the 2-kHz system clock. The leading edge of this clock generates the interrupt signal that synchronizes the RFL 93B CC Communications Controller Module, the RFL 93B SV Supervisor Controller Module, all RFL 93B PC phase controllers, and the single-pole logic.

While the RFL 93B SV is initializing, the microcontroller's internal timers of are programmed to generate a 2-kHz clock (1980 Hz for a 3-terminal application). The phase controllers use this clock to synchronize their program execution to the RFL 93B SV. In 3-terminal applications the supervisor phase locks the system clock to the line frequency on the basis of error signals received from the phase controllers.

Once the RFL 93B SV has initialized, it establishes an interface with all the controllers at the local RFL 9300. The RFL 93B SV interfaces to the display controller through an RS-485 serial link. It interfaces to all other controllers through an 8-bit bi-directional data bus and a 10-bit control bus located on the system backplane.

First, the RFL 93B SV establishes the RS-485 interface with the display controller. Once this interface is established the display controller will supply the transmit address of the communications channel. Two separate addresses are required if the relay is configured for 3-terminal operation.

The RFL 93B SV initiates contact with the RFL 93B CC by sending it the transmit address of the communications channel. This triggers a set initialization routine between the two controllers. During this routine, the RFL 93B SV receives verification that the RFL 93B CC has established communications with the correct remote station, that both stations have the same configuration, and are measuring the same channel delay value.

Each phase controller will trigger an initialization sequence with the RFL 93B SV by passing its software ID number. The supervisor will not complete the sequence until a valid channel delay value is available from the communications controller.

All communications between the RFL 93B SV, RFL 93B CC, and all four RFL 93B PC phase controllers is through a non-volatile static RAM "mailbox" on the RFL 93B SV. The RFL 93B SV controls all access to the mailbox; the other controllers are granted access to the mailbox through a hardware-generated sequential series of interrupt signals. Each phase controller is allowed a maximum of 50 µs to read three bytes from and to write three bytes to its mailbox locations. The RFL 93B SV has access to the memory for about 30 µs and then grants access to the Communications Controller for the remainder of the 0.5-ms interval. The RFL 93B CC and RFL 93B PC controllers will only have access to the mailbox when the interrupt signal received from the RFL 93B SV is low. Once this signal goes high, hardware control will isolate the controller from the mailbox. Since the RFL 93B PC modules and the RFL 93B CC use a different language, messages originating at one must be formatted by the supervisor before they can be passed to the other.

The RFL 93B SV supplies the received DTT trip signal to the Oscillography Board through a dedicated hardware line. It also monitors the local RFL 9300 's DTT input port. The DTT input trip signals it detects are passed to the Communications Controller for transmission to the remote RFL 9300. The DTT signal is described in detail later in this section.

Breaker open/closed status is determined by the RFL 93B SV on the basis of a zero-true-current signal (ZTC) received for each phase controller. A phase controller will send this signal to the supervisor if it has not detected a CT current >1/8A peak for 40ms. A phase controller will not rescind its' ZTC signal until a CT current >1/4A peak is detected. If the RFL 9300 is configured for three-pole trip operation and is receiving a ZTC signal from all four phase controllers it will issue an open breaker signal to all of them. If any one of the phase controllers rescinds its ZTC signal the RFL 93B SV will signal all phase controllers that the breaker is closed. When the RFL 9300 is configured for single-pole operation the open breaker condition is determined on a phase-by-phase basis. Any phase controller sending a ZTC signal to the RFL 93B SV will wait to declare its breaker to be open until the RFL 93B SV returns the open breaker signal.

The RFL 93B SV monitors all trip signals originating at both the local and remote terminals. If the RFL 9300 is configured for three-pole trip operation and a trip signal (generated locally or remotely) is detected, a 150ms timer is started. If trips are detected on all phases before this timer expires, a three-phase trip is said to exist, and the reclose block output relay is energized for 50ms. If the RFL 9300 is configured for single-pole trip operation and a trip signal is detected, a 3 second timer is started. If a trip signal is detected on another phase before this timer expires, and Selective Pole Relaying is not enabled, all three single-pole breakers will be tripped and the reclose block output relay will be energized for 50ms. If Selective Pole Relaying is enabled, a trip signal must be detected on all three phases before the 3 second timer expires before the reclose block output relay will be energized.

The RFL 93B SV continuously monitors all system and communications alarm signals. If it detects an alarm, the appropriate alarm relay will drop out, initiating an alarm. If it detects a communications alarm, the RFL 93B SV will command the RFL 93B PC modules to enter the backup mode. The RFL 93B PC modules will disable permissive trip, but will only enter backup mode if the operator has enabled it. (See stub bus description in paragraph 2.7.7) If the RFL 9300 is configured for single-pole trip operation and the relay is operating in backup mode, any locally calculated trip signal that is detected will result in all three single-pole breakers being tripped and a reclose block signal being issued. This is the case regardless of the status of the Selective Pole Relaying option.

Only the RFL 93B CC can establish a communications alarm due to bad data or noise. The only communications alarm determined by the RFL 93B SV, is the channel delay alarm. This alarm is active when the channel delay value received from the Communications Controller is greater than 31 ms.

2.6 AUXILIARY CURRENT TRANSFORMER (ACT)

A separate RFL 93B PC Phase Controller and RFL 93B ACT I/O monitors each phase current and the ground or $3I_0$ current. The input to the RFL 93B ACT I/O consists of a small toroidal core with a single turn looped through its center. This single turn is an extension of the secondary winding of the CT supplying the phase current waveform. Like most static relays, the burden presented by the RFL 93B ACT I/O is in the milliohm range. An active circuit cancels out the flux in the toroidal core. This allows the toroid to handle large dc offsets without saturating. The circuit maintains its accuracy over a 250-ampere (rms) dynamic range.

The RFL 93B PC detects disturbances in the phase current waveform received from the RFL 93B ACT I/O. It generates a signal in response that prevents a charge from accumulating on the feedback capacitor in the RFL 93B ACT I/O's feedback control circuit. This patented procedure prevents any dc offsets that may be present in the current waveform from saturating the core.

2.7 PHASE CONTROLLERS

Once the phase controllers have initialized, they begin to monitor system current and execute the protection algorithms. The leading edge of the 2-kHz system clock supplied by the RFL 93B SV synchronizes phase controller program execution. All background and foreground routines execute during the 0.5-ms system clock interval. The phase controllers execute the CCS trip algorithms listed below. Except for DTT (which is controlled by the RFL 93B SV module), the individual RFL 93B PC modules make all trip/no trip decisions.

Phase Controller operation differs radically depending on whether the relay is configured for 2-terminal or 3-terminal operation:

2-Terminal Operation:

a. Phase Controllers execute their trip algorithms based on true CT current values.

b. Trip algorithms are executed immediately upon receiving a CCD, WCM or UHST message from the remote station.

3-Terminal Operation:

a. The system clock supplied by the supervisor is phase locked to the line current waveform (if one exists) on the basis of error signals supplied by whichever phase controller is currently selected by the 93B SV. The phase controller measures the number of clock signals received over a defined interval and signals the supervisor to adjust the period of the system clock until it is receiving exactly 33 clock signals per line frequency period.

b. Phase Controllers, with the exception of the 3I0 controller, execute their trip algorithms based on transient CT current values obtained by subtracting prefault load current from true CT current on a continuous basis. This is done to counteract the wide phase angle swings encountered in 3-terminal systems. 3I0 controller trip algorithm execution, is based on true CT current, the same as in 2-terminal applications.

c. Trip algorithms are not executed until a CCD, WCM or UHST message is received from both remote stations. In addition, before the messages are accepted they must “validate” each other i.e. they must, with a high degree of certainty, represent the total remote station CT transient current during the same time interval.

d. Once this “validation” process is complete, the remote station composite transient CT current value and the local station CT current transient value are run through the same trip algorithms used for 2-terminal systems.

In 2-terminal systems the analog output of each RFL 93B ACT I/O is passed to an RFL 93B PC Phase Controller Module. The RFL 93B PC uses an equivalent 10-bit serial A/D converter to convert the analog signal to a digital value. The integral of all such “control” CT current samples taken during a half-cycle is computed when the half-cycle-ending zero-crossing time-tag is recorded.

In 3-terminal systems the analog output of each RFL 93B ACT I/O is passed to an RFL 93B PC Phase Controller Module. The RFL 93B PC uses an equivalent 10-bit serial A/D converted to convert the analog signal to a digital value. The converted value is compared with a sample at least 1-cycle old and the difference or "control" CT current value is recorded. The integral of all control CT current values recorded during a half-cycle is computed when the half-cycle-ending zero-crossing time-tag is recorded.

Note - In a 2-terminal system the control CT current value is a true CT current value while in 3-terminal systems the control CT current value is a transient value.

In both 2- and 3- terminal systems the integral is converted to an equivalent ampere rms value, and stored in an on-board buffer along with the half-cycle's start and finish time-tags. A bit indicating polarity is also stored. Integral values representing the positive half-cycles of the phase A, B, and C currents and the negative half-cycles of the 3I0 current, are truncated to six bits. The truncated value is transmitted to the remote station as a CCD message. Transmitting the currents to the remote station in this manner greatly reduces the communications channel throughput requirements without compromising system protection. If all recorded samples or both the positive and negative half-cycle integral values were transmitted, the throughput requirements would be much greater. This communication technique has been proven through extensive field and laboratory tests.

2.7.1 WEAK CURRENT MESSAGE - WCM

For three terminal systems the integral sum of the control CT current samples is continuously calculated over the latest 8-millisecond interval. If this sum is <0.5A rms for a minimum of 16ms WCM transmission to the remote station is enabled. In this case the WCM conveys no information on breaker status. This message is essential for 3-terminal systems since a control message must be received from both remote stations to enable permissive trip. This is a change from the way CCS operates in two terminal mode, as there is no control message transmitted if the control CT current is <0.5A rms, unless the breaker is open.

If the relay is configured for 2-terminal operation the WCM represents an open breaker at the sending station. However if the relay is configured for 3-terminal operation a phase controller could be sensing a constant strong true CT current and still be sending a WCM since the transient value is <0.5A rms.
It is important to recognize this difference in order to understand CCS 3-terminal operation.

The RFL 9300 will not store a CCD message in the local on-board buffer or transmit it to the remote station if either of the following occur:

1. The CT current recorded during a given half-cycle interval is less than 0.5 A_{rms}.

2. The duration of the half-cycle is less than 6 ms.

The RFL 9300 executes the following trip algorithms during each 0.5-ms system clock interval.

1. Strong-feed trip (SFT).

2. Weak-feed trip (WFT).

3. Switch-into-fault (SIF) with communications.

4. Ultra high-speed trip (UHST).

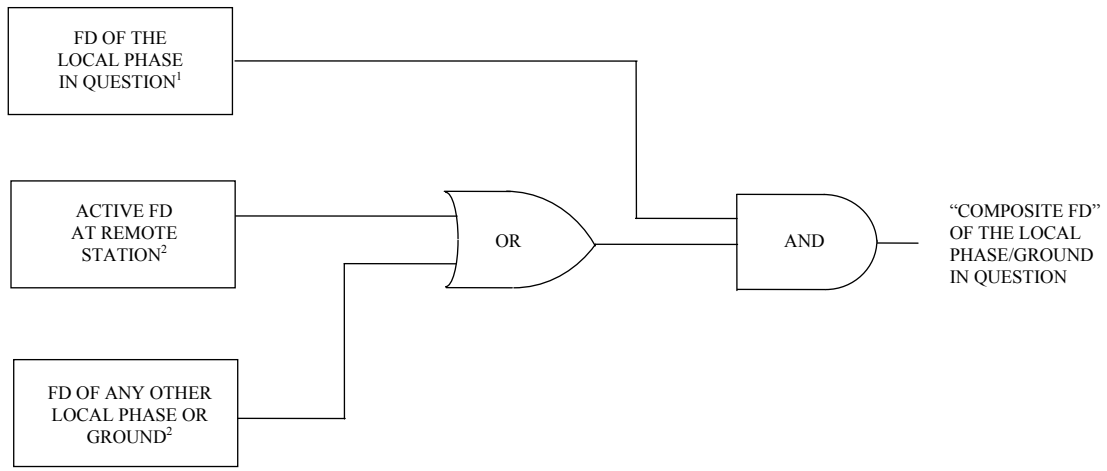
5. Open Conductor.

The SFT, WFT, SIF, and UHST algorithms depend on a comparison of local and remote current waveforms. For these algorithms, a knowledge of event timing is critical. When each current value arrives from the remote station, the RFL 9300 time-tags it. Each algorithm uses different formulas to adjust the received time-tag.

In 2-terminal systems the adjusted received time-tags are used to select or "nest" with the locally stored half-cycle integral that should be compared with the received CCD or WCM control signal value when executing the SFT algorithm.

In 3-terminal systems the adjusted received time-tags are used to select a locally stored half-cycle nested by both CCD, WCM or a combination of these control signals received from the remote stations. Once this determination is made the remote signals must be combined to form a composite signal that will be compared with the selected or “nested” local half-cycle integral when executing the SFT algorithm.

The open conductor algorithm depends only on current values read at the local station. When a trip condition exists, the algorithms produce a trip enable signal; this is a necessary but not sufficient condition to cause a trip signal to be issued. Besides the trip enable signal, at least two fault detectors must be active somewhere in the system. (See Figure 2-2.) One of the active detectors must be the fault detector for the phase in question. A RFL 93B PC will only issue a trip signal without having an active fault detector if it receives a trip signal (CCT-U) from the remote RFL 9300.



1. In a two terminal system, if the 3Io controller has an active fault detector it will compute a composite FD when the remote breaker is open. For this special case additional fault detectors are not required.

2. In three terminal systems this does not include the overcurrent fault detector for the phase A, phase B or phase C controllers. The overcurrent fault detector of the 3Io controller is “global” for only 125 ms after it becomes active.

Figure 2-2. Logic diagram, composite fault detector

2.7.2 STRONG-FEED TRIP (SFT) ALGORITHM

The SFT algorithm detects strong internal faults. (See Figure 2-3.) The RFL 9300 enters a special LCCT (Local Current Comparison Trip) alarm mode if the SFT algorithm produces a trip enabled signal under the following conditions:

1. The necessary fault detectors were not activated to cause a trip signal to be issued.

2. This condition persists for 10 consecutive nested half-cycles of CT current.

This mode will persist for 5 seconds. During this time, the affected phase controller is disabled. The other phase controllers remain active to provide protection for all fault types, except open conductor. After the 5-second interval expires, the phase controller will re-initialize and attempt to come back-on line. As long as this condition exists, the LCCT alarm will be active. This alarm mode protects the RFL 9300 against A/D converter failures.

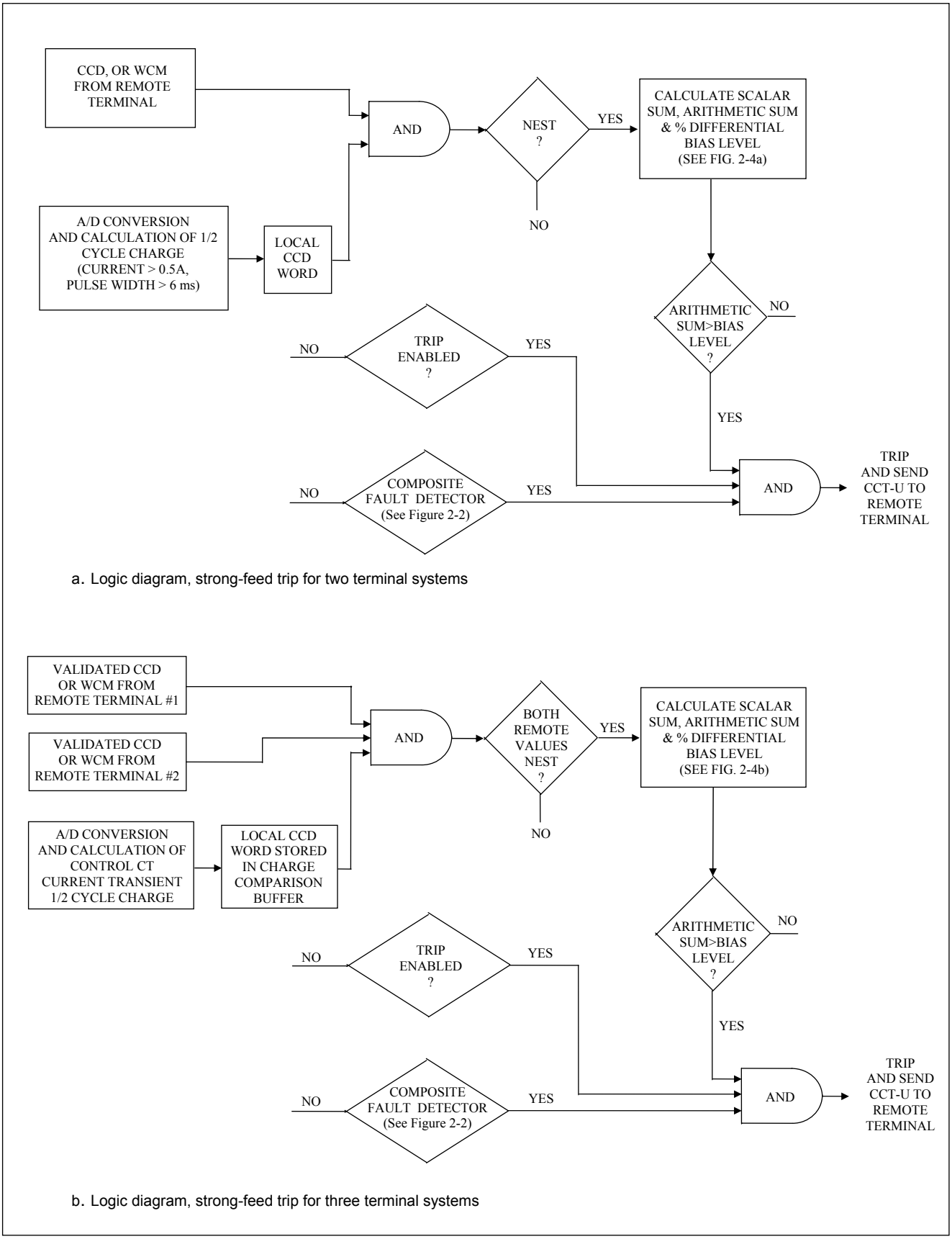
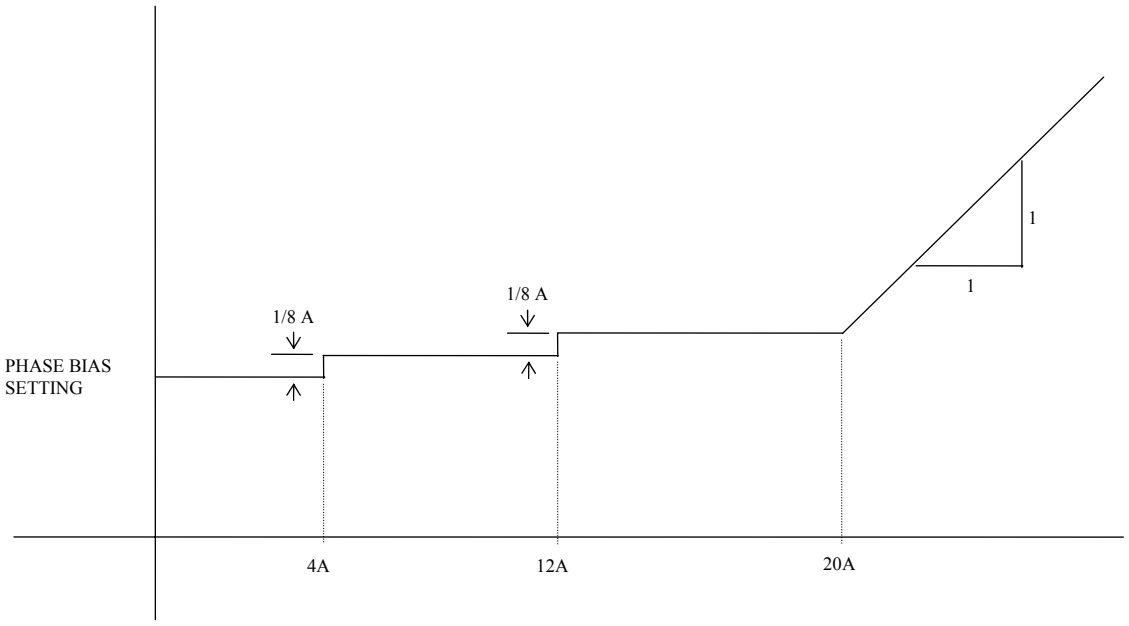
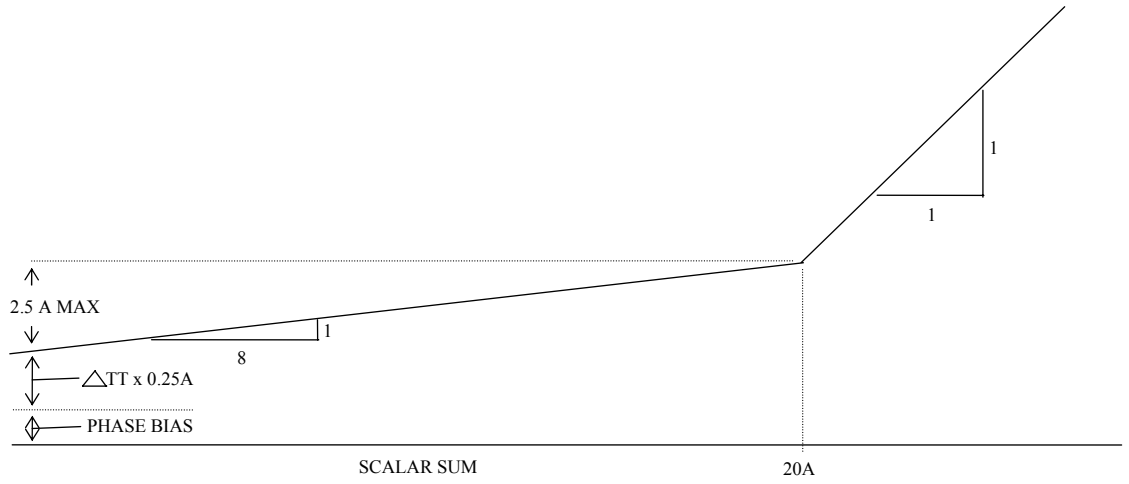


Figure 2-3. Logic diagram, strong-feed trips (for 2- and 3- terminal systems)



a. Differential Characteristic for 9300 in 2- terminal mode



△ TT = The total nest error of signals from both remote stations. The nest error of a received CCD message is the time tag difference between the adjusted received time tag of the received CCD message and a perfect nest with the local station half-cycle value. Received WCM messages are automatically assigned a 1 time tag error. Both received signals must nest within the same half-cycle value at the local station for this calculation to be done.

b. Differential Characteristic for 9300 in 3- terminal mode

Figure 2-4. Differential Characteristics for 9300 in 2- and 3- terminal modes

2.7.3 WEAK-FEED TRIP (WFT) ALGORITHM

In 2-terminal systems the SFT (Strong-Feed Trip) algorithm requires a received CCD or WCM message to be compared with a local CCD half-cycle integral value for the corresponding interval. In 3-terminal systems the SFT algorithm requires a composite CCD value derived from a validated pair of received CCD values, a pair of received WCM values, or a combination of CCD and WCM values to be compared with a local CCD half-cycle integral value for the corresponding interval. However, if the local station current is less than 0.5 Arms, there will be no stored half-cycle integral value for comparison. Also, if the fault at the local station is weak enough, there may be no fault detector activity. The WFT (Weak Feed Trip) algorithm would then be used to enable tripping for weak internal faults. (Refer to Figure 2-5.)

A weak-feed trip will be enabled if both of the following conditions are met:

1. The CCD value (2-terminal) or composite CCD value (3-terminal) received by the phase controller is greater than 1.5A rms plus the bias level setting. Note that if the bias control function is enabled for underground lines, the CCD value (2-terminal) or composite CCD value (3-terminal) received by the phase controller must be greater than 3A rms plus the bias level setting.

   The composite CCD value used in the WFT algorithm for 3-terminal applications is calculated as follows:

   a) If a CCD value received from one remote terminal is validated by a WCM from the second remote terminal the CCD value along with its adjusted received time-tag is used as is.

   b) If a pair of CCD values received from the remote terminals validate each other the adjusted received time-tag will be the average of the two. The CCD values will be resolved to this time-tag and summed to calculate the composite value used in the algorithm.

2. The current value recorded locally is less than 1.5 Arms.

If these conditions are satisfied and there is no composite fault detector, a weak-feed trip will not be enabled at the local station. Instead, a weak-feed trip signal will be sent to the remote station. If the remote station has the required number of active fault detectors, it will issue a trip signal and transmit a CCT-U signal back to the local station.

Receiving a UHST signal without the necessary fault detector conditions being satisfied, also will result in a WFT signal being echoed back to the sending RFL 9300. This will result in a faster trip response time, since the remote RFL 9300 does not have to wait for the zero crossing of the current waveform before it transmits the UHST signal.

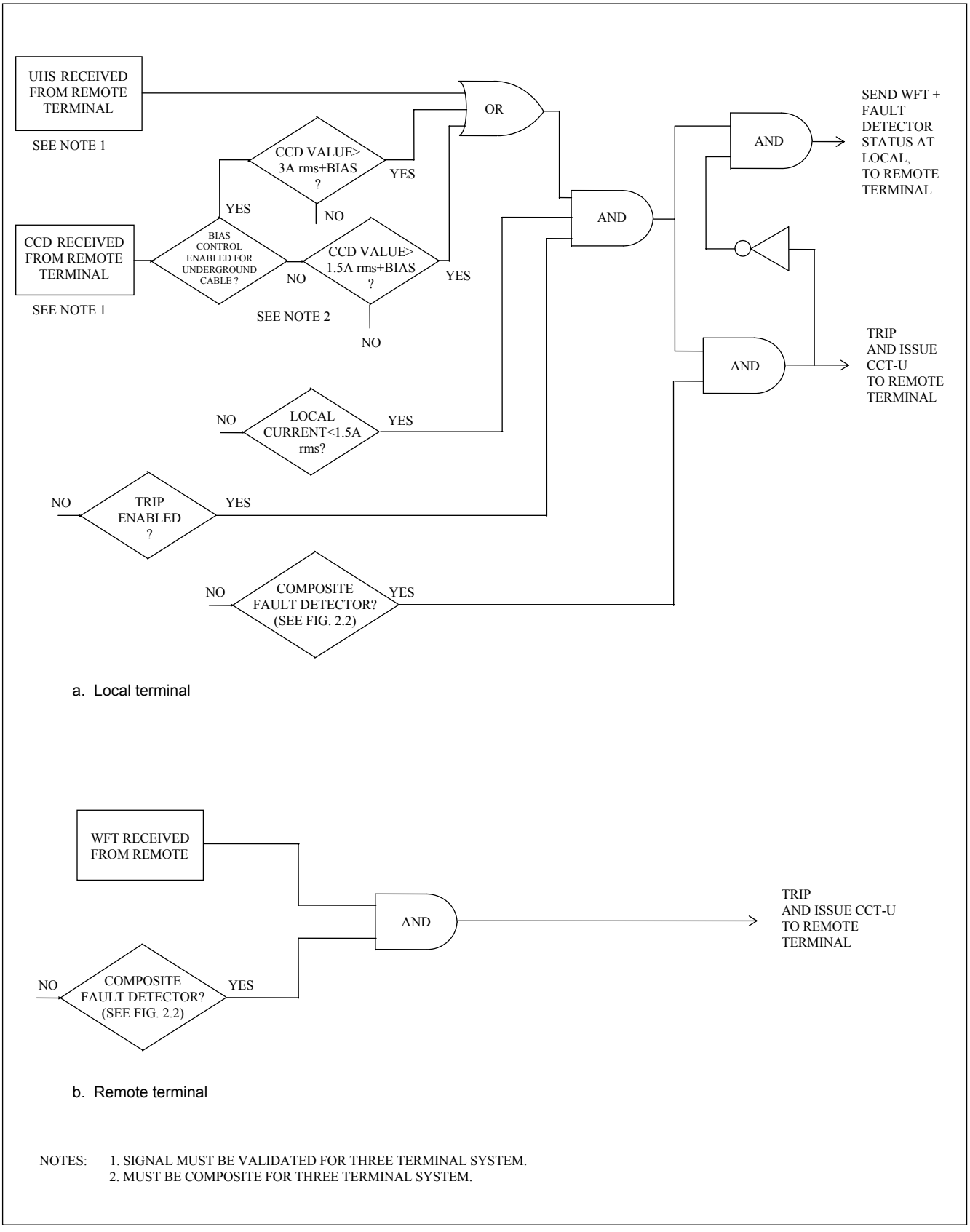


Figure 2-5. Logic diagram, weak-feed trip (for 2- and 3- terminal systems)

2.7.4 SWITCH-INTO-FAULT (SIF) ALGORITHM WITH COMMUNICATIONS

The RFL 93B PC modules will begin sending weak-current messages (WCMs) to the remote terminals after the breaker opens (2-Terminal systems) or transient CT control current (3-terminal systems) drops below 0.5A rms for 8ms. (See the description of the WCM in paragraph 2.7.1). If the breaker is open WCMs will be transmitted to the remote terminals at approximately 2ms intervals. The SIF algorithm provides a fast trip at any station that closes its main breaker into a fault (See Figure 2-6). After a WCM message is received (validated WCM message in the case of a 3-terminal system) the RFL 9300 uses a special formula to adjust its time-tag. From that point on it is treated as a CCD message with zero value and run through the SFT algorithm.

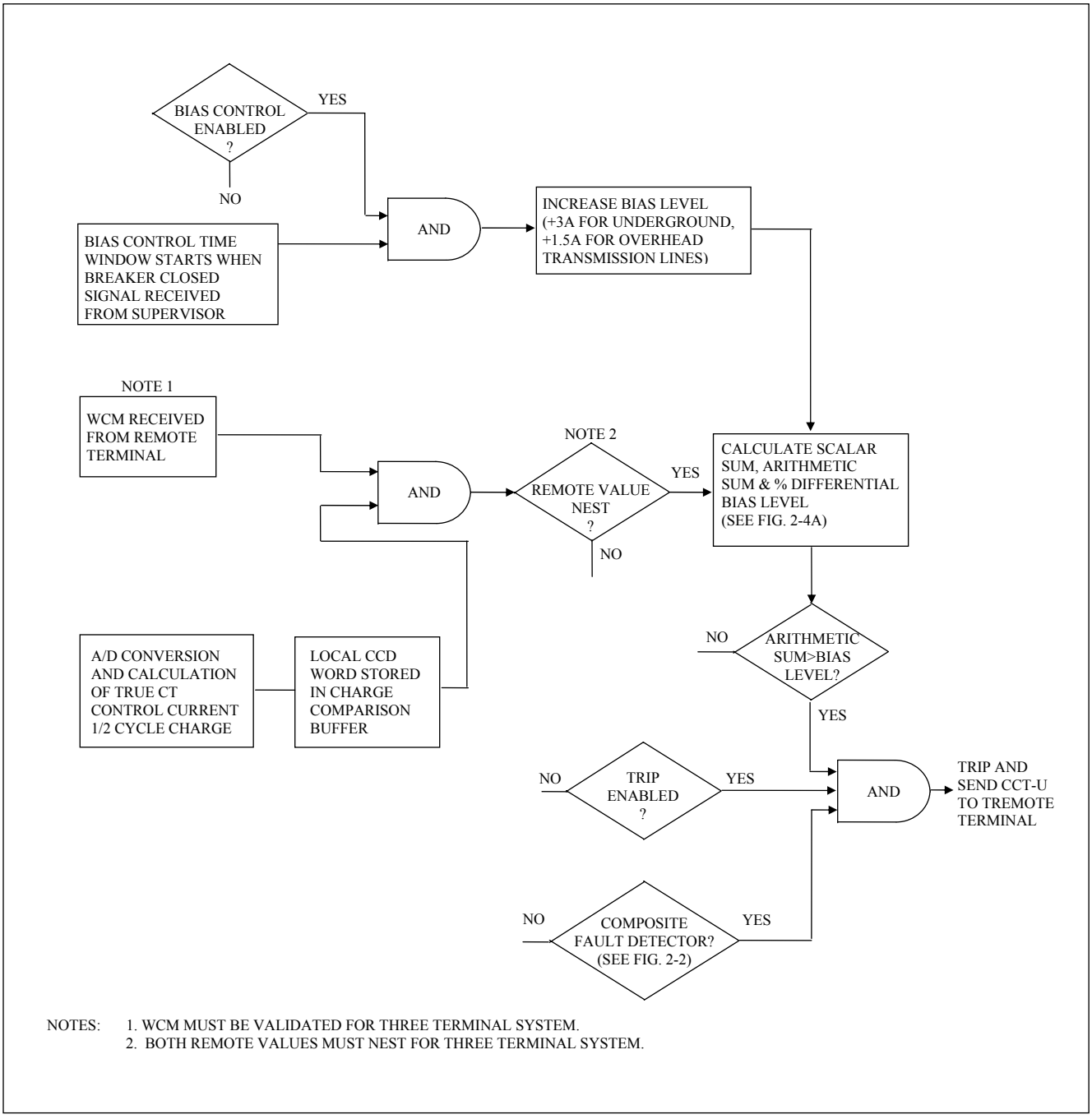


Figure 2-6. Logic diagram, switch-into-fault with communications (2- and 3- terminal systems)

2.7.5 ULTRA HIGH-SPEED TRIP (UHST) ALGORITHM

The UHST algorithm is a blocking algorithm that allows a trip at the remote station if a blocking current equal to - (11A - bias setting) $_{peak}$ has not been recorded (See Figure 2-7). The minimum blocking current allowed is - 7.5A peak. The RFL 9300 sends a UHST signal to the remote RFL 9300 whenever the local station detects that the input current's peak value is +12 amperes or more for 2 ms. This results in a much faster trip response at the remote RFL 9300 for strong internal faults, since it doesn't have to wait for the current waveform's zero crossing to send the signal.

For the ground subsystem, the blocking current is + (11A - bias setting) $_{peak}$ and the input current's peak value is –12 amperes or more for 2 ms. The minimum blocking current allowed is +7.5A peak.

For examples of UHST operation, see Figures 3-11 and 3-12 in Section 3 of this manual.

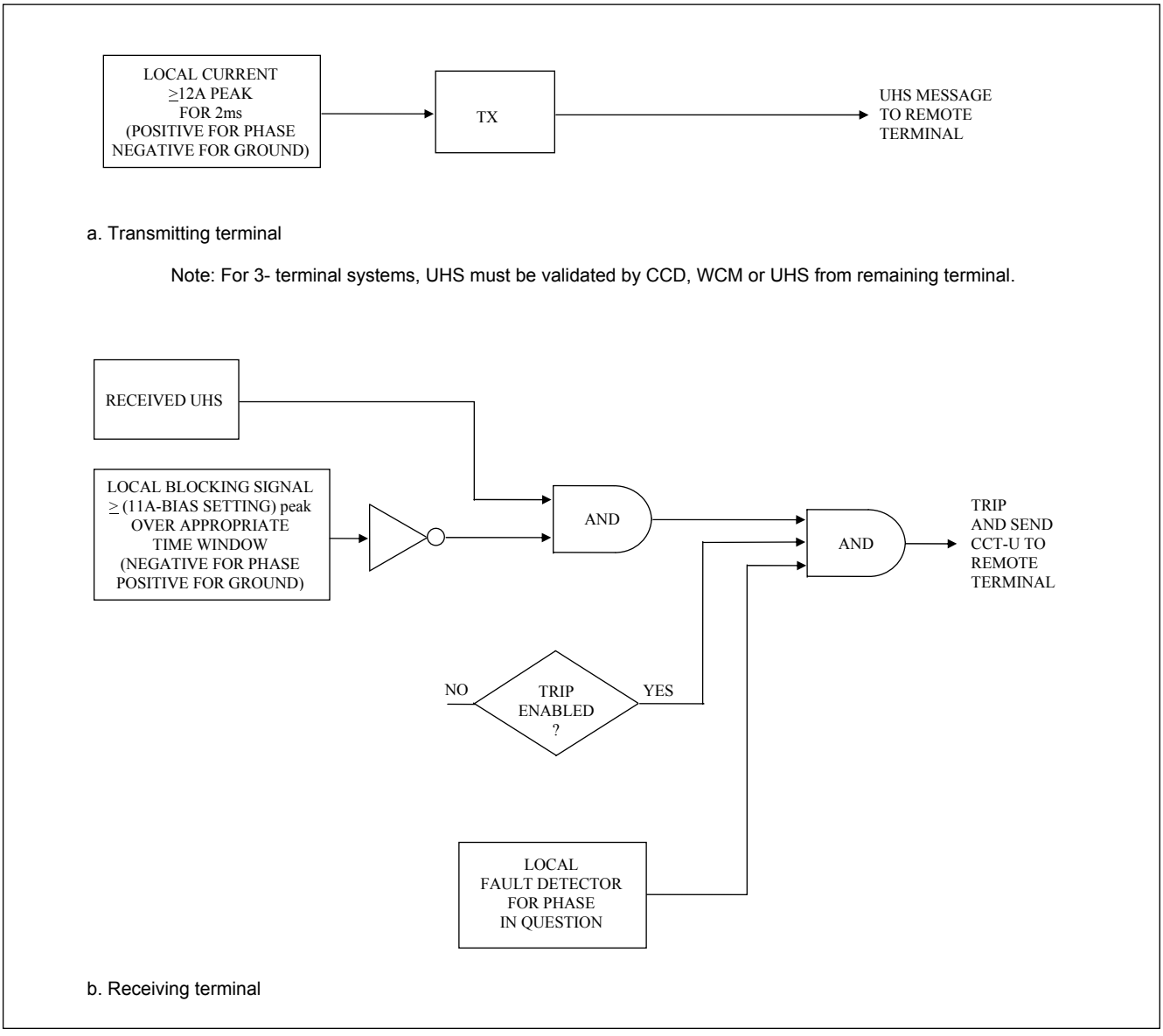


Figure 2-7. Logic diagram, ultra high-speed trip

2.7.6 OPEN CONDUCTOR ALGORITHM

The open conductor algorithm is the only non-backup mode function that does not rely on the communications link. (See Figure 2-8.) This function is enabled when the Phase A, Phase B and Phase C controllers all have a load current ≥ 1.5 Arms. From this point on the function looks for a loss of load current on one or more phases while at least one of the remaining phases carries at least 3A of load current. The open conductor requires fault detector supervision. The phase detector executing the algorithm must have a composite phase fault detector. A 500-ms Zone 2 timer starts when the open conductor condition is detected. This timer gives the Zone 2 protection relays time to clear the fault in the event that the fault exists beyond the remote breaker. If the open conductor condition is still present when this timer expires, the open conductor trip signal or alarm will be issued, depending on how the RFL 9300 is programmed.

Note that when the RFL 9300 is programmed for trip on open conductor, this function issues a trip signal, not a trip enable signal. This is because the fault detectors probably will no longer be active when the Zone 2 timer expires.

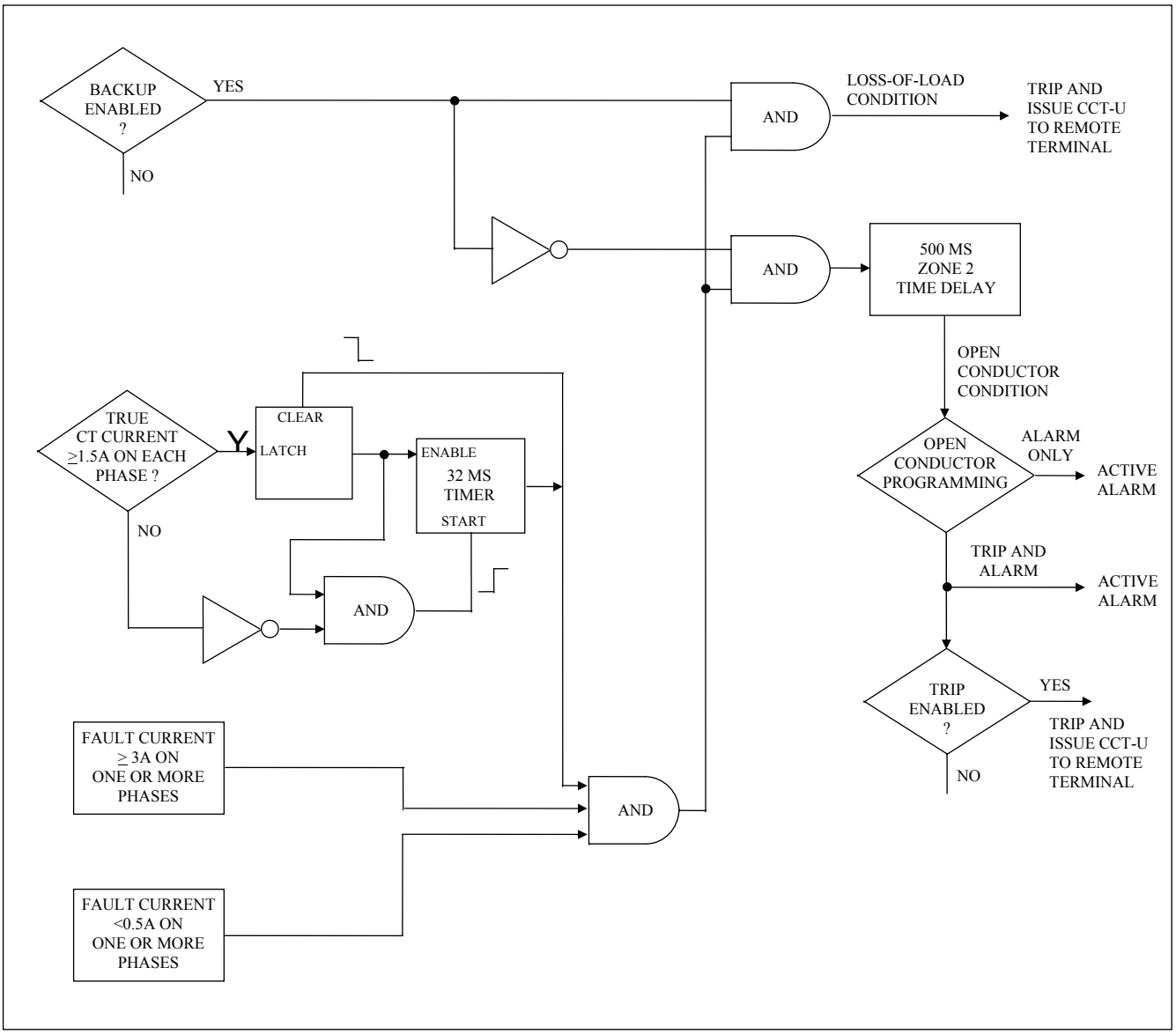


Figure 2-8. Logic diagram for open conductor and loss of load algorithm

2.7.7 STUB-BUS OPERATION

The transmission line between the local and remote stations may be disconnected via an open line switch at the local station. If a strong fault occurs at the local station (on the stub or within the double-breaker set-up for example) the local station may calculate a trip, and transmit a trip signal to the remote station. Since there is no fault at the remote station, the remote breaker should not be tripped. To prevent this type of trip, a simple “Stub-Bus” algorithm will be used:

The relay will require a disconnect switch signal (89B) to make the stub bus function active at the local station, protecting the stub. When the open disconnect switch is detected, the local station relay will react as follows:

1. A steady stream of WCMs will be transmitted to the remote station(s). All other control signal messages will be disabled.

2. All trip and control signal messages received at the local station will be discarded. This will effectively disable permissive trip at the local station. The remote station(s) will continue to function in a normal manner. Permissive trip will still be enabled due to the received WCM signals.

3. The local station relay will be forced into backup mode. This will enable the instantaneous overcurrent function. Inverse time overcurrent will still be available if the operator chooses to enable the function. The switch-into-fault and loss-of-load functions will be disabled when stub bus is active.

4. The DTT signal will remain active between stations.

Stations that do not have an active stub bus signal will operate in a normal manner. Standard fault detector requirements must be met in order to trip.

When stub bus is active, backup functions ENABLED or DISABLED will no longer appear on either the programming or read menus. Instead “SBACTIVE” will appear on the display in place of ENABLED or DISABLED. This will inform the operator that stub bus is active and the relay has been forced into backup mode (See Figure 2-9).

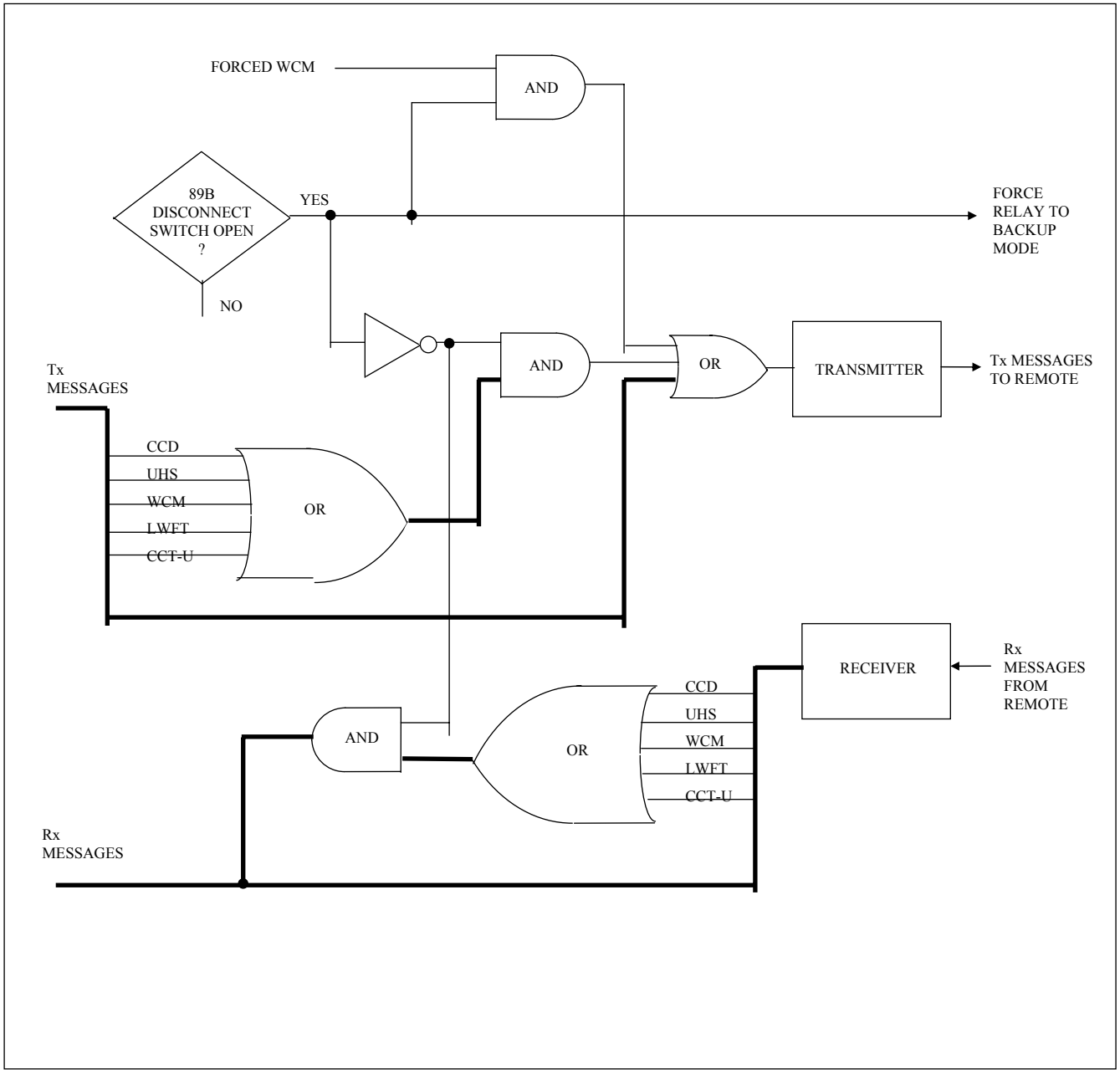


Figure 2-9. Logic diagram, stub-bus applications

2.7.8 EFFECT OF CHANNEL DELAY ON RFL 9300 PERFORMANCE

The RFL 9300 depends on accurate channel delay measurements for proper operation. Channel delay measurement errors approaching ±3.5 ms can be tolerated without producing false trip signals. This is a vast improvement over previous current differential systems. Most existing systems have difficulty dealing with delays that exceed 0.25 ms.

The "ping-pong" method of measuring channel delay has one basic limitation. If the sending and receiving paths have different delays they will not be detected. The RFL 9300 uses a method based on the measurement of zero crossings of the phase current waveforms to correct this. It is called "DML" (Delay Measurement based on Load current). The locally stored half-cycle integral value that is compared with the received CCD value is selected by time-tag comparison. The adjusted received time-tag must "nest" between the stored start and finish time-tags of the local value.

The "nesting error" is computed by the Phase A Controller and passed to the RFL 93B SV. This shows how close the adjusted time-tag comes to falling exactly half-way between the local start and finish time-tags. The RFL 93B SV uses the nesting error to correct the channel delay measurement value. The corrected value is the channel delay compensation (CDC) value that is distributed to all phase controllers. This correction is not made if there are active fault detectors anywhere in the system or if the Phase A load current is less than 1 A_{rms}.
This insures that system disturbances or line charging currents are not distorting the current waveform; this would interfere with accurate zero-crossing measurements. CDC will detect transmit and receive path differences in the ping-pong measurement and correct them. Channel Delay Compensation is not available when the relay is configured for 3-terminal operation. In this mode of operation the relay is working with transient CT control currents which will likely occur only when a fault detector is active.

Fault detectors are an integral part of the RFL 9300 system. Traditional relaying systems have used discrete fault detector relays to supervise tripping. In the RFL 9300, software techniques detect phase current waveform disturbances and supply the fault detector signals. Phase fault disturbances are noted by a lit LED indicator on the front panel of the affected phase controller module. The fault detector algorithms are the same regardless of whether the relay is configured for 2-terminal or 3-terminal operation i.e. they are based on true CT current readings at all times.

All phase controllers execute a bias-control function to protect against false-tripping caused by line-charging current during breaker turn-on. The function is enabled through the key pad. Bias control protection is provided for a maximum of 1 second from the time that breaker closing is detected. The duration of the protection is programmable through the key pad in 50-ms steps, up to a maximum of 1 second. This is shown in Figure 2-6.

2.8 BACKUP MODE OPERATION

Except for the open conductor algorithm, the RFL 9300 cannot execute any of its charge comparison protection algorithms if the communications channel to the remote station is disrupted. If a communications failure occurs, some degree of protection is still provided. Whenever the RFL 93B CC Communications Controller detects a communications failure, it signals the phase controllers to enter the backup mode. If the operator has enabled backup (through the keypad), the local RFL 9300 will enter backup mode, disable permissive trip signals, and execute the backup protection algorithms. Some form of fault detector supervision is still required to cause a backup trip signal to be issued. As long as communications still exist between the phase controllers and the supervisor controller, one additional local RFL 9300 fault detector (besides the phase controllers' own fault detector) must be active for a backup trip signal to be issued.

If the operator has enabled the backup mode, the phase controllers can enter backup mode without being commanded to do so by the RFL 93B SV. This will happen if all four phase controllers at the local terminal have an active alarm. This condition can occur if there is a problem with the parallel bus linking the RFL 93B SV with the phase controllers. It also can occur if the RFL 93B SV is malfunctioning. Then only the phase controllers‘ local fault detector is required to supervise a backup trip signal.

While operating in backup mode, each phase controller will continue to execute all protection algorithms. It will still attempt to transmit all signals, including trip signals, to the remote terminals on the chance that they may get through. The only difference is that now, backup trip signals are enabled while permissive trip signals are disabled.

The protection algorithms listed below are active when a phase controller operates in backup mode.

2.8.1 SWITCH-INTO-FAULT WITHOUT COMMUNICATIONS (SIF W/O C)

The (SIF W/O C) algorithm looks for individual phase currents greater than 10 Arms lasting at least 16 ms. It enables a backup trip signal if this condition is detected. This function will detect the presence of an internal fault when the local breaker is closed into the fault with the remote breaker still open. The function will remain active for 50 ms after breaker closing. (See Figure 2-10.)

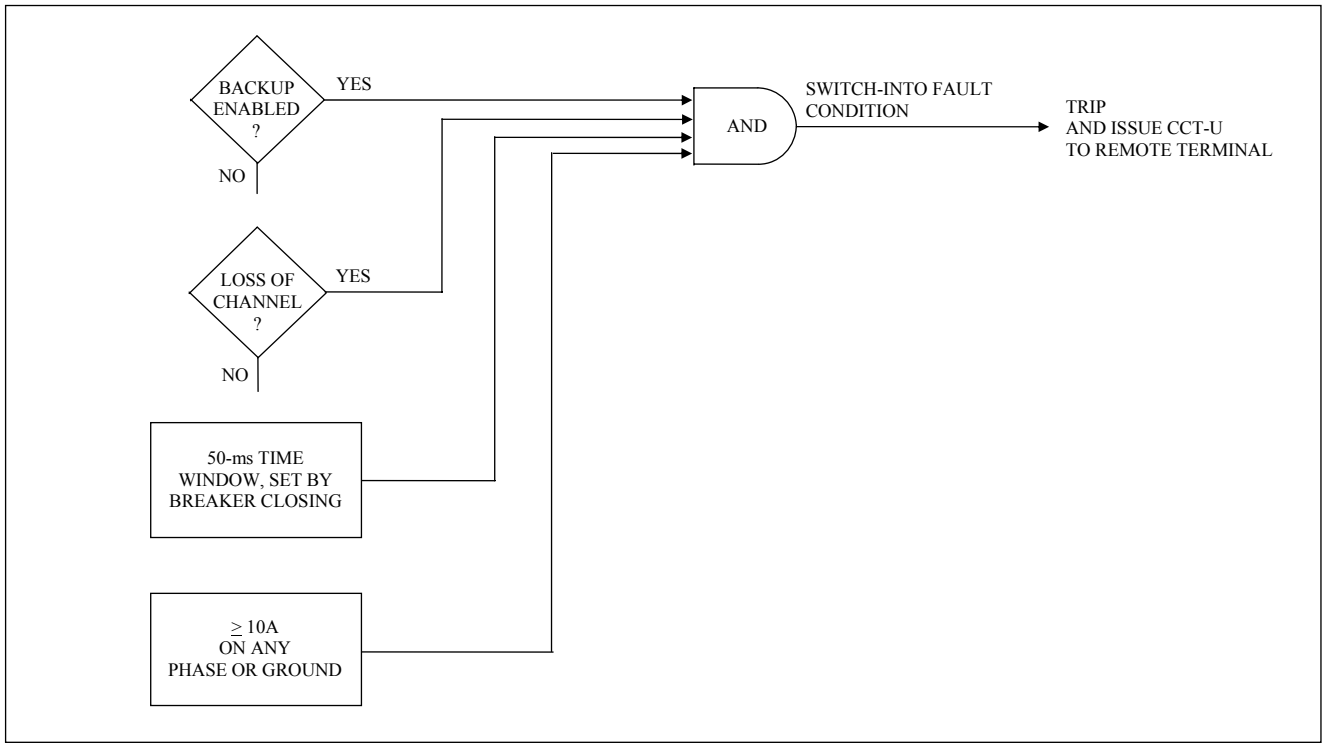


Figure 2-10. Logic diagram, switch-into-fault without communications

2.8.2 OVERCURRENT ALGORITHM

This is strictly a fuse type of protection. Instead of instantaneous peak readings, half-cycle integral values are used to determine if the overcurrent setting has been exceeded. The overcurrent setting is programmed by the operator through the keypad. There is a separate setting for the phase overcurrent (A/B/C) backup and the ground overcurrent backup.

2.8.3 LOSS-OF-LOAD ALGORITHM

In the loss-of-load protection algorithm (Figure 2-8), the controller looks for a loss of load on one phase while one or both remaining phases carry a strong load current (greater than 3 amperes). It also looks for a loss of load on two phases while the third carries a strong load current (greater than 3 amperes). These conditions suggest that the remote breaker has opened, but since one or more phases is carrying strong current, there is an internal fault. The phase (A, B, C) currents must be $\geq$ 1.5 A to enable the loss-of-load algorithm.

The loss of load function allows sequential tripping in situations where communications may still be established in one direction. If an internal fault condition exists and the breaker at the remote station opens, phase current in the faulted phase(s) will remain high. The phase current on the unfaulted phase(s) will fall to line charging levels. The remote station could then trip through a CCD message received from the local station. The local station would trip on loss-of-load after the remote breaker opens.

2.9 DIRECT TRANSFER TRIP (DTT)

When the DTT initiate signal is asserted, the transmitting terminal sends ten consecutive DTT words. This is followed by a refresh of two DTT words every 40 milliseconds. The DTT refresh pattern continues as long as the DTT initiate signal remains active.

At the receiver terminal, two consecutive received DTT words are required to qualify the signal. Once qualified, a single received DTT word will keep the signal active. A 100 ms drop-out timer at the receiver terminal bridges over the holes in the refresh pattern. DTT trip release at the receiver terminal will be delayed until DTT trip coil current is no longer sensed and there has not been a DTT signal received for 100 ms.

2.10 DISPLAY CONTROLLER

The display controller has a 15-character display and a keypad for operator interface, and an RS-232 serial port. It monitors and enables the trip signals. (See Section 5 for instructions.)

By using the display and keypad, the operator can modify the protection algorithms executed by the phase controllers to meet system requirements. These variables are stored in non-volatile memory on the display controller. The "official" copy of these variables is stored in non-volatile memory on the RFL 93B SV. The 15-character display is used for alarm annunciation and to display many other system parameters. (A complete list of programmable parameters appears in Section 6 of this manual.)

The display controller is connected to the RFL 93B SV through a RS-485 serial link. A serial link to external equipment is provided through the RS-232 port located on the RFL 93B RELAY I/O assembly. This port is also controlled by the display controller. The microcontroller on the display controller has only one serial port that must be shared between these two serial links.

If any system or communications alarms are active, the RFL 93B SV will signal the display controller. Each alarm message has an error number that appears on the display. The display controller monitors the trip signals; it generates alarm messages if any error conditions are detected.

The display controller also monitors the outputs of the Contact Current Sense circuits. It will light the appropriate indicator on the Display Module whenever it senses contact current. The status of all front panel indicators (except the two-color PROTECTION EN/DIS indicator) are saved in non-volatile memory. If the RFL 9300 is turned off or loses power for any reason, these indicators will reflect their previous status when power is restored.

When a phase controller trip signal is detected, the output trip relay is latched. The phase controller will continue to apply the trip signal until either of the events listed below occurs, whether or not the fault detectors remain active.

1. A breaker-open signal is received from the Supervisor.
2. A breaker-open signal has not been received from the Supervisor and 200ms has passed since the fault condition was last detected.

The display controller will utilize the trip release algorithm selected by the operator (parameter #145) to unlatch the trip relay. Three methods are available for unlatching the trip relay:

1. Output trip will unlatch without delay when both the internal trip and DC trip current sense signals are no longer active.
2. Output trip will be unlatched 100ms after the internal trip signal is no longer active.
3. Output trip will be released with 0ms delay when the internal trip signal becomes inactive. (Note that the internal trip signals are supplied by the Phase Controllers)

It is very useful for diagnostic purposes, to know which algorithm calculated the trip signal. Sequence of Events data, available via the RS-232 port, includes this fault algorithm information (See Figure 2-11)

If the dc current flowing through the trip contacts is $>$ 0.1 Amp dc and lasts for more than 500 ms, ALARM No. 27 operates, indicating a breaker failure or interposing relay failure.

If the dc current level is not detected, there is no alarm, and the TRIP LED(s) do not operate, however the A/B/C/G targets still operate. The breaker trip indication would now have to come from the interposing tripping device, if one is used.

When a DTT trip signal is detected, the DTT trip relay is latched. The display controller will unlatch the trip relay 100ms after the DTT trip signal is no longer detected so long as there is no current flowing through the trip contacts.

If the dc current level (now 0.1A) is not sensed, there is no alarm. If the current is sensed for more than 500 ms, ALARM No. 24 is operated. This indicates a failure of the lockout relay (Device 86), interposing tripping relay (Device 94), or circuit breaker (Device 52), which should be operated by the 9300 output relay contact and should interrupt the dc current in the DTT output contact.

If dc current flowing through the trip contacts is detected for an interval exceeding 60ms and a trip signal has not been issued, ALARM No. 25 operates, indicating a trip relay contact failure or current sense circuit failure.

The RESET switch on the front of the Display Assembly serves a dual purpose. When it is pressed, as long as there are no active trip signals, all LED status indicators on both the Display and Single-Pole Assemblies will be reset and a 3-second LED test will be triggered on both. After the LED test is completed, the remaining modules except for the comms cards in the RFL 9300 will execute a 3-second LED test. If there are any active trip signals on the main chassis, a “TRIP ACTIVE” message will appear on the display and the reset signal will have no effect. Even if there are active trip signals detected on the main chassis the reset signal will still be transmitted to the Single-Pole logic where LED status indicators will be reset only on unfaulted phases without active trip signals. The RESET switch is also used to reset any alarms generated by the Display Controller. Alarms transmitted to the Display Controller by the RFL 93B SV and the Single-Pole logic will not be reset when the RESET switch is pressed. These alarms will only be reset when the alarm condition itself disappears.

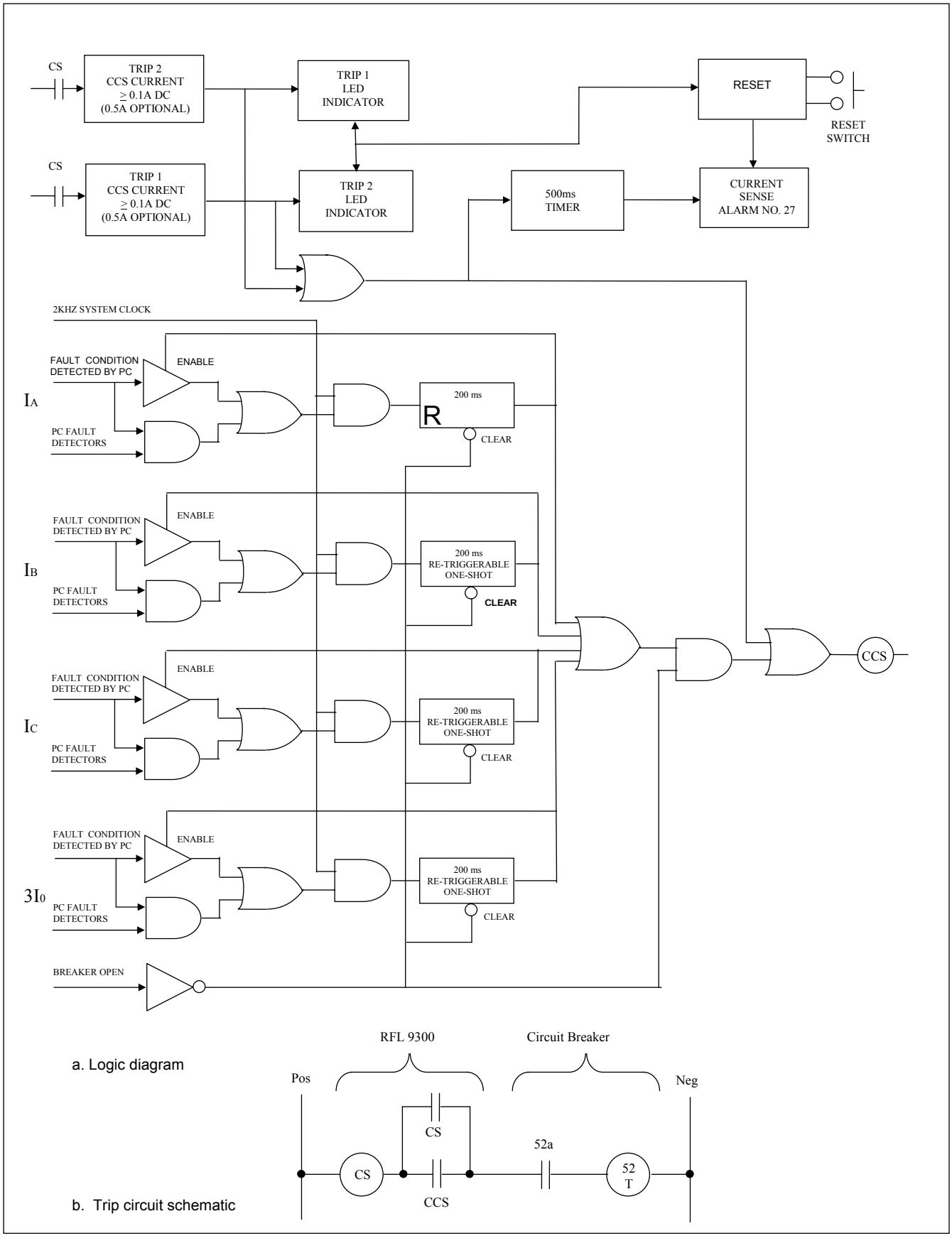
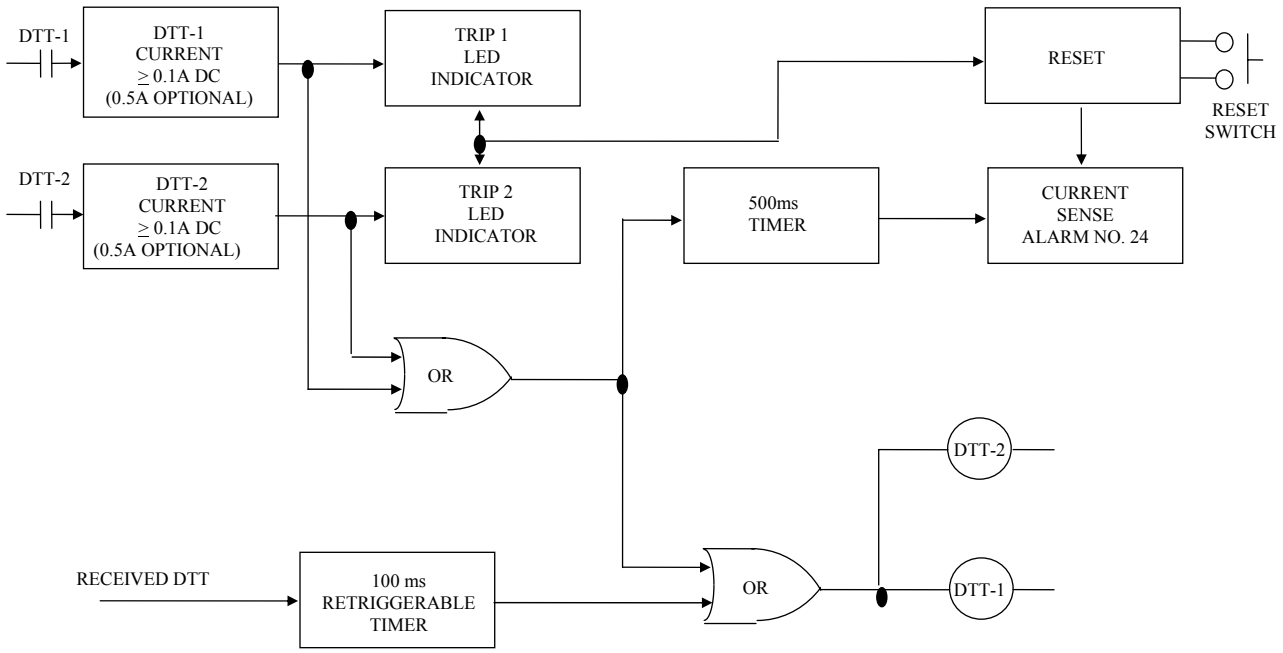
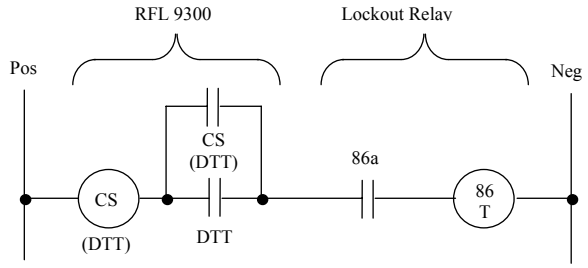


Figure 2-11. Logic diagram, trip seal-in



a. Logic diagram



b. Trip circuit schematic

Figure 2-12. Logic diagram, DTT trip seal-in

2.11 OSCILLOGRAPHY BOARD

The Oscillography Board is an extension of the display controller. It is directly connected to the display controller through an 8-bit bi-directional data bus and additional control lines. When a trip event occurs, the oscillography board will record and store ten cycles of all four measured trip currents as well as the trip output signals. Five cycles of pretrip and five cycles of post trip information will be saved. The four current signals are read by an 8-bit analog to digital converter and kept in a rolling buffer by the controller. In the event of a trip, the buffer is time tagged and a new buffer will be opened.

Five buffers are available to store oscillography data for five of the most recent trip events. Section 6 of this manual describes how the oscillography data can be accessed.

The oscillography board also holds the alarm annunciator.

The trip signals that originate on the phase controller modules and the DTT signal from the RFL 93B SV terminate on the Oscillography Board. These signals are applied to a programmable logic chip along with various control signals originating on the display controller and Relay I/O module. The combination logic circuit programmed into this chip insures that once issued, the trip signals applied to the output relays remain latched until released by the display controller. If the display controller disables trip, the trip signals have no effect.

2.12 IRIG-B

The RFL 9300 has the ability to synchronize its internal real time clock with an external IRIG-B clock source. The IRIG-B signal enters the RFL 9300 via a BNC connector on the Relay I/O module. The signal is then routed to the oscillography board, which demodulates the IRIG-B signal and feeds it to an embedded controller, which is also used for the oscillography feature. The controller updates its battery operated real time clock based on the received IRIG-B signal. In the absence of IRIG-B, the APRIL setting of the display clock will be used. IRIG-B is only used for time stamping alarm and trip events.

2.13 DIAGNOSTICS

Various diagnostic routines are continuously being executed while the RFL 9300 is operating. These include the following:

1. During normal program execution, a different programmed variable is tested and then passed to all phase controllers at 4-second intervals. This means each controller will have its programmed variables refreshed once every 32 seconds. The display controller also stores a copy of these variables but the "official" copy resides on the RFL 93B SV.

   The display controller also refreshes its stored programmed variables at 32-second intervals by requesting a different variable from the RFL 93B SV every 4 seconds.

2. Periodically, each phase controller passes a parallel bus test request message (55H) to the RFL 93B SV. The RFL 93B SV must return a response message (AAH) within a preset time limit or the test will fail. The RFL 93B SV executes the same test with all phase controllers in the opposite direction. The only difference is that the RFL 93B SV will alarm if any one of the phase controllers does not respond properly. The phase controller alarm applies only to the controller conducting the test.

3. All messages passed between controllers at the local RFL 9300 station consist of three bytes: address, data, and security code. The security code is the XOR of the data and address bytes. All received messages are tested to insure that the security code is correct. The phase controllers will alarm if the frequency of corrupted messages exceeds 1 in 16.

   The RFL 93B SV does not alarm on bad messages received from the phase controllers. It assumes that if there is a problem receiving messages from the phase controllers, there is also a problem on the other end and the phase controllers will alarm. Many of the messages passed to the phase controllers, including programmed variables and CDC values, require an acknowledge sequence. This is the same three-byte message returned to the RFL 93B SV. The RFL 93B SV will continue to transmit the message until the proper acknowledge is received. The parallel port bus test messages between controllers have deliberately been given the lowest priority. If a given message is continuously being repeated because a proper acknowledge has not been received the bus test message will never be sent. This will result in a parallel port bus test alarm (Alarm 34). The same type of error checking exists for all messages passed between the RFL 93B SV and the display controller board.

4. The 2-kHz system clock generated by the RFL 93B SV is the heartbeat of the system. The accuracy of this clock is critical because of the differential nature of the RFL 9300 system. Each phase controller monitors the period of this clock to insure that its period lies between pre-defined limits that are application dependent. Since each phase controller will base the test on its on-board crystal, the RFL 9300 has four independent crystal based frequency discriminators monitoring this clock. If a phase controller detects an error in the clock, it will reset and attempt to re-initialize.

5. The phase controllers and the RFL 93B SV both monitor the CDC values supplied by the Communications Controller. The maximum value that will be accepted is 31 ms for a 30-bit message pair and 29 ms for a 15-bit message. If a value exceeding the allowed range is received, the CDC message is not acknowledged. If the condition is not corrected, the transmission of CDC messages will quickly tie up the local communications channel and cause parallel port alarms.

6. The local 9300 verifies the remote 9300's transmit address on a periodic basis using a TDM message. It alternately requests the remote station's least significant transmit address byte, then its most significant transmit address byte, at 2.5 second intervals. This will not tie up the communications channel and will insure some level of protection against any possible undetected switching of the communications link between stations.

SECTION 3: APPLICATIONS

3.1 INTRODUCTION

The RFL 9300 is suitable for high-speed protection of both overhead and underground ac transmission and sub-transmission lines. All line lengths and voltage levels can be accommodated.

Since the RFL 9300 operates from current-only, it shares properties with all current-based schemes. These include the following:

1. Mutual induction has no effect on performance.

2. Current reversals are easily handled.

3. There is inherent blocking during swing conditions.

In addition, the RFL 9300 is particularly well-suited to many difficult or unusual applications. Many of these applications will be discussed in this section.

3.2 SERIES COMPENSATED LINES

The RFL 9300 can be used to protect series compensated lines, or lines adjacent to series capacitors. Series capacitors create three conditions that can affect the protection:

1. Voltage inversion.

2. Off-normal frequencies (particularly subnormal frequencies).

3. Severe phase unbalance.

These conditions do not affect the RFL 9300, because it is current-only, not frequency-dependent, and uses per-phase operation.

3.2.1 VOLTAGE INVERSION

The relay voltage will be inverted if the impedance between the fault location and the relay potential location is net capacitive. (See Figure 3-1.) A similar inversion may take place on external faults where the adjacent line has line-end series capacitors. These voltage inversions affect distance relays, but they will have no effect on current-only relays like the RFL 9300.

3.2.2 SUB-NORMAL FREQUENCIES

There is some resonant frequency below the fundamental where $| Z_C | = | Z_S + nZ_L |$. When the system is shock-excited by fault F, the system may oscillate at this low frequency. Off-normal frequencies may affect distance relays, and current-only relays that are based on operation at the fundamental frequency.

The RFL 9300 is based on the principle of Conservation Of Charge, which is independent of frequency. Its operation is not affected by the off-normal frequencies that may appear during the post-fault period. These off-normal frequencies may be caused by series capacitors or other power system parameters.

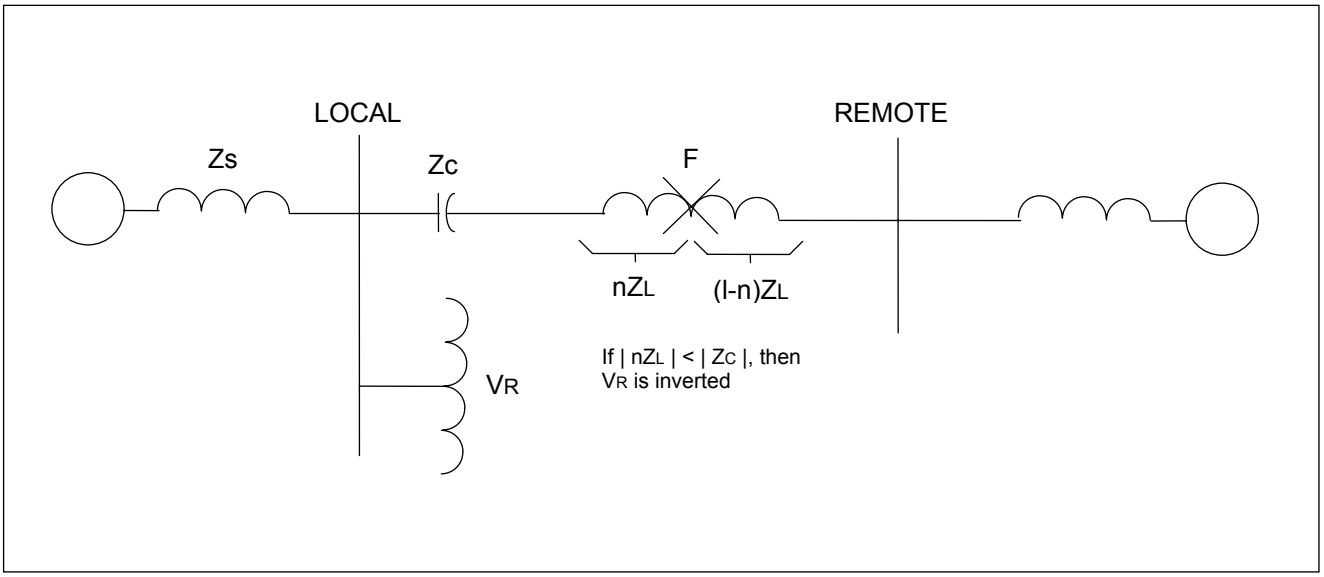


Figure 3-1. Voltage inversion

3.2.3 PHASE UNBALANCE

Severe phase unbalance may occur in series-compensated power systems. This unbalance may be caused by non-symmetrical behavior (flashing or reinserting) of the gaps or other capacitor protective devices. (See Figure 3-2.)

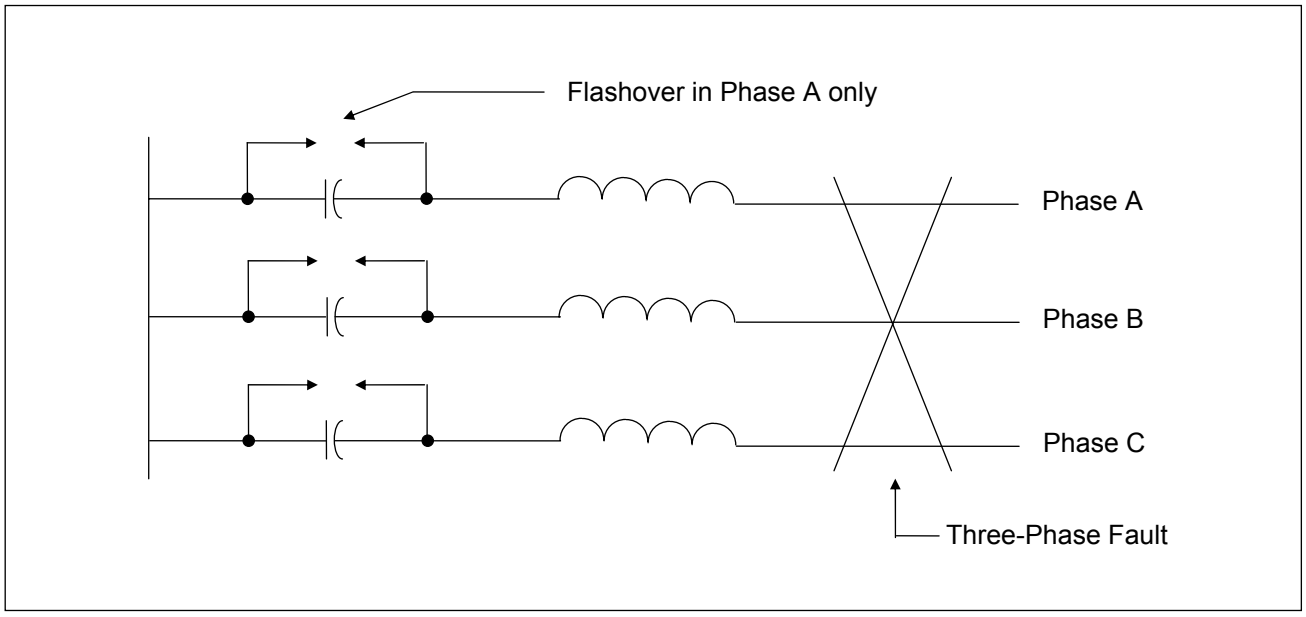


Figure 3-2. Phase unbalance

Phase unbalance causes circulating zero-sequence and negative-sequence currents. These may affect the operation of distance relays, directional overcurrent relays, and current-only schemes that compare composite quantities. The RFL 9300 is unaffected by phase unbalance because it operates on a per-phase basis; each phase current and the $3I_0$ current are compared separately.

3.3 VERY SHORT LINES

Figure 3-3 shows a condition where the ratio between the source impedance and the line impedance is very high. This condition may occur on very short lines, or longer lines connected to a weak source.

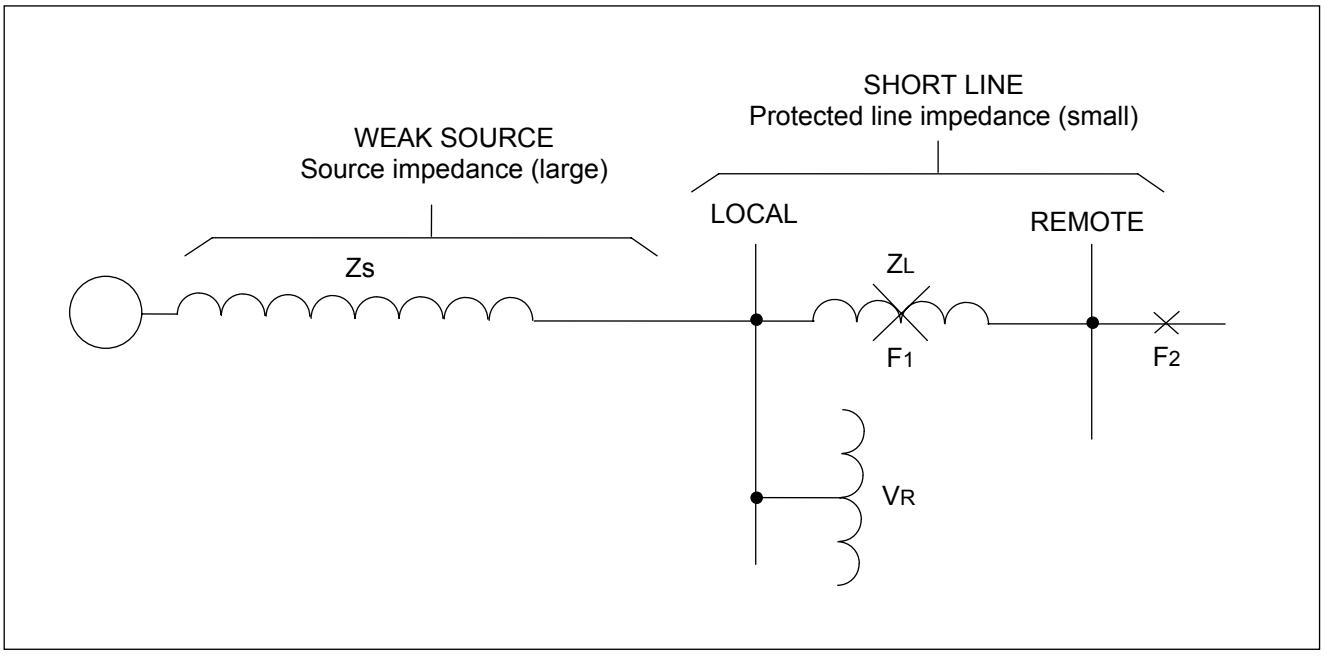


Figure 3-3. High source-to-line impedance ratio

If Z_S is much greater than Z_L, V_R is very small for both faults (F1 and F2). This makes it difficult for a distance relay at the local station to distinguish between a fault at F1 and one at F2. Current-based relays compare the currents (or charges) at the local station to those at the remote station. This makes it easy to tell whether the fault is internal or external to the protected line.

3.4 EFFECT OF INFEED/OUTFEED

Consider the 3-terminal transmission line shown in Fig 3-4. Each of the terminals will pass current to the fault. The impedance seen by relay Rr is:

$$Z' = Zr + Zf (1 + Im/Ir)$$

Distance relays must be concerned about over-reaching or under-reaching for this fault. Current-based relays base trip decision on the arithmetic sum of the currents (or total charge) entering/exiting the zone of protection. Therefore they are not subject to the effects of infeed or outfeed currents supplied by a third terminal.

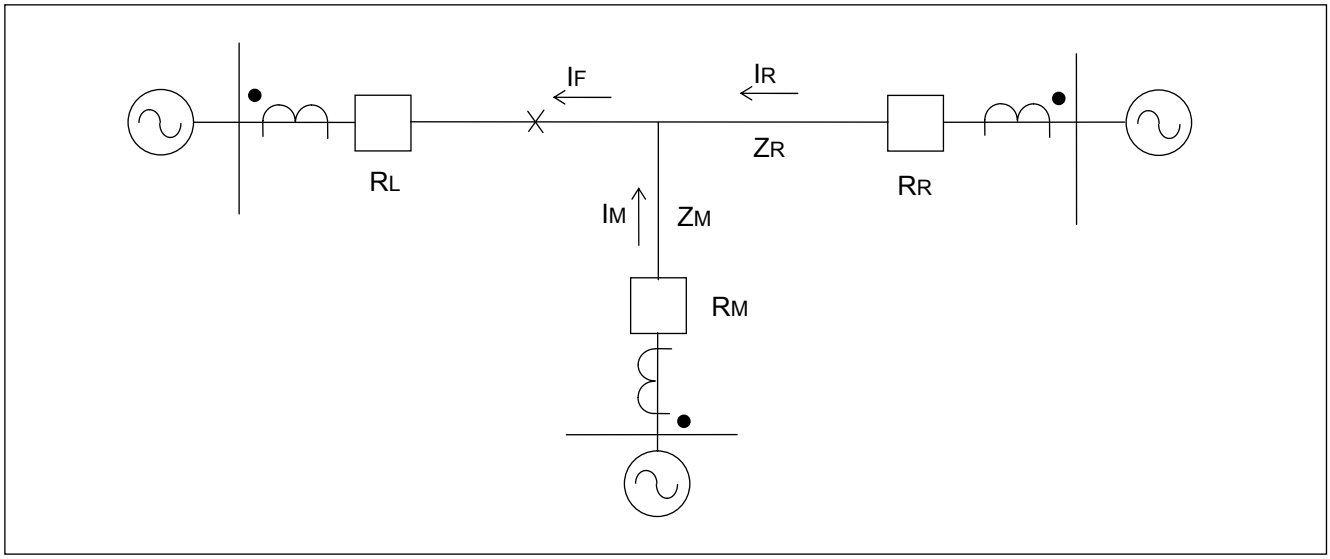


Figure 3-4. Effect of infeed/outfeed

3.5 STRONG BUS TIE

Consider the case where a strong bus tie exists between Bus M and Bus R as shown in Fig. 3-5. If a strong internal fault exists near Bus R and outfeed current can flow through terminal M. This would cause a distance or directional relay at terminal M to see the fault as external. They will not clear the fault until relay R opens.

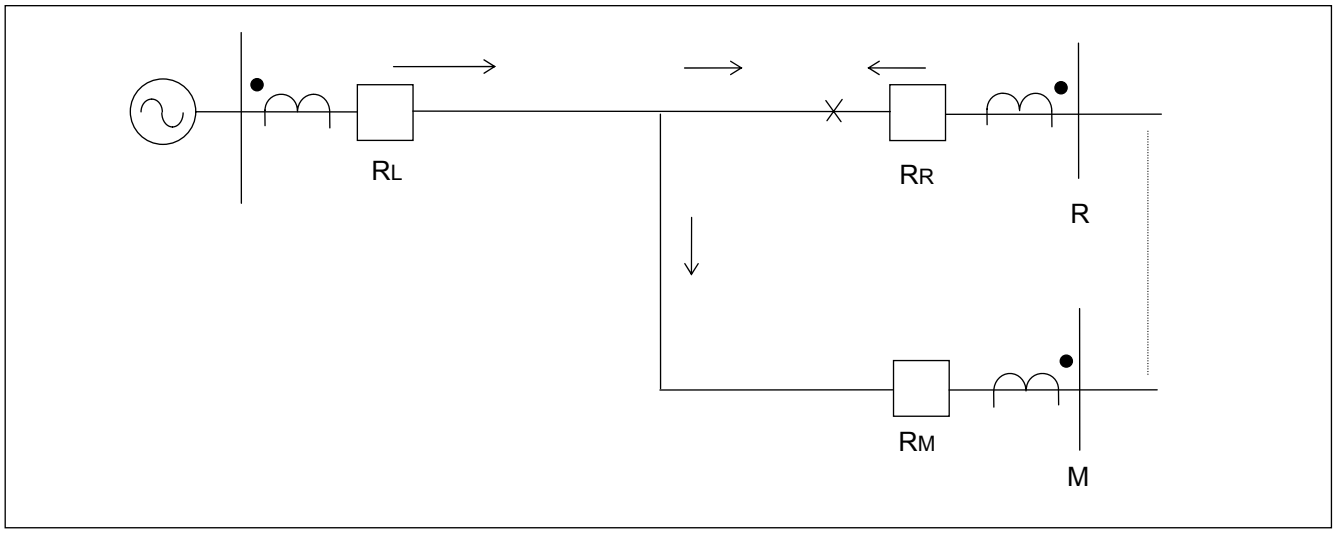


Figure 3-5. Strong bus tie

3.6 HIGH-RESISTANCE GROUND FAULT

Heavy through-load coupled with a high-resistance ground fault may create an "outfeed" condition that is very difficult for most relay schemes to detect. (See Figure 3-4.)

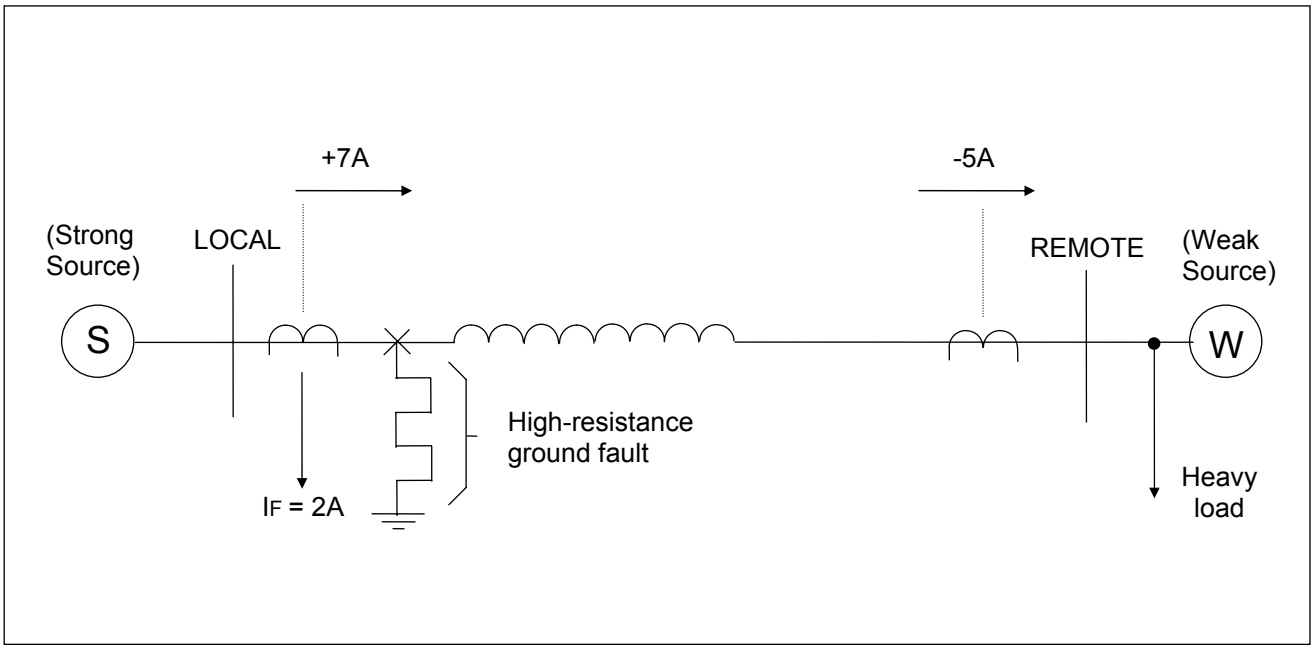


Figure 3-6. High-resistance ground fault with heavy through-load, causing an outfeed condition

Figure 3-7 is a polar diagram with the currents on the faulted phase in Figure 3-6 plotted. Since the RFL 9300 has a "rainbow" characteristic, the relay correctly trips.

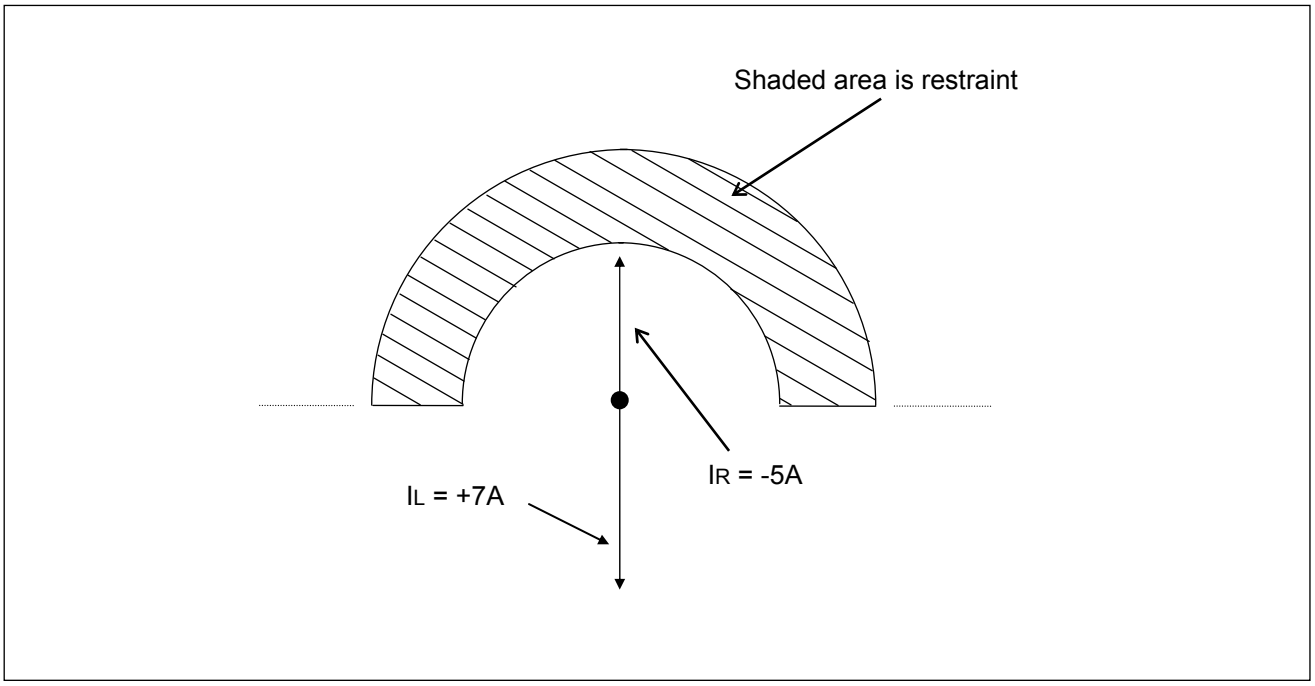


Figure 3-7. Polar diagram,
(shows how the RFL 9300's "rainbow" characteristic provides proper tripping for high-resistance ground faults)

3.7 PREFAULT LOAD SUBTRACTION

The current flowing through a transmission line is determined by the phase angle difference between the generation at either bus. This angle difference is generally in the ten to thirty degree range. So long as there is no internal fault the currents entering the zone of protection will equal the currents leaving it. It's true that there will be line-charging current differences but for the purposes of this discussion they can be neglected. For 2-terminal applications the currents at the terminals are generally well behaved. The time correspondence between the half-cycle current integrals at the local and remote terminals is fairly easy to maintain.

When an internal fault occurs the generator angles come into play. The fault tends to separate the system and the current flow to the fault is now a function of the generator voltage and line fault impedance. For phase-to-phase and 3-phase faults the phase angle between the local and remote terminal currents is approximately equal to the generator angle difference. This relationship is modified to some degree for ground faults because of fault resistance. Since both terminals see the same currents, through faults do not present a phase angle problem. The end result of this discussion is that for 2-terminal systems we can expect phase angle differences for internal faults but since the CCS "nesting" tolerance approaches 4ms (90 degrees) these angular differences pose no particular problem for the relay.

When 3-terminal systems are considered the situation changes radically. A fault simulator was used to generate an external fault on a tie line between terminals M and R in a 3-terminal system similar to that represented by the single line diagram shown in Figure 3-8. The waveforms shown in Figure 3-9 represent the Phase A current seen at each of the terminals. The generator angle difference was 40 degrees. Admittedly a generator angle this large is rare but it's useful for purposes of illustration. Note that even though the waveforms represent an external fault there are wide phase angle shifts for the relay to contend with. This phase shift cuts into the 4ms margin allowed for communications channel delay error between the terminals.

The effects of generator angles and fault impedance can be eliminated if only the fault current component of the total post fault current is considered. The concept is best illustrated by considering the 3-terminal one-line diagram shown in Figure 3-8. The fault type being considered is a symmetrical 3-phase fault. This is easy to visualize as it consists of only positive sequence currents. The fault is represented in a) by a shorting switch. In b) the shorting switch has been replaced by a pair of voltage generators with the same value and opposite polarity. Since the voltage from the fault to neutral is Vf - Vf =0 this is a valid substitution. Using superposition techniques the equivalent network is now broken down into two parts as shown in c) and d). Let's consider the voltage Vf to be the open circuit voltage at the fault point just prior to the fault. In d) we see that voltage source Vf will oppose the flow of any current in that branch of the circuit. Because the circuit branch with voltage source Vf has no current flow it can be removed from the circuit and we end up with e) which is equivalent to the original circuit in a). The only difference is that the reactances have been converted into their Thevenins equivalent values. Therefore the current flowing in the equivalent circuit represented by e) must be the prefault load current.

Now consider c). There is nothing to oppose current flow in the branch containing voltage source Vf. Since there was no current flowing in this circuit branch prior to the fault this current must be the fault current. The important point to note here is that the Thevenins equivalent impedance of the three circuit branches are being driven in parallel by Vf. Regardless of the angle of this voltage, as long as the impedance angles of each branch are the same, the phase angle of the fault current in each branch will be the same. This will essentially eliminate the generator angles and fault resistance from consideration.

Prefault load subtraction was applied to the fault waveforms shown in Fig 3-9 with the result shown in 3-10. Notice how the waveforms line up essentially restoring the entire 4ms communications error margin to the relay. When the RFL 9300 relay is configured for 3-terminal operation its control algorithms, for the most part, are based on transient fault currents obtained using prefault load subtraction.

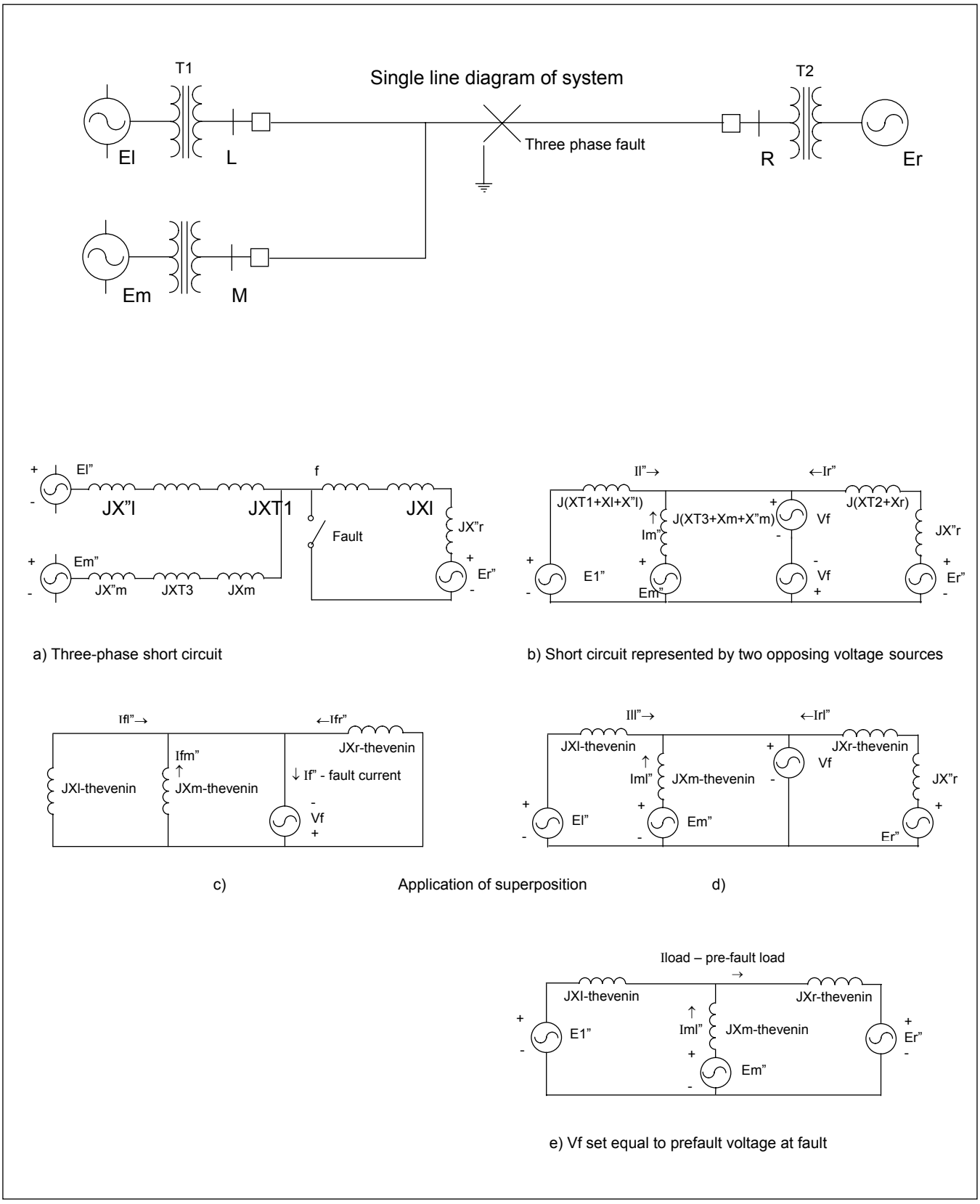


Figure 3-8. Prefault load subtraction eliminates generator angles

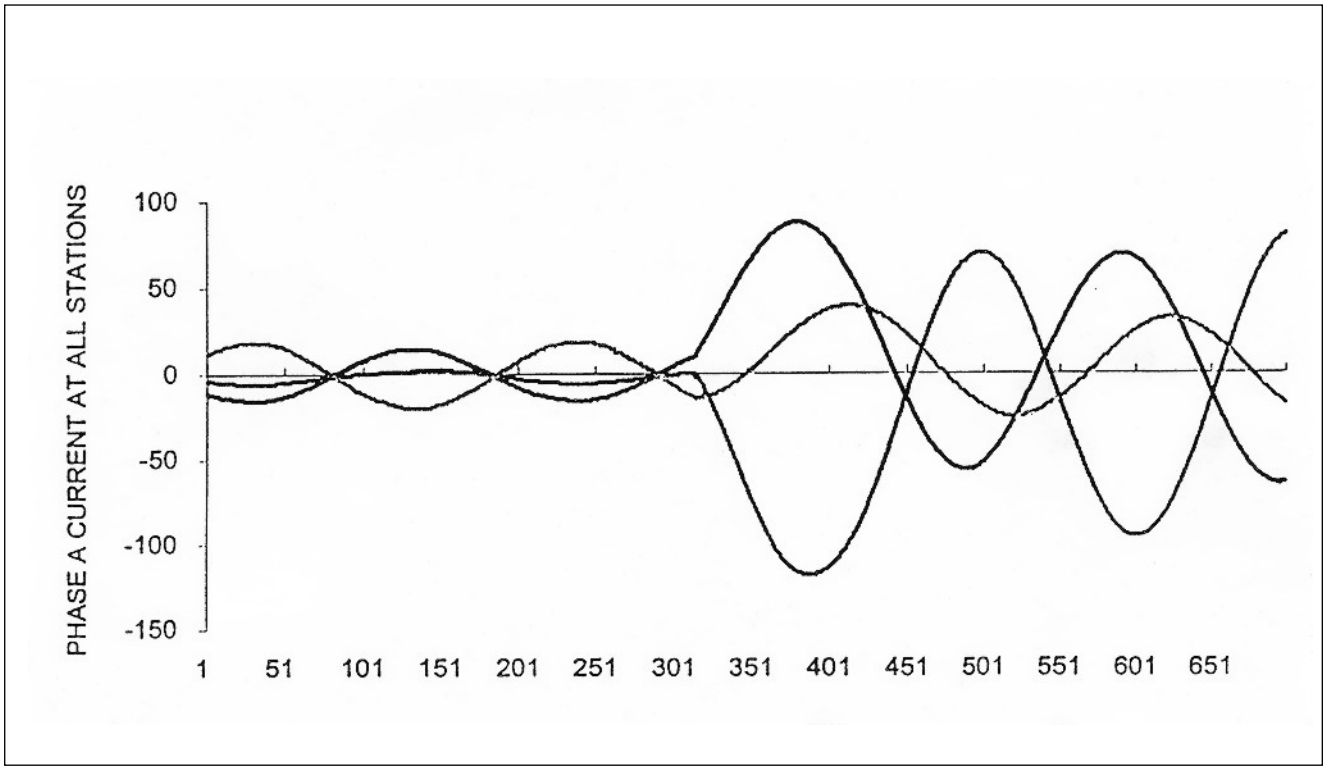


Figure 3-9. Currents before pre-fault subtraction

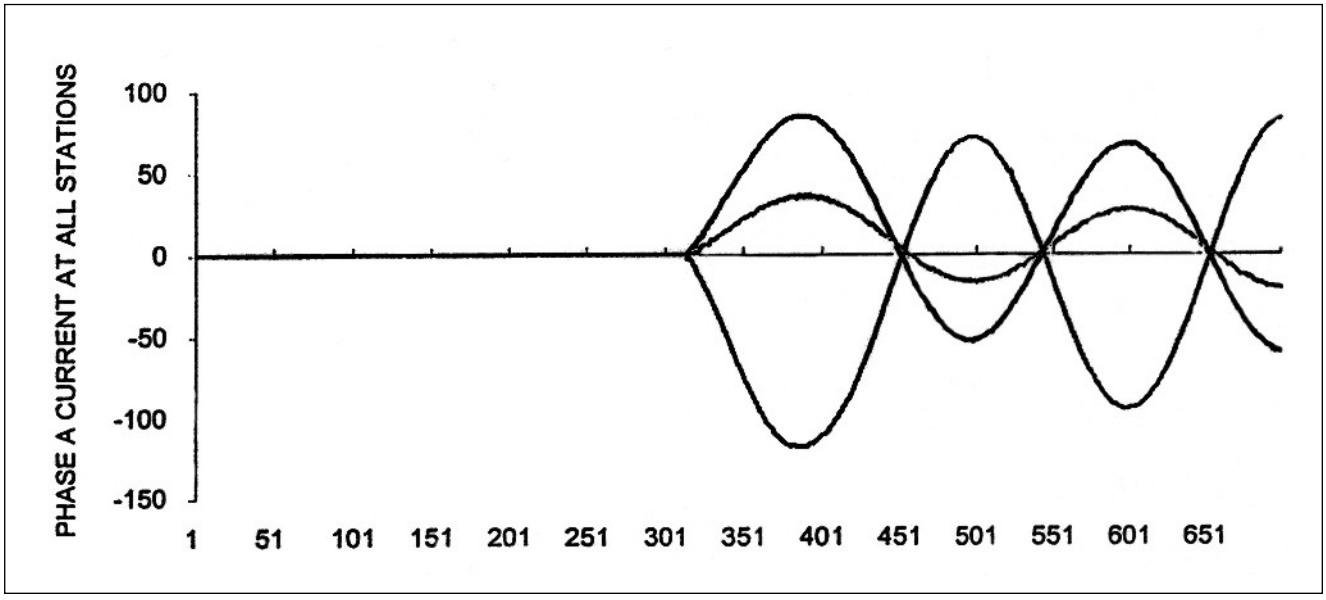


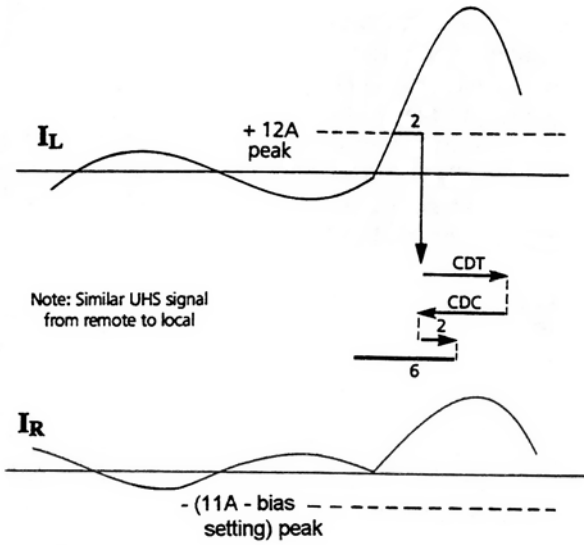
Figure 3-10. Currents after pre-fault subtraction

3.8 ULTRA HIGH-SPEED TRIPPING

The RFL 9300's UHS (Ultra High-Speed) circuit provides a trip decision in as little as 7 ms, when the RFL 9300 is using a 56-Kbps or fiber channel. (Actual breaker tripping takes about 4 ms longer; this allows for the auxiliary relay's pick-up time). The UHS circuit sends a high-priority message whenever a current greater than +12 A_{peak} is present for 2 milliseconds. Tripping occurs at the receiving terminal, unless the UHS is blocked by at least one current sample of -(11A - bias setting)$_{peak}$ or more. The minimum blocking current allowed is -7.5A peak for the phase A, B, or C controller or +7.5A peak for the 3I0 controller. The sample that blocks the UHS circuit must occur at some time during a 6-ms time window. This provides correct operation for internal and external faults, with incorrect channel compensations up to $\pm$3 ms. (See Figures 3-11 and 3-12.)

When the relay is configured for 3-terminal operation a UHS signal received from a remote terminal will not execute the UHS algorithm until it has been "verified" by a WCM, UHS or CCD message received from the second remote terminal. "Verified" means that the adjusted received time-tags of the two messages must be compared to insure that they represent the same time interval. The message from the second remote terminal may have a time-tag that precedes or follows the UHS message. Trip speeds comparable to those observed for 2-terminal systems are possible if the second terminal is sending a WCM or UHS message. If the second terminal is sending a CCD message the trip speed will tend to be similar to a SFT since the second terminal will not transmit the CCD message until a zero-crossing of the fault waveform is recorded.

Figures 3-11 & 3-12 represent UHS operation regardless of the system configuration. It must be understood that if the relay is configured for 3-terminal operation the waveforms represent transient fault current waveforms after pre-fault load subtraction.



2: 2ms dwell time at +12A peak. (Create UHS)

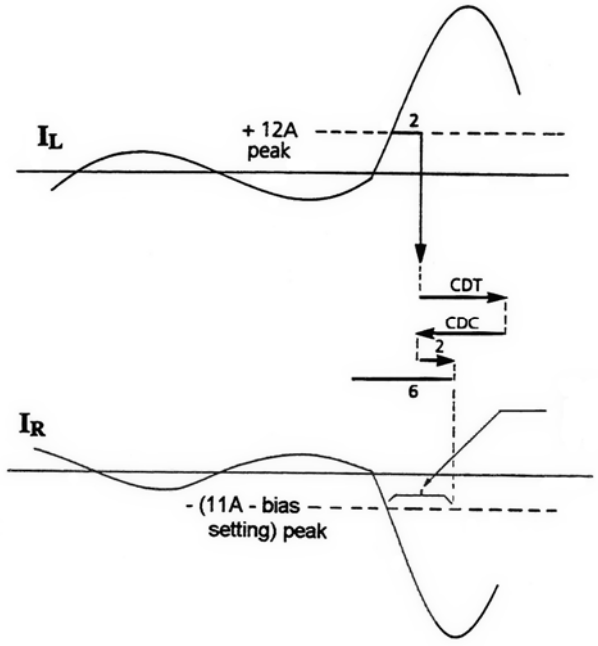
CDT: Channel Delay Time

CDC: Channel Delay Compensation

2: "Reach Forward Time" of 2 ms

6: Time window of 6 ms that looks for – (11A – bias setting) peak sample to block UHS.

Figure 3- 11. Operation of the RFL 9300's UHS circuit during an internal fault



Correct blocking during this time interval. (Only 1 sample equal to – (11A – bias setting) peak, or more negative, is required to block UHS tripping)

Figure 3-12. Operation of the RFL 9300's UHS circuit during and external fault

3.9 SATURATED MAIN CURRENT TRANSFORMERS

The main current transformers are particularly subject to saturation on close-in internal faults. A general rule of thumb is that the CTs used in relay applications will reproduce the primary current waveform with acceptable accuracy for at least a half-cycle or more. The UHS algorithm is designed to execute during this interval. This provides high-speed clearing for this condition.

3.9.1 INTERNAL FAULT CALCULATION

Two separate calculations should be made to select the proper CT's: one for "SLG" (single-line-to-ground) faults, and one for three-phase faults. Use the following formula for SLG faults:

$$V_{KPS} = I_{SLG} \times R_{2W} \times TF_G$$

where

V_{KPS} = Kneepoint voltage of the CT's B-H curve for worst-case SLG fault.

I_{SLG} = Maximum expected SLG fault current (symmetrical, in secondary amperes rms).

R_{2W} = "Two-way" secondary cable resistance, in ohms.

TF_G = "Transient factor" for ground faults. This is equal to $(1 + X_L/R)$ where (L/R) is the primary system time constant.

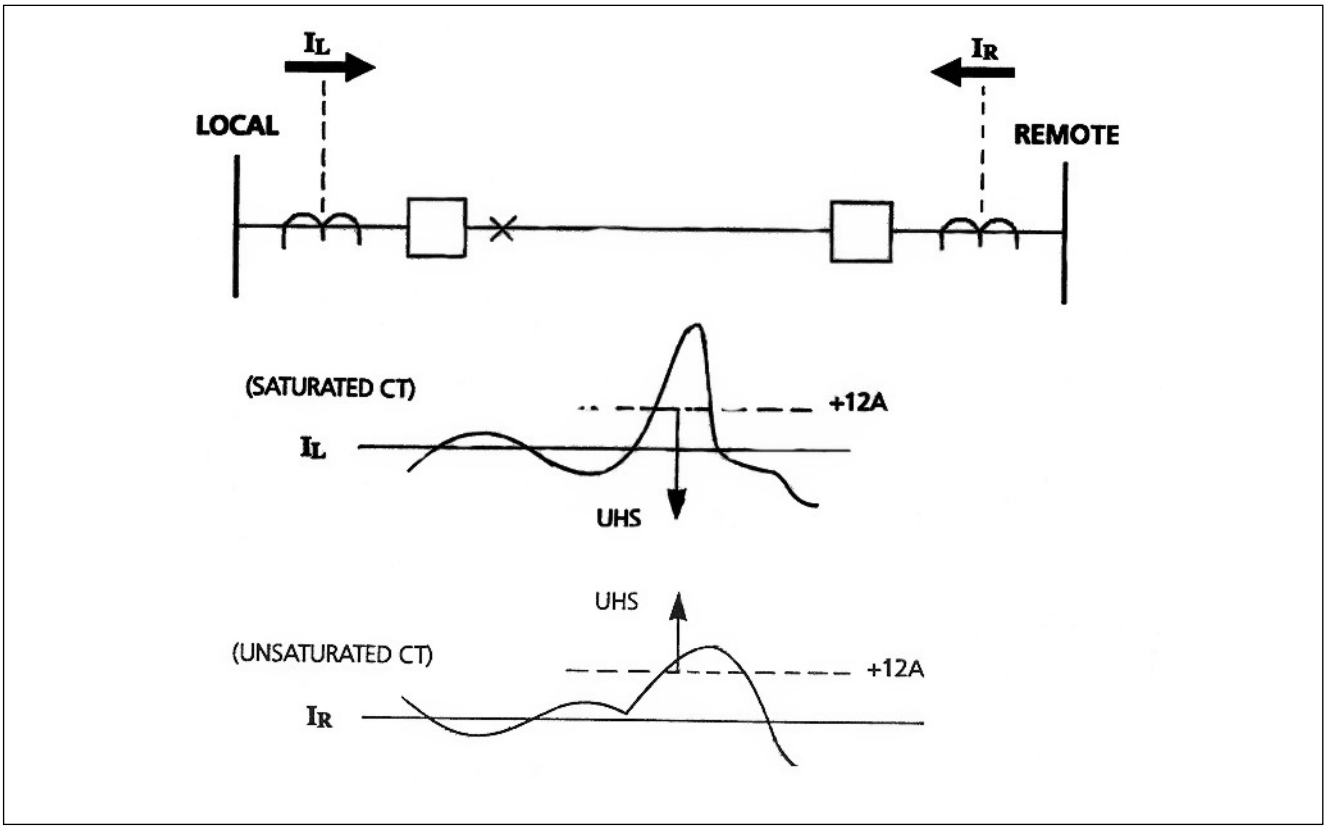


Figure 3-13. Saturated main current transformers during close-in internal fault

The CT's secondary winding resistance and the relay burden of most modern low-burden relays are much smaller than the secondary cable resistance. Because of this, these components can be ignored during the calculations.

For SLG fault calculations, the two-way (or round-trip) cable resistance must be used. This is because the CT for one phase must drive secondary current through the phase secondary cable resistance **and** the neutral secondary cable resistance.

For three-phase faults, the following formula is used:

$$V_{KPP} = I_{3PH} \times R_{1W} \times TF_P$$

where

V_{KPP} = Kneepoint voltage of the CT's B-H curve for worst-case three-phase fault.

I_{3PH} = Maximum expected three-phase fault current (symmetrical, in secondary amperes rms).

R_{1W} = "One-way" secondary cable resistance, in ohms.

TF_P = "Transient factor" for phase faults. This is equal to $(1+ X_L/R)$ where (L/R) is the primary system time constant.

For phase faults, the CT for the faulted phase drives current through its secondary cable resistance only. The voltage drop in the return cable (or cables) is driven by the other faulted phase CT (or CT's).

To select the proper CT class, take the higher of the calculated kneepoint voltages (Vkps or Vkpp), and divide it by ten since Vk must be modified if residual flux is taken into consideration. The next-higher CT class will be adequate for RFL 9300 operation on internal faults. This is because the RFL 9300's UHS circuit operated to provide fast tripping even though one or more CT's are very severely saturated.

Example:

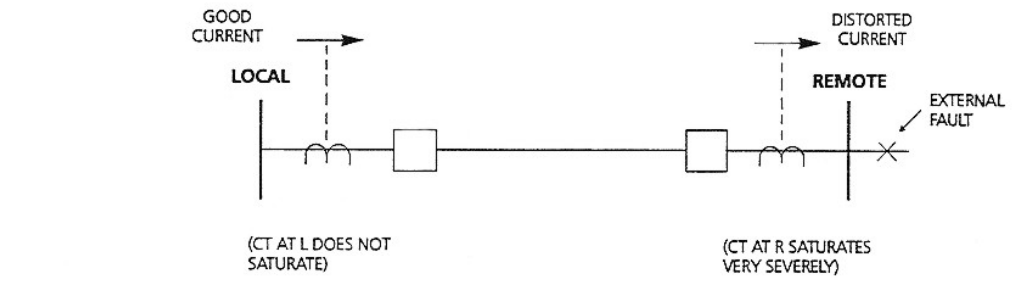
V_{KPS}	= 1700 volts
V_{KPP}	= 1550 volts
1700 / 10	= 170

CT's rated "C200" should be used.

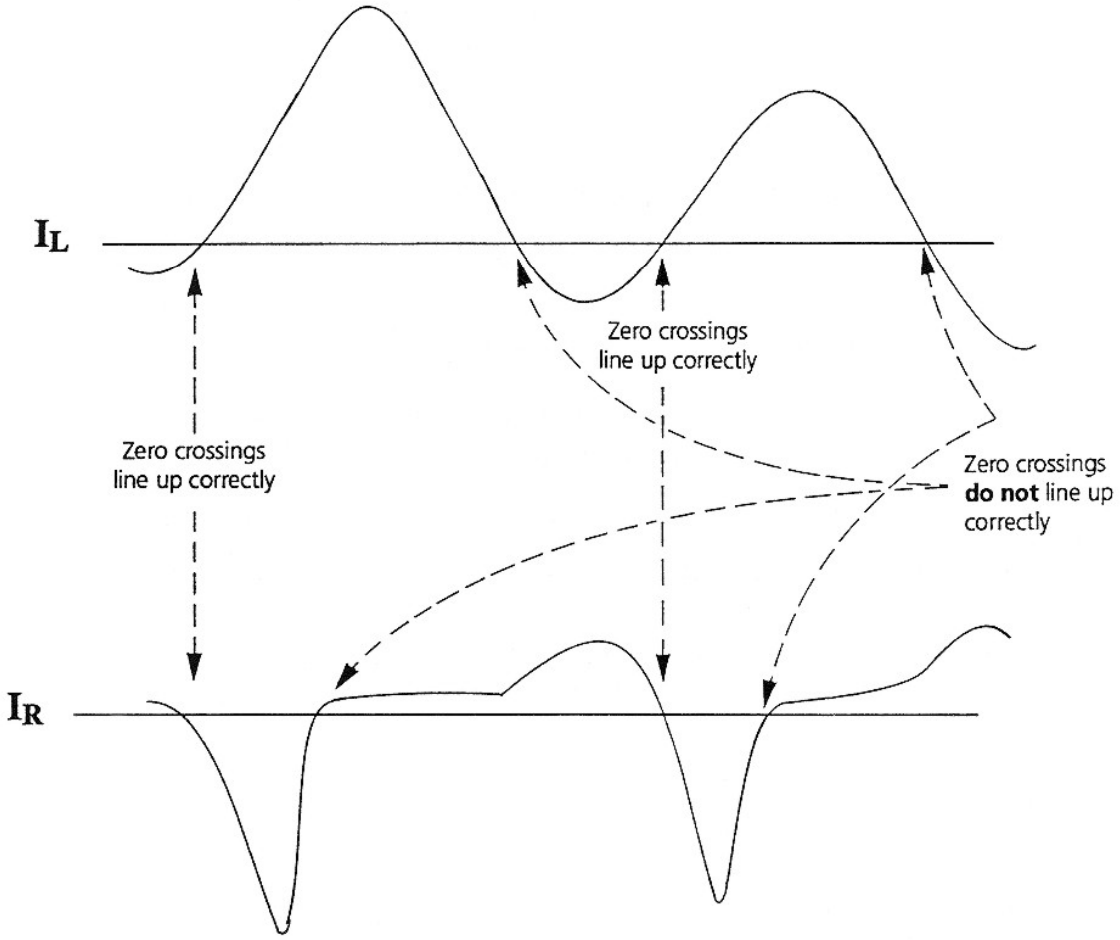
3.9.2 EXTERNAL FAULT CALCULATION

The RFL 9300 tolerates less CT saturation on external faults than it does on internal faults. The UHS circuit operates (blocks) correctly on the odd half-cycles (1st, 3rd, 5th, etc). However, the CCD (Charge Comparison Data) on all half-cycles may trip incorrectly. The UHS may trip incorrectly on an even half-cycle (2nd, 4th, 6th, etc) if the main CT is very severely saturated. (See Figure 3-9)

The large shifts in zero-crossings shown in Figure 3-9 only occur when there is a very large unbalance in CT performance. The RFL 9300 bias characteristic (see Figure 2-4) has been designed to provide additional security in the presence of moderate to large CT saturation. Also, because of the phase angle swings that are encountered in 3-terminal systems, extra security has been built into the 3-terminal bias characteristic (Figure 2-4b). Dynamic time-tag compensation adds additional bias equal to 1/4A rms X the difference between the adjusted received time-tag of a validated CCD value and the time-tag representing the center of the “nested” half-cycle stored at the local terminal. This is designed to be effective in the rare instance that a prefault load value is not acquired prior to a fault. The 1:8 slope to the characteristic is designed to combat the effects of CT saturation due to the higher scalar sums encountered in 3-terminal systems.



a. One-line diagram



b. Current waveforms

Figure 3-14. External fault with very severe CT saturation at one end

The calculations for external faults are similar to those for internal faults. First, the V_{KPS} value is determined for SLG faults:

$$V_{KPS} = I_{SLG} \times R_{2W} \times TF_G$$

where

V_{KPS} = Kneepoint voltage of the CT's B-H curve for worst-case SLG fault.

I_{SLG} = Maximum expected SLG fault current (symmetrical, in secondary amperes rms).

R_{2W} = "Two-way" secondary cable resistance, in ohms.

TF_G = "Transient factor" for ground faults. This is equal to $(1 + X_L/R)$ where (L/R) is the primary system time constant.

Then calculate V_{KPP} for three-phase faults:

$$V_{KPP} = I_{3PH} \times R_{1W} \times TF_P$$

where

V_{KPP} = Kneepoint voltage of the CT's B-H curve for worst-case three-phase fault.

I_{3PH} = Maximum expected three-phase fault current (symmetrical, in secondary amperes rms).

R_{1W} = "One-way" secondary cable resistance, in ohms.

TF_P = "Transient factor" for phase faults. This is equal to $(1 + X_L/R)$ where (L/R) is the primary system time constant.

For external faults, the currents used will be smaller than for internal faults, because the protected line's impedance helps to limit the current. The transient factors (TF_G and TF_P) also will be smaller, because line impedance usually has a smaller angle (about 75 degrees) than source impedance (as high as 85 degrees, or more).

To select the proper CT class for external faults, take the larger of the calculated kneepoint voltages (V_{KPS} or V_{KPP}), and divide it by four. The next-higher CT class will be adequate for RFL 9300 operation on external faults.

Example: V_{KPS} = 640 volts
V_{KPP} = 720 volts

720 / 4 = 180

CT's rated "C200" should be used.

3.10 WEAK INFEED APPLICATIONS

"Weak infeed" is an application concern for any transmission line protection scheme. This is particularly true of pilot wire schemes that will only trip when valid trip signals are received from both the local and remote stations. This is referred to as a "tripping" philosophy. Since the RFL 9300 uses a tripping philosophy for enhanced security, special provisions must be incorporated to assure proper operation in weak-feed applications.

Strong Feed

This is the normal mode of 9300 operation. In 2-terminal applications this requires 0.5 Arms and a half-cycle pulse width of 6 ms or more at each station. The only exception is that the phase controller will transmit a WCM when the local station breaker is open. This can result in a SFT at the receiving station if it meets the 0.5 Arms/6ms requirement and has a sensitive bias level setting. In 3-terminal applications a phase controller will transmit a WCM if the transient current does not meet the 0.5 Arms/6 ms requirement regardless of breaker status.

Weak Feed

This mode covers situations where one terminal does not meet the strong-feed requirements described above. The weak-feed circuit operates when it senses a local current of 1.5 A_{RMS} (or less) at the same time it receives a remote current of 1.5 A_{RMS} + bias setting or more. **These are absolute values, without regard to frequency or polarity.**

The difference between the RFL strong-feed and weak-feed trip algorithms is not as sharply defined as it once was now that the WCM is used instead of the ZCM. The WCM indicates that a weak current condition exists at the sending terminal. The message says nothing about breaker status. The ZCM signaled that an open breaker, based on a 52B signal, existed at the sending terminal. A CCD was transmitted, as it still is, when the control CT current ≥0.5Arms. This left a gap where no message was transmitted. Without a control signal being transmitted there was no possibility of a SFT at the remote terminal. As noted above this has changed. The main emphasis of the weak-feed algorithm is now to allow a faster trip at the weak-current terminal if fault detectors are active.

The weak-feed circuit takes care of some difficult applications, such as the one illustrated in Figure 3-15. In this application, the shunt reactors at the remote station interact with the distributed capacitance of the protected line, producing a small current with a poor waveform.

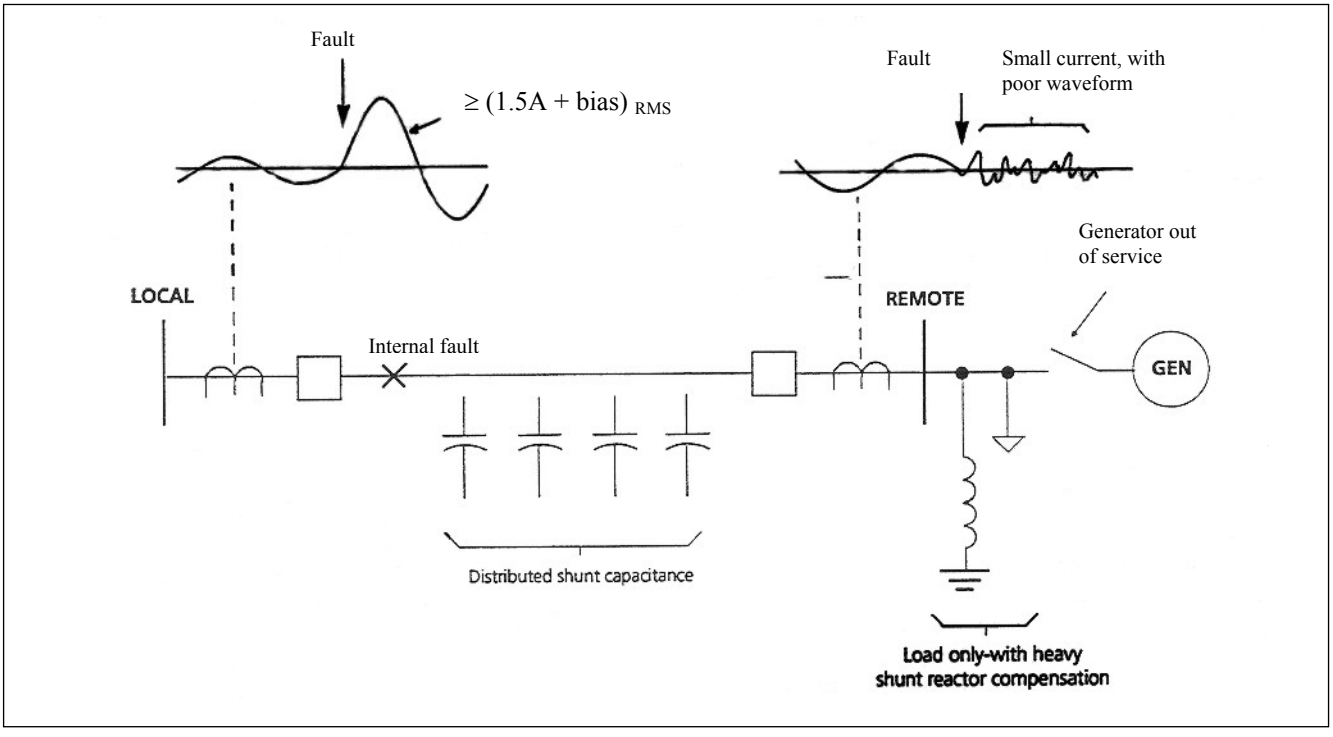


Figure 3-15. Weak infeed application

3.11 RECLOSE BLOCKING FOR THREE-PHASE FAULTS

Because the RFL 9300 is a per-phase (or "segregated phase") scheme, fault types are always correctly identified. This means that reclosing can be blocked for three-phase faults, if desired. (The output is always furnished; the user may choose to connect this output to the reclosing relay's block input.)

Protection schemes that are **not** per-phase will sometimes mistake DLG (double line-to-ground) faults for three-phase faults. This may occur when there is a very strong zero-sequence source at one end and the positive-sequence source is at the other end. (See Figure 3-16.)

The unusual current line-up in Figure 3-16 will fool a non-segregated phase scheme at the local station into thinking there is a three-phase fault. Also, these schemes probably will interpret the fault at the remote station as SLG, instead of DLG. The RFL 9300 will correctly recognize this condition as a BC-G fault at both stations.

In the DLG fault condition shown in Figure 3-16, the Phase B and Phase C current line-ups at the local and remote stations are 60 degrees out of phase. This still provides correct "nesting," but the margin for incorrect channel compensation is reduced from a nominal 90 degrees (about 4 ms) to only 30 degrees. However, this is not a problem for tripping; if the error in channel delay compensation hurts one of the faulted phases, it will actually help the other faulted phase. (This happens because the out-of-phase relationship between I_B at the local station and I_B at the remote station is opposite to that of I_C at the local station and I_C at the remote station). This is one of the advantages of per-phase charge comparison.

Also in Figure 3-16, there is no $3I_0$ current at the local station. Because of this, the $3I_0$ phase controller in the RFL 9300 at the local station will operate in its weak-feed mode during a DLG fault.

The RFL 9300 calculates a trip independently on each phase. If a long channel delay exists or high-speed breakers are used, the fault could be cleared before all three phases have calculated a trip. Because of this, reclose block on modem-equipped RFL 9300's is not recommended.

3.12 UNDERGROUND CABLES

The distributed wire-to-ground shunt capacitance of an underground cable is very high - usually 10 to 20 times that of overhead lines of equal length. This is because the phase wires in an underground cable are closer to earth ground. Also, the phase-to-phase capacitance of an underground cable is usually very high, depending upon cable construction. (The exception is where the phase cables are buried or laid separately. This is done in some submarine installations.)

Shunt capacitive currents are sometimes referred to as "line charging currents." These are "false differential" currents that can fool a current-based protection scheme into thinking there is a low-grade internal fault.

The RFL 9300 can be applied to underground cables by setting the phase bias and ground bias levels high enough to provide security in the presence of line charging currents (or the discharging currents present during a fault). The minimum bias setting is 1.0 amperes; this allows for up to 0.5 amperes of line charging current. If the cable's line charging current is higher than 0.5 amperes, a higher bias setting must be used.

A false differential can also be created by transient in-rush to a cable when the line is energized. The amount of in-rush is a function of source impedance and cable capacitance. The RFL 9300 can be made secure during the transient in-rush period by using its Bias Control feature. This raises the RFL 9300's bias level by an additional 1.5 amperes for a preset time (up to 1 second maximum, as selected by the user).

The RFL 9300 has a programmable parameter called "OVHD/UVG." This sets it for use with either overhead (OVHD) or underground (UVG) cables. When this parameter is set to UVG, the incremental bias is increased to 3.0 amperes.

Weak Feed Boost

When a phase controller is configured with Bias Control enabled and is set to protect for underground cables (UVG) a weak feed boost feature is automatically enabled. In this case a remote current greater than 3 Arms + bias setting is required to cause a weak feed trip signal to be returned to the remote station if the local station breaker is open. This prevents the weak feed trip function from tripping the remote station at a fault current lower than its Bias Control setting.

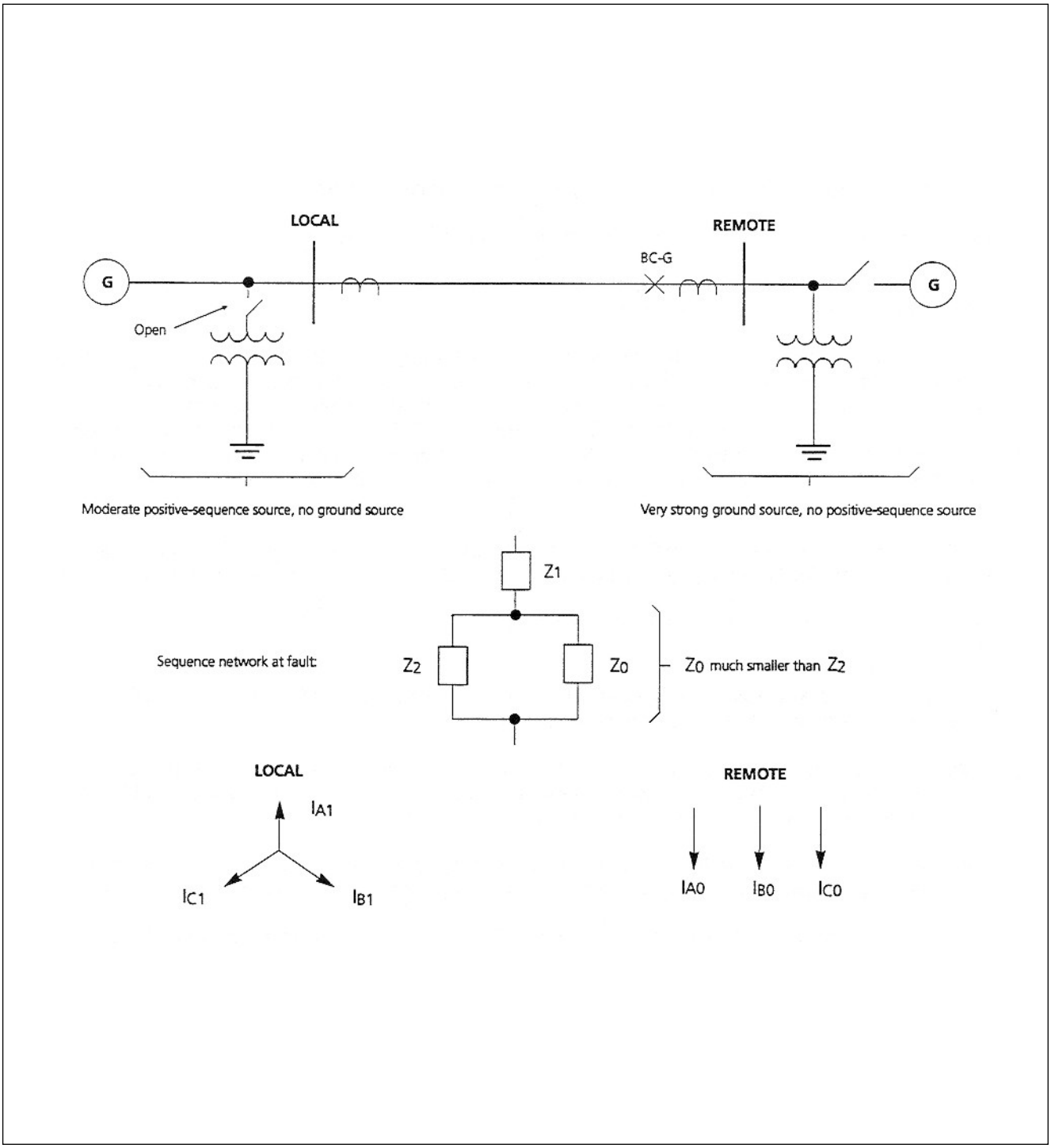


Figure 3-16. Double line-to-ground (DLG) fault
(May look like three-phase fault to protection schemes that are not per-phase.)

3.13 STUB-BUS PROTECTION

On double-breaker terminals (ring-bus or breaker-and-a-half), the stub-bus must be protected when the breakers are closed but the line disconnect is open. This condition may occur during line maintenance. There are several variations to this application as shown in Figure 3-17.

1. Remote terminal is single-breaker, no tapped load (2-terminal system).

2. Remote terminal is single-breaker, with tapped load (2-terminal system).

3. Remote terminal is double-breaker, with or without a tapped load (2-terminal system).

4. Remote terminals are single-breaker, no tapped load (3-terminal system).

5. Remote terminals are single-breaker, with tapped load (3-terminal system).

6. Remote terminals are double-breaker, or a combination of double breaker and single breaker, with or without a tapped load (3-terminal system).

If a stub-bus fault occurs, the two breakers at the local station will always have to be cleared. For the condition shown in Figure 3-17a, it doesn't matter if the remote breaker trips for a stub-bus fault at the local station. (Although this would result in increased breaker maintenance). However, the remote breaker(s) cannot be allowed to trip for the conditions shown in Figures 3-17b through 3-17f. For the conditions shown in Figures 3-17c and 3-17f, the ring (or 1 1/2 breaker bay) at the remote station(s) must be kept intact. This is true whether there is a tapped or untapped load at the remote station(s), and whether the disconnect at the remote station is open or closed.

To cover all the conditions shown in Figure 3-17, the breakers at the local station **must** be cleared, and the breakers at the remote station(s) **must not** be cleared. The RFL 9300 meets these requirements as follows:

1. When the disconnect switch is opened at the local station, the relay immediately enters stub-bus active mode.

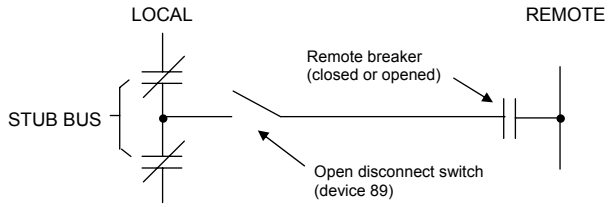
2. While in this mode all control messages received from the remote station(s) are processed by the supervisor but are not passed to the phase controllers.

3. Permissive trip is disabled at the local station and the phase controllers are forced to enter backup mode. While in this mode only the instantaneous overcurrent backup and inverse time-overcurrent backup functions are available for local stub-bus protection.

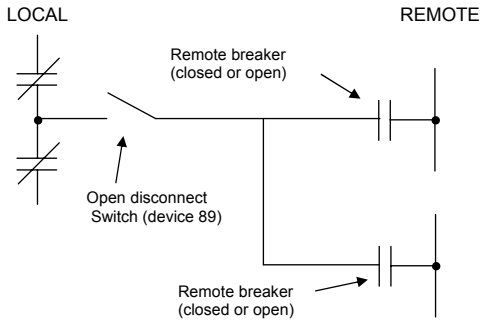
4. Since the transmission line to the local station has been opened, a steady stream of WCM messages is transmitted to the remote station(s). Transmission of all remaining control messages are blocked.

5. The remote station(s) continue to operate in normal fashion. They are not even aware that the local station is in stub-bus mode. The steady stream of WCM messages that they are receiving enables them to continue to provide differential protection.

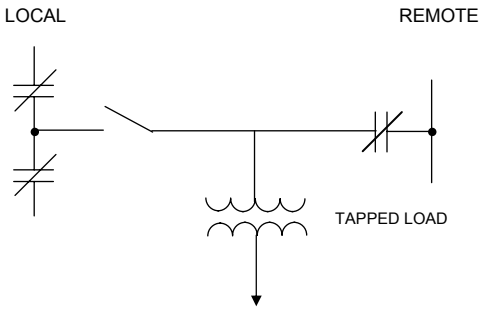
Note that when the 3IO controller operates in 2-terminal mode, it requires only a single active fault detector on its own card to trip if the remote station breaker is open. In the 2-terminal systems depicted in Figure 3-17, this will apply at the remote stations when the local station is in stub-bus mode.



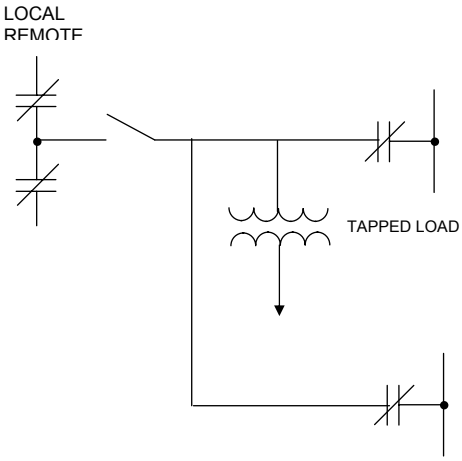
a. Remote terminal is single-breaker, no tapped load (2-terminal system)



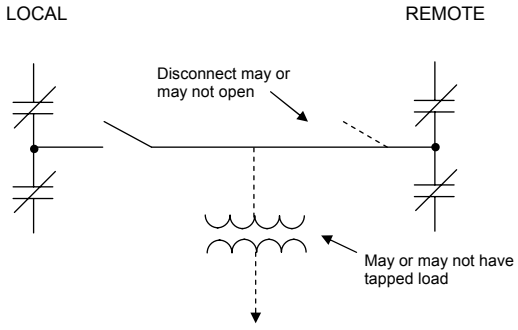
d. Remote terminals are single-breaker, no tapped load (3-terminal system)



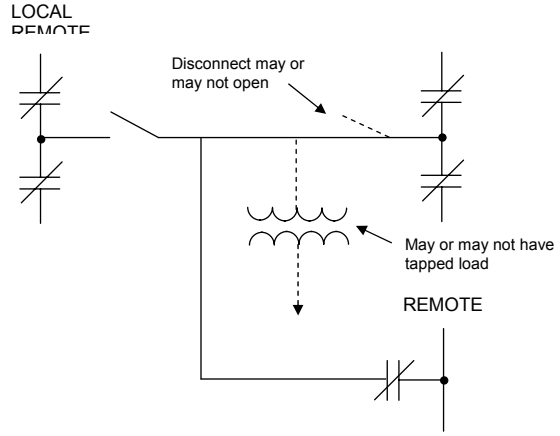
b. Remote terminal is single-breaker, with tapped load (2-terminal system)



e. Remote terminals are single-breaker, with tapped load (3-terminal system)



c. Remote terminal is double-breaker, with or without tapped load (2-terminal system)



f. Remote terminals are double-breaker, or a combination of double breaker and single breaker, with or without a tapped load (3-terminal system)

Figure 3-17. Sub-bus protection

3.14 TAPPED LOAD

Tapped load applications are a concern for all line protection schemes. Sometimes it is easier to apply distance relays to a tapped line, because the forward-looking relays can sometimes be set "into the bank" without affecting line coverage. In other cases, the application of current differential (or charge comparison) relays is easier. This is particularly true when the tap is near one terminal on a medium-length or long line. The response of the current differential system is based on **total** fault current. In contrast, the distance relays respond to local information only and the distance relays must create a correct trip/no-trip decision at both terminals in permissive schemes.

A typical tapped-line application is shown in Figure 3-18. Applications such as this present three problems to the RFL 9300:

1. The load current looks like a low-grade internal fault.

2. Low-side faults look like medium-grade internal faults.

3. Transformer in-rush looks like a low-grade internal fault, particularly when the transformer is energized by closing a high-side disconnect switch at the tap. If the transformer is energized by closing a circuit breaker, the bias control function provides security. (See Figure 3-19.)

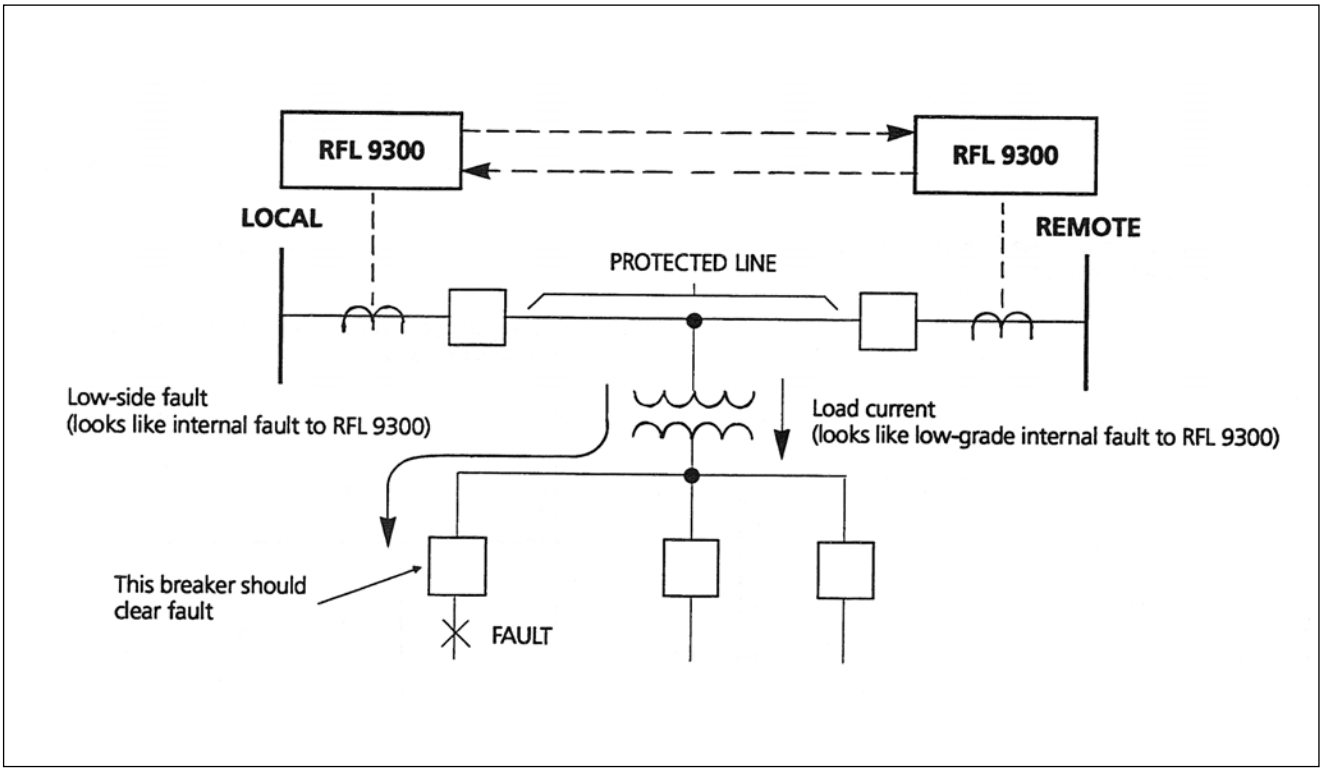


Figure 3-18. Typical tapped line application

The problem of handling low-side faults is much more severe than that of load current, because transformer impedance is typically 6 to 10percent. This means that low-side phase faults are at least ten times the magnitude of the rated current. The RFL 9300 can be applied to tapped lines by raising the bias level so that the RFL 9300 will not respond to low-side faults. At the same time, the RFL 9300 will still see all internal faults on the protected line.

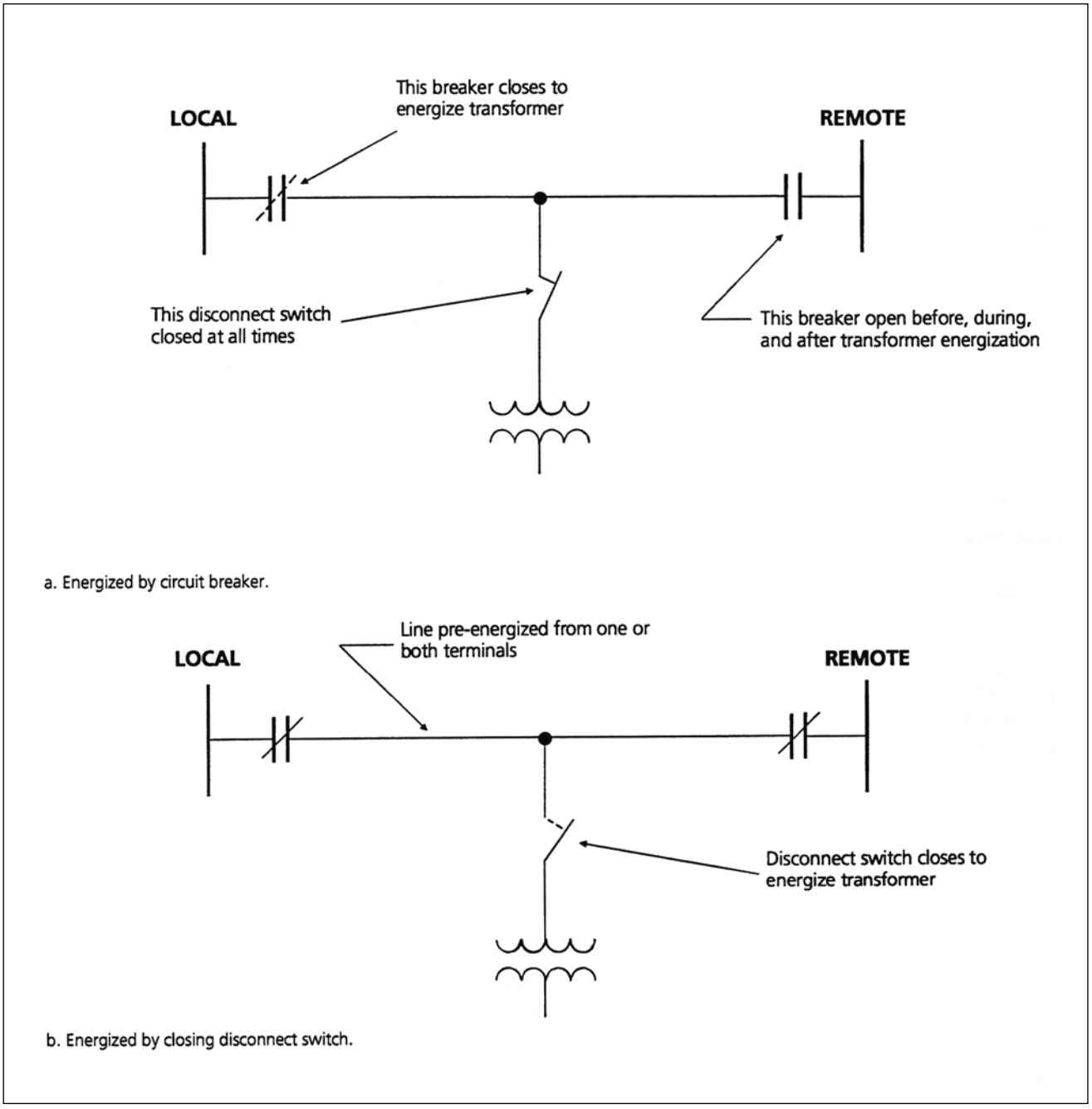


Figure 3-19. Transformer in-rush

In general, this makes the RFL 9300 suitable for all tapped lines, except for those applications where the transformer allows significant zero-sequence current to flow from the high-side to feed low-side faults. An example of this is the wye-wye transformer configuration shown in Figure 3-20, where both sides are solidly grounded. The RFL 9300 would not work well in this application because its $3I_0$ bias level would have to be raised to prevent the RFL 9300 from false-tripping on low-side SLG (single line-to-ground) faults. This prevents the RFL 9300 from detecting low-current SLG faults on the protected line, such as the ones caused by high resistance ground faults. Fortunately, the condition shown in Figure 3-20 appears to be quite rare. Most tapped transformer applications appear to be delta high-side and grounded-wye low-side.

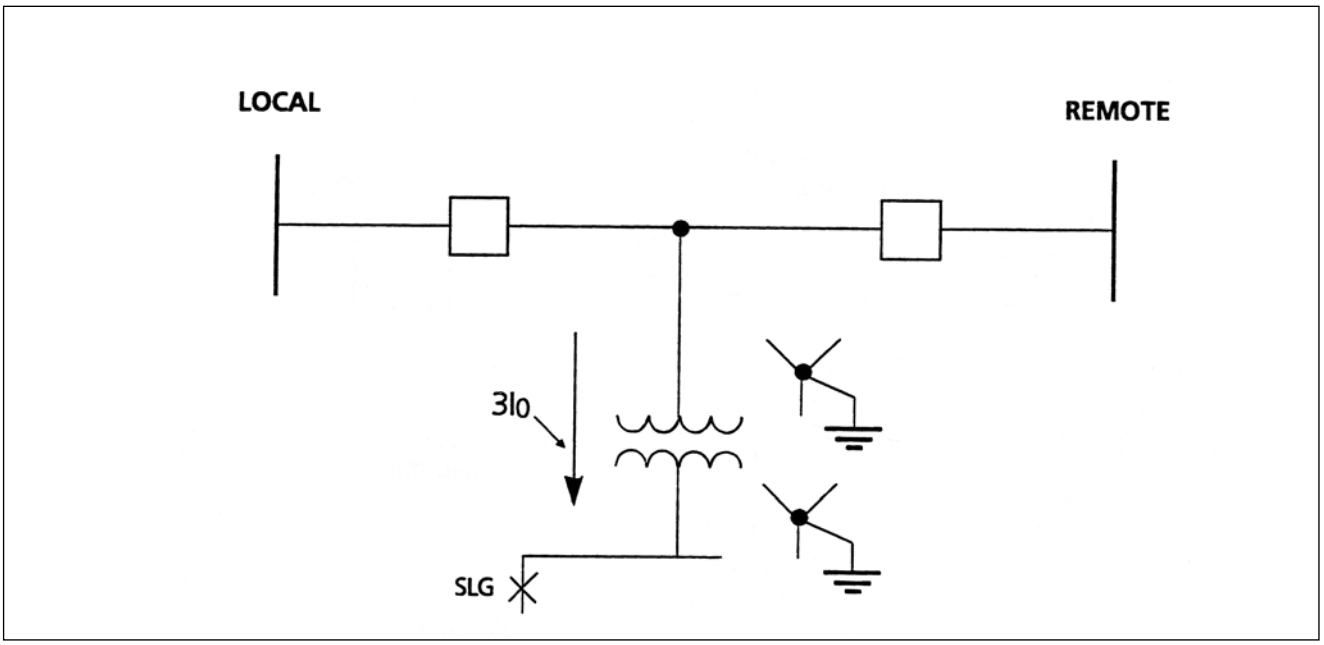


Figure 3-20. Zero-sequence current flows through transformer

3.14.1 CALCULATIONS FOR LOW-SIDE FAULTS

Figure 3-21 shows a typical tapped line application. Assume that the high-side three-phase fault current under minimum system conditions is 15,000 amperes primary (which is equal to 31.25 amperes secondary). To conduct a worst-case analysis of this application, a maximum system will be considered (all generators and all lines in service). The equivalent system impedance will be ignored, so the high-voltage bus at the tap will be treated as an "infinite" source. It is also assumed that all the limiting impedance for the low-side fault is due to the transformer impedance. This will introduce a safety factor of about 10-percent into the calculations.

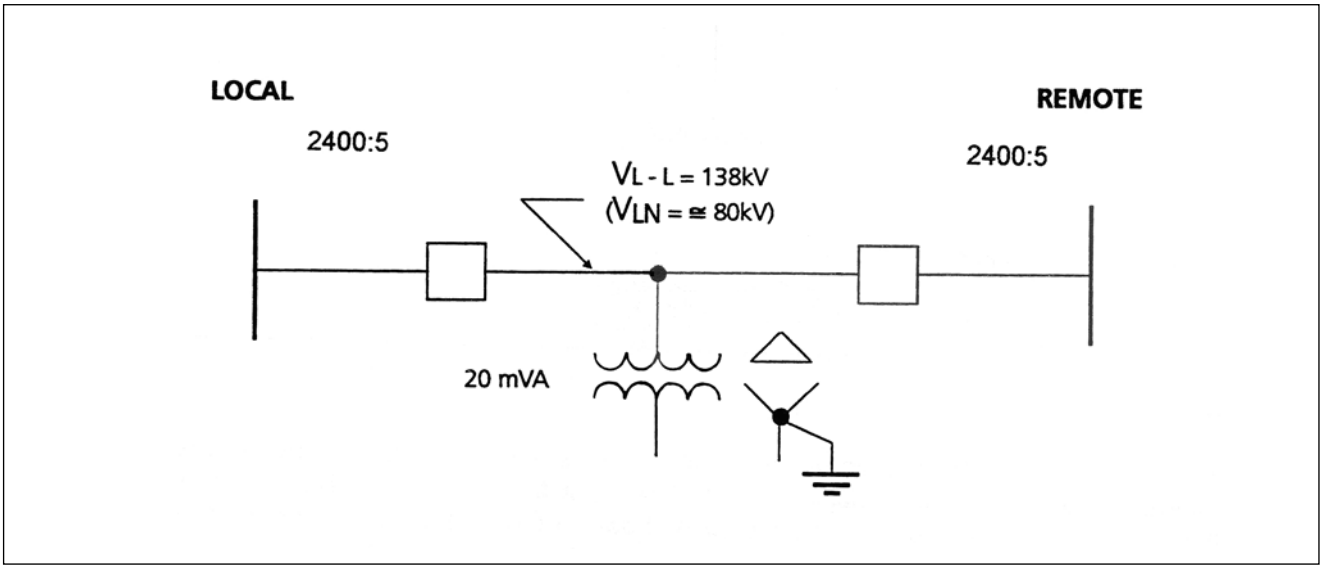


Figure 3-21. Typical tapped line application

The best method of calculating a low-side, three-phase fault (worst-case) is to first calculate the rated load current. This is based on the MVA rating of the transformer:

$$MVA = 3 \times I_L \times V_{LN}$$

For the system shown in Figure 3-21, the calculation would be as follows:

$$20 \times 10^6 = 3 \times I_L \times 80{,}000$$

$$\therefore \quad I_L = 20{,}000 / 240 = 83.3 \text{ amperes}$$
(0.175 secondary amperes)

Since the impedance of a 138-kV transformer is usually 10 to 15 percent, the worst-case value (10 percent) is assumed for the calculations. The following formula is used to calculate the three-phase fault current (I_F):

$$I_F = 1 / 10 \text{ percent} \times I_L$$

$$= 10 \times I_L$$

$$= 10 \times 83.3 \text{ amperes}$$

= 833 amperes
(1.75 secondary amperes)

Although this is a high "false differential" current, it is only about one-eighteenth the magnitude of the high-side fault current (31.25 secondary amperes). Since there is an 18:1 ratio between the minimum internal phase current and the maximum external fault phase current, there is plenty of room to apply the RFL 9300. To do this, the correct phase bias level must be set.

The ground bias level may be set at minimum (1.0 secondary amperes), since $3I_0$ will not flow through the delta-wye transformer to feed low-side ground faults. The maximum phase bias setting available in the RFL 9300 is 8 amperes. Low-side phase faults cause a maximum "false differential" of 1.75 amperes, as calculated above. The phase bias should be set to a value equal to at least three times the maximum let-through current; this will take care of transient over-reach due to dc offset. With the phase bias set at 6 amperes, the RFL 9300 can tolerate a let-through current of 2 amperes, so a setting of 6A phase bias is appropriate for this application.

The final step is to verify that a 6-ampere phase bias setting will allow the RFL 9300 to sense all internal phase faults. At a 2400:5 ratio, the minimum high-side fault current for a three-phase fault was calculated to be 31.25 secondary amperes. For a phase-phase fault, this figure would be

$$\sqrt{3} / 2 \times 31.25 \text{ A} = 27.05 \text{ secondary amperes}$$

Since this value is well above the phase bias setting of 6 amperes, it does not compromise RFL 9300 sensitivity.

3.14.2 TRANSFORMER IN-RUSH

The worst-case in-rush is caused by closure of the high-side disconnect switch at the tap. (See Figure 3-19b.) This is worst-case because the RFL 9300's at both ends of the protected line have no knowledge of the disconnect switch closure, and cannot introduce temporary desensitizing of the bias level (called "bias control").

Extensive simulator testing has shown that transformer in-rush is not as severe as a low-side fault. Therefore, 9300 settings that are secure for low-side faults will also be secure for transformer in-rush

3.14.3 CONCLUSION

If the tap transformer blocks the flow of zero-sequence, and the minimum internal phase fault current is at least three times the magnitude of the maximum external phase fault current, the RFL 9300 may be applied. This requires elevated phase bias settings, and possible resistor changes in the RFL 9300's ACT (auxiliary current transformer) circuits.

3.15 OPEN CONDUCTOR WITH SINGLE LINE-TO-GROUND FAULT

Most open-conductor (OC) conditions also involve SLG faults at both sides of the open. (See Figure 3-22.) This is called an "OC/2-SLG" fault (open conductor with two single-line-to-ground). The SLG faults are usually high resistance, since the broken conductor may touch only dry or frozen earth, or dry pavement. However, this condition is **easier** to relay than a high-resistance SLG fault without a broken conductor. This is because the through-load current that tends to mask the internal fault current on some relay schemes is interrupted by the broken conductor.

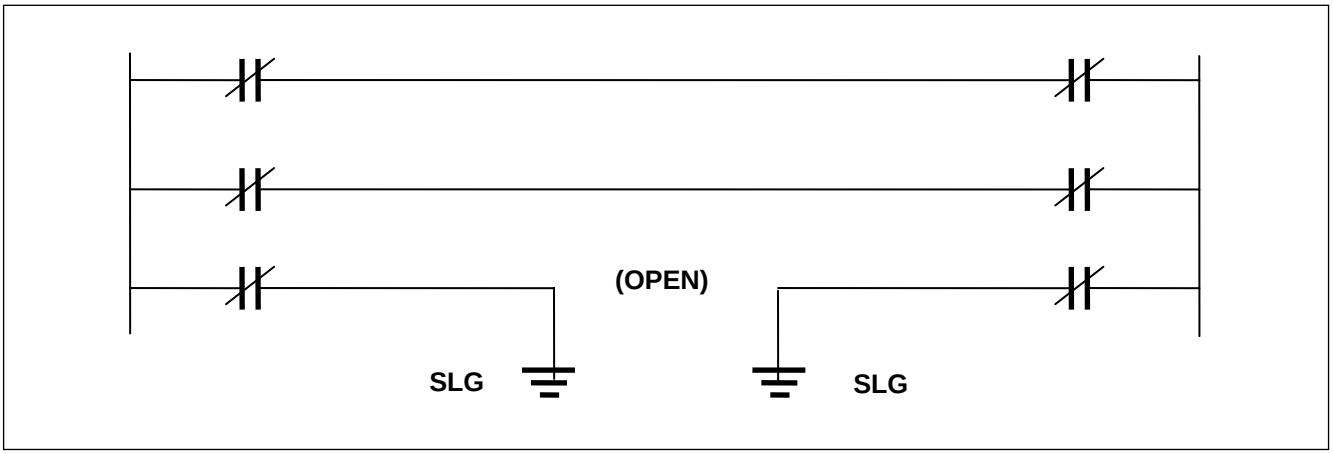


Figure 3-22. Open conductor with two single-line-to-ground faults (OC/2-SLG)

Because of its "rainbow" characteristic, the RFL 9300 is not affected by the through-load component. It can handle OC/2-SLG and high-resistance SLG faults equally well.

If the open conductor occurs near a tower, it is possible to have an open conductor with an SLG fault on only one side of the open conductor. (See Figure 3-23.) This is called an "OC/SLG" fault (open conductor with one single-line-to-ground). This is a common occurrence if the line opens at the supporting insulator.

The RFL 9300 has three modes it can use to clear an OC/SLG condition: phase weak-feed, ground weak-feed, and ground strong-feed. Phase weak-feed and ground weak-feed are not very sensitive, since they require a minumum of 2.5 amperes at the remote terminal. This is equivalent to a fault current caused by about 130 ohms of fault resistance @ 138 kV, using 1200:5 CT's. Ground strong-feed normally provides much more sensitive protection.

3.15.1 PHASE WEAK-FEED

In phase weak-feed, the faulted phase current at the open conductor side (the local terminal in Figure 3-23) is zero or very small, if there is no tapped load. This current will be caused by the capacitive charging current of the portion of the line to the left of the open. This is less than 0.5 amperes for all overhead lines less than 100 miles long (160 km).

The faulted phase current at the right terminal is equal to the total fault current. If this current is above 1.5amperes plus phase bias, a weak-feed trip is established at the local terminal. (This happens because the local current is less than 1.5 amperes and it receives 1.5 amperes plus phase bias or more from the remote terminal.) As a result, high-speed tripping will occur at both terminals.

3.15.2 GROUND WEAK-FEED

If there is a small load current flowing during the OC/SLG condition (less than 1.5 amperes), the $3I_0$ current at the local terminal will be less than 1.5 amperes. The ground phase controller also will trip on weak-feed, assuming the total $3I_0$ current at the remote terminal is 1.5 amperes plus phase bias or more.

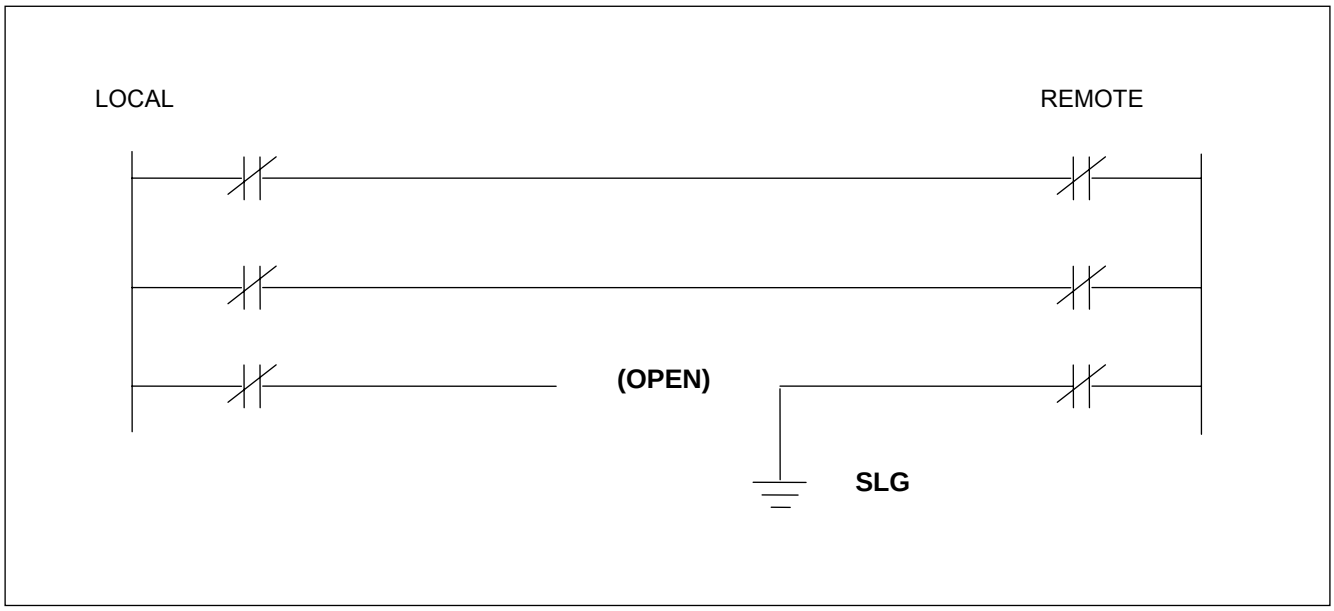


Figure 3-23. Open conductor with one single-line-to-ground fault (OC/SLG)

3.15.3 GROUND STRONG-FEED

If the load current is 0.5 ampere or more, ground strong-feed will usually operate and provide sensitive protection for the OC/SLG condition. This is equivalent to a fault current caused by about 220 ohms of fault resistance @ 138 kV, using 1200:5 CT's.

A phasor analysis of ground strong-feed operation is shown in Figures 3-24 and 3-25. From this analysis, several observations can be made about ground strong-feed operation:

1. The $3I_0$ component due to the high-resistance SLG fault is **in-phase** or **180 degrees out-of-phase** with the $3I_0$ due to the open conductor. This is because both are "watt-flow" (resistive) currents. The open conductor effect relates to load current (resistive) on the affected phase. The SLG effect relates to the resistive effect of the ground fault resistance.

2. The $3I_0$ magnitude due to the high-resistance SLG fault is a direct function of the ground fault resistance (R_G).

3. If the SLG is on the load **sending end** side of the open conductor (Fig. 3-24), the $3I_0$ currents due to the open conductor and the SLG are **subtractive**. This creates a region of net $3I_0$ on the SLG side that may be below 0.5 amperes. This prevents ground strong-feed operation for certain R_G values.

4. If the SLG is on the load **receiving end** side of the open conductor (Fig. 3-25), the $3I_0$ currents due to the open conductor and the SLG are **additive**. This assures ground strong-feed tripping for all R_G values of 220 ohms or less @ 138 kV, using 1200:5 CT's.

The OC/2-SLG and OC/SLG conditions will both be correctly detected by the RFL 9300. The RFL 9300's degree of sensitivity depends upon the value of the ground fault resistance (R_G), load current, and which side of the open is shorted to ground.

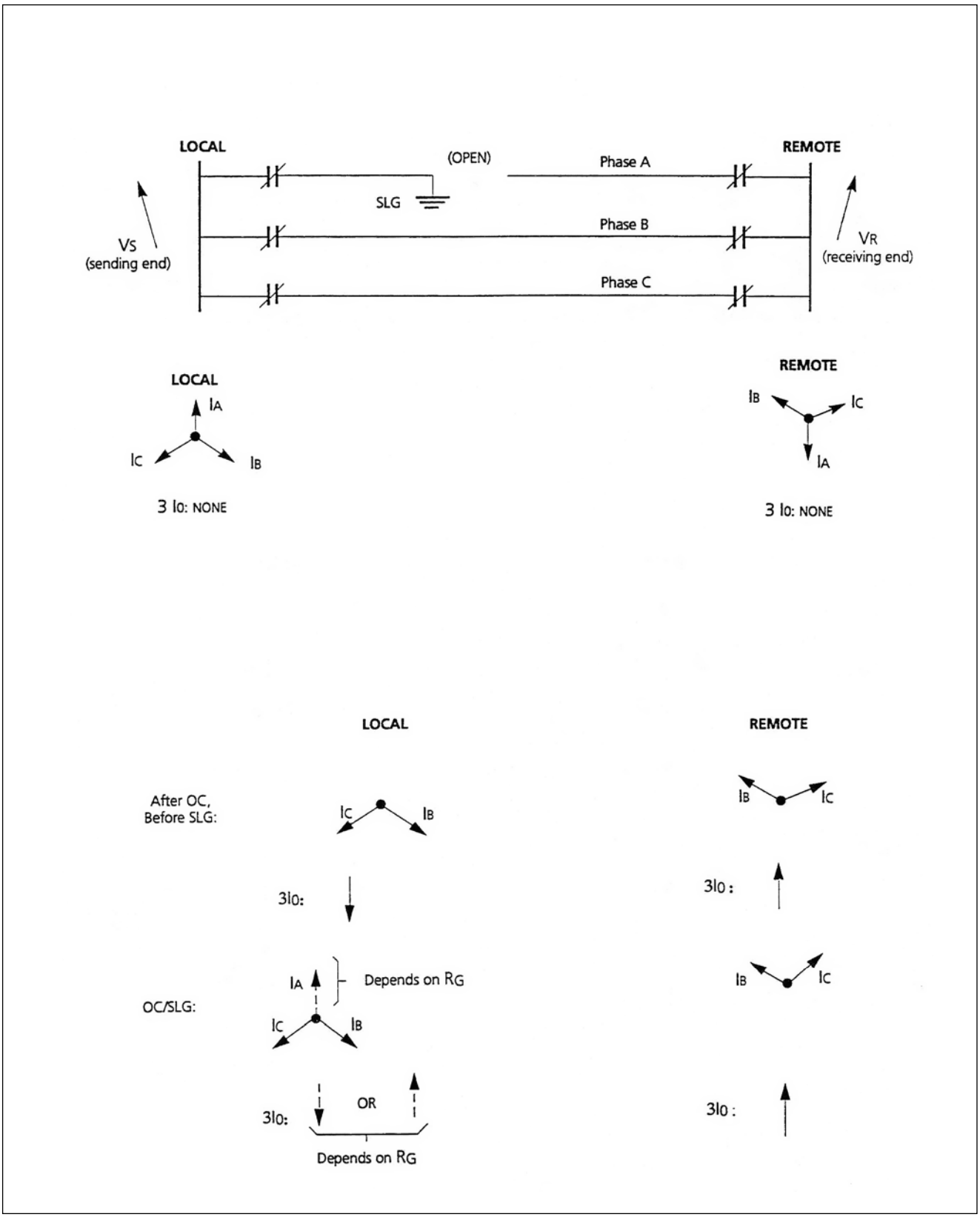


Figure 3-24. Phasor analysis of ground strong-feed operation, based on a load current of 0.5 amperes or more, with the SLG fault occurring on the load sending end side of the open conductor

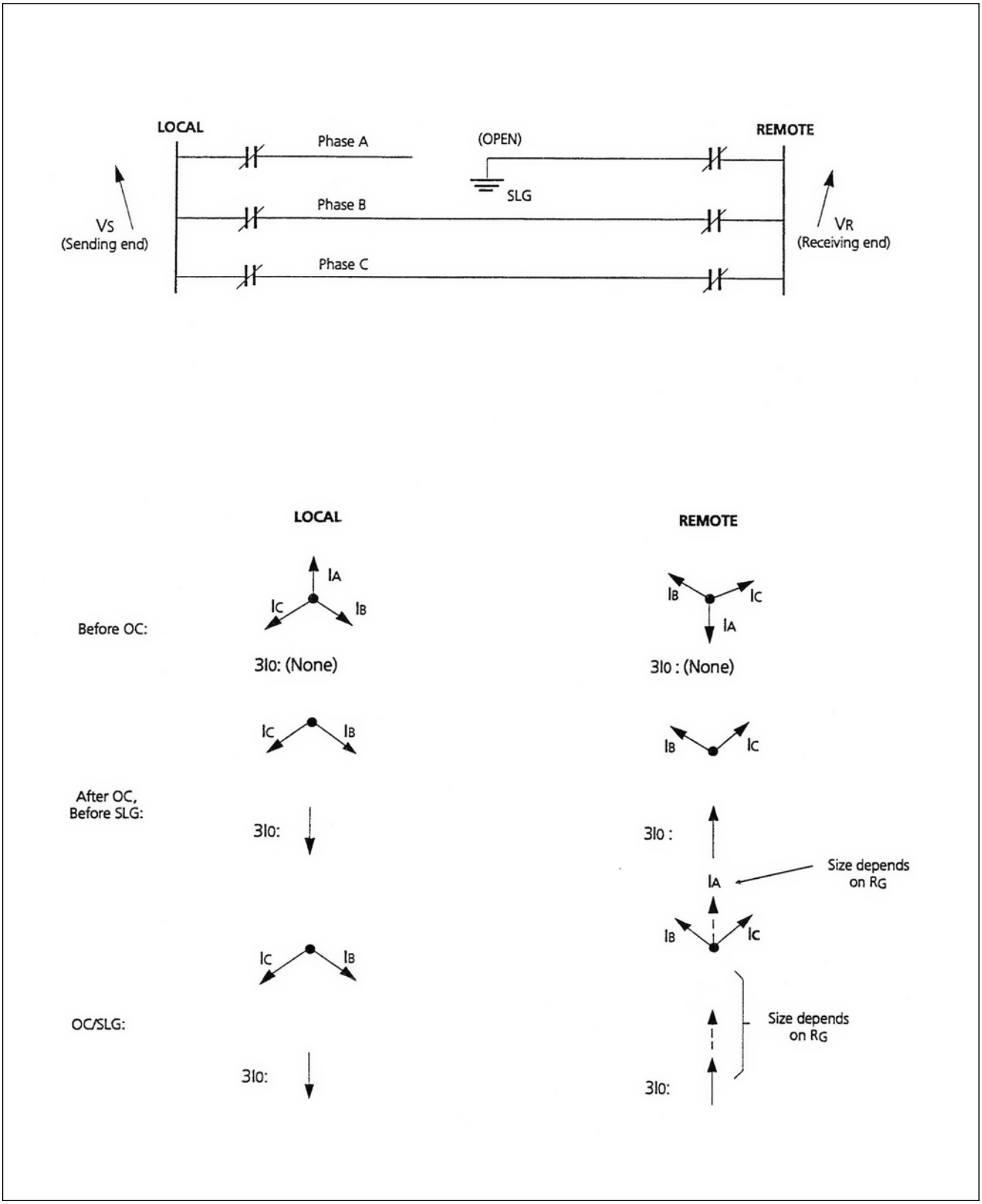


Figure 3-25. Phasor analysis of ground strong-feed operation, based on a load current of 0.5 amperes or more, with the SLG fault occurring on the load receiving end side of the open conductor

3.16 OPEN CONDUCTOR WITHOUT SINGLE LINE-TO-GROUND FAULT

Occasionally, an open conductor may occur that does not involve any ground fault at all. For example, this could happen at a direction-changing tower, where the break occurs in the short conductor between strain insulators. This would produce the condition shown in Figure 3-26.

If there is no load flow between the local and remote terminals before the conductor opens, there is no way to detect an open circuit. This is because basic electric circuit theory states that a wire that is not carrying current may be replaced by an open circuit. But if the transmission line is carrying load current before the conductor opens, the open circuit will create the phasors shown in Figure 3-26. Since the phasors do not violate Kirchhoff's Laws or the Principle of Conservation of Charge, the RFL 9300 does not create a trip signal.

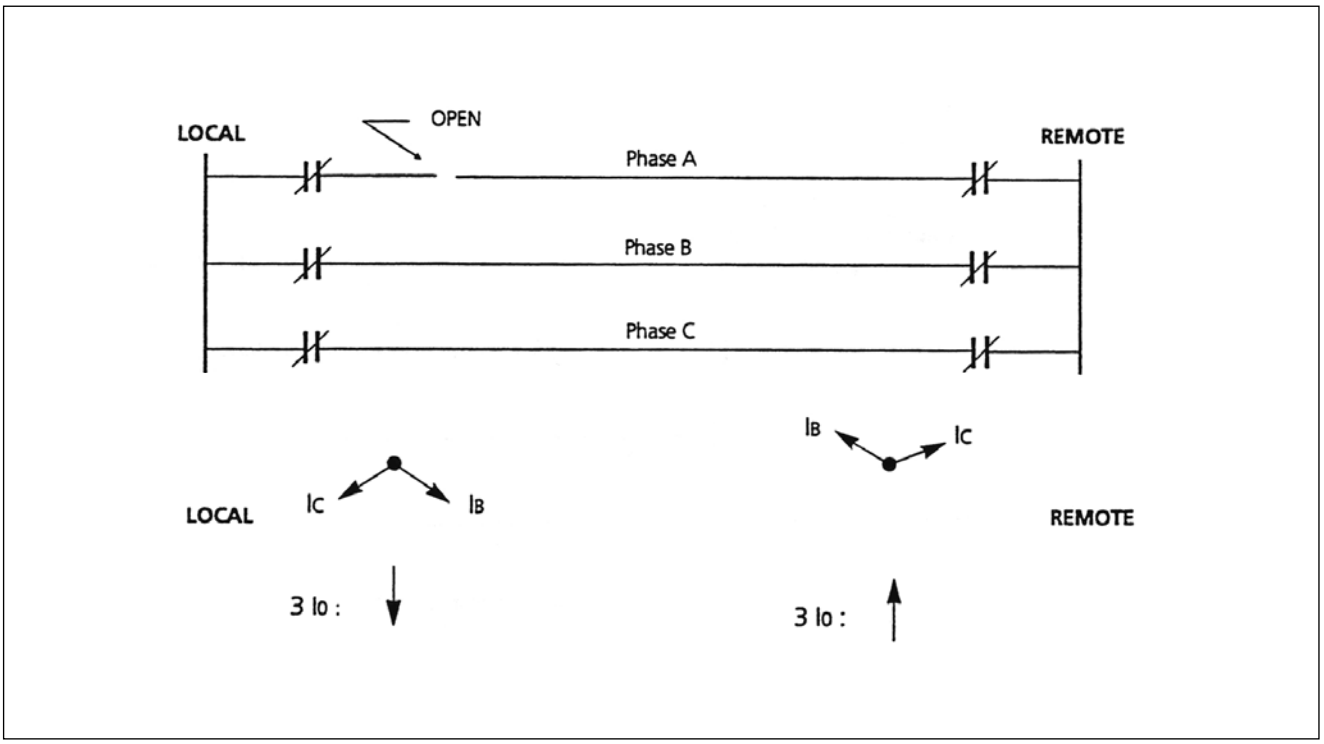


Figure 3-26. Open conductor without single-line-to-ground fault

On the other hand, the condition in Figure 3-26 does look like an internal BC-G fault where the remote breaker has tripped. In other words, it looks like a loss-of-load condition. The loss-of-load circuit can detect the open conductor condition. To provide security, the loss-of-load circuit requires a "Zone 2" timer before tripping or alarming takes place. The timer is usually set to about 150 ms, and the choice between tripping or alarming is made by the user. The Zone 2 timer prevents other conditions that can masquerade as an open-conductor from creating a false trip signal.

It has been suggested that $3I_0$ operation plus a Zone 2 timer would be a simple way to detect an open conductor. This would result in a problem coordinating the $3I_0$ and the timer with all external ground faults that may not be cleared before the Zone 2 timer times out. On the other hand, loss-of-load plus a Zone 2 timer is not operated by external ground faults. The only possible miscoordination occurs for an open-conductor condition on an adjacent line where the following conditions are present:

1. There are no other lines connected at the remote bus.

2. There is no SLG fault on either side of the open conductor on the adjacent line. (If there is an SLG fault, it is assumed that the adjacent line will be cleared before the Zone 2 timer times out.)

The conditions that can result in miscoordination of loss-of-load plus the Zone 2 timer are illustrated in Figure 3-27. If this condition is a concern, loss-of-load plus Zone 2 timer should be used to alarm, not to trip.

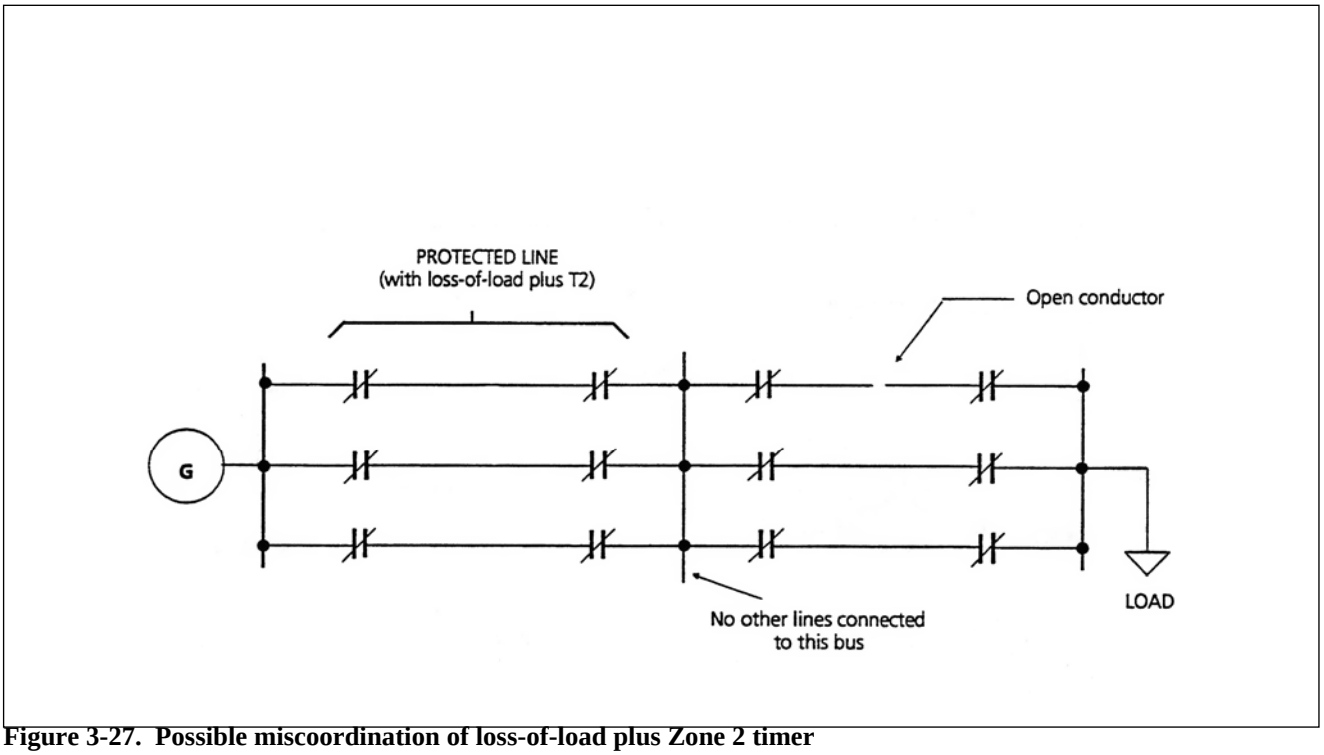


Figure 3-27. Possible miscoordination of loss-of-load plus Zone 2 timer

SECTION 4: SETTING GUIDELINES

4.1 INTRODUCTION

This section provides guidelines to help the user determine the parameter settings required to adapt the RFL 9300 to a specific application. For background and basic concepts, the user should first read sections 2 and 3 of this manual. Instructions for entering settings can be found in Section 6 of this manual.

The RFL 9300 has over a hundred parameters that it uses during operation. A complete list of these parameters can be seen in Tables 6-5 and 6-6. Some of the parameters are programmable, and others are read only. Tables 4-1 and 4-2 list all RFL 9300 parameters that are programmable. Space is provided in these tables for you to record the settings you will need to make for your system.

4.2 PROGRAMMABLE PARAMETERS

4.2.1 PH BIAS - PHASE BIAS

Parameter #20 (PH BIAS) controls the phase bias. It can be set anywhere from 1.0 to 8.0 amperes, in 0.5-amp steps.

The most sensitive phase bias setting (1.0 A) may not be suitable for all applications. The setting should be selected on a case by case basis. Applications that require a higher setting are lines with high charging current, lines with heavy tapped loads, and those with CT errors greater than allowed for in (2) below. The 1.0 A minimum setting is based on an "error budget" that has three components:

1. A 0.25-amp "false differential current" caused by net line charging or a tapped load. (Net line charging includes the effect of any line-connected shunt reactors).
2. 0.5 amperes for analog and digital resolution errors. This includes main CT errors at low current, ACT error, A/D converter quantizing errors, and rounding errors in the local and remote charges.
3. A 0.25-ampere safety factor.

Components 2 and 3 remain the same for many applications. Component 1 (false differential current) remains 0.25 ampere for all untapped overhead lines up to about 50 miles in length, and all underground cables up to about 5 miles in length. Tapped lines, 3-terminal lines, and longer lines will require a higher phase bias setting.

EXAMPLES

Tapped Line

A 20-mile overhead line has a tap that draws a maximum secondary load current of .2 ampere. A multi-phase fault on the low side of the transformer draws 2.0 ampere, based on transformer impedance only. As described in Section 2, the phase bias is set at three times the let-through current, or 6.0 amperes. This setting accommodates full dc offset and includes Components 2 and 3 listed above.

Long Line

A 150-mile, overhead EHV line has a total charging current of 0.75 secondary amperes. Since this exceeds the 0.25-ampere value of Component 1 above, the phase bias must be set to the first level above minimum, or 1.5 amperes.

3-Terminal Line

Since an additional terminal with its own 0.5 ampere analog and digital resolution errors is present in the system, a minimum phase bias setting of at least 1.5 amperes is recommended.

Very Long Line With Shunt Reactor Compensation

A 200-mile, 500-kV line has shunt reactors within the RFL 9300's zone of protection. These reactors prevent overvoltage under light-load conditions. The total capacitive current is 1.0 secondary amperes. The shunt compensation is 50 percent, or 0.5 amperes. This results in a net line charging current of 0.5 ampere, which is slightly above Component 1 of the error budget. Therefore, a phase bias setting of 1.5 ampere is appropriate.

Table 4-1. Programmable parameters, RFL 9300 Two-Terminal Charge Comparison System

No.	Display	Definition	Range	Step	Default	Setting
20	PH BIAS	Phase bias	1.0 to 8.0 A	0.5 A	8.0 A	
21	GND BIAS	Ground bias	1.0 to 2.25 A	0.25 A	2.25 A	
22	BIAS CTL	Bias control	ENABLE/DISABLE	. . .	ENABLE	
23	GND DLY	Ground delay	ENABLE/DISABLE	. . .	ENABLE	
24	DLAY SEC	Bias control and ground delay time	Bias: 50 to 1000 ms Ground: 50 ms to 30 s	50 ms Variable (1)	1000 ms 30 s	
25	FD PHASE	Local phase fault detector current	6 or 8 A	. . .	8 A	
26	FD GND	Local ground fault detector current	0.5 or 1.0 A	. . .	1.0 A	
27	BACKUP	System backup functions	ENABLE/DISABLE (See note 8)	. . .	DISABLE	
28	PH OC BU	Phase overcurrent backup	6 to 31.875 A	0.125 A	31.875 A	
29	G OC BU	Ground overcurrent backup	1 to 31 A	0.125 A	31 A	
30	PH TOC	Phase inverse time-overcurrent enable/disable	ENABLE/DISABLE	. . .	DISABLE	
31	P PICKUP	Phase inverse time-overcurrent pickup value	0.5 to 31.875 A	0.125 A	31.875 A	
32	PH CURVE	Phase inverse time-overcurrent curve select	See note 6	. . .	USA 1	
33	PH DIAL	Phase inverse time-overcurrent dial setting	See note 6	. . .	SET 15.0	
34	GND TOC	Ground inverse time-overcurrent enable/disable	ENABLE/DISABLE	. . .	DISABLE	
35	G PICKUP	Ground inverse time-overcurrent pickup value	0.5 to 31.0 A	0.125 A	31.0 A	
36	G CURVE	Ground inverse time-overcurrent curve select	See note 7	. . .	USA 1	
37	GND DIAL	Ground inverse time-overcurrent dial setting	See note 7	. . .	SET 15.0	
38	OVHD/UGD	Overhead or underground cable	OVHD or UGD	. . .	UGD	
39	OPEN CON	Open conductor action	ALARM or TRIP	. . .	ALARM	
41	CM ALM D	Communications alarm delay	ENABLE/DISABLE	. . .	ENABLE	
42	DC FILT	Dc filter for tapped load applications	ENABLE/DISABLE	. . .	ENABLE	
43	DEFAULT	Resets Parameter #'s 20 - 52 to default values	ENABLE/DISABLE	. . .	DISABLE (2)	
44	BEEPER	Enable/disable audible beeper	ENABLE/DISABLE	. . .	ENABLE (3)	
45	DISPLAY	Adjust display intensity	4 levels	. . .	Brightest (4)	
46	XMIT ADD1	Select transmit address 1	16 to 4079	1	0000	
48	COM MODE	Selects hot standby communications mode	AUTO/MAN	. . .	AUTO	
49	ACT CHAN	Selects channel for hot standby communications	CH 1/CH 2	. . .	(5)	
50	G B4 TRP	Guard before trip	ENABLE/DISABLE	. . .	ENABLE	
51	RS232 BD	Selects RS-232 baud rate	1200, 2400, 9600	. . .	9600	
52	RS232 PR	Selects RS-232 handshaking protocol	XON/XOFF or RTS/CTS	. . .	XON/XOFF	
141	SEL POLE	Selective pole relaying enable/disable	ENABLE/DISABLE	. . .	DISABLE *	
145	TRIP RLS	Selects trip release algorithm	3 modes	. . .	TRIP + 100	

* Only when single pole trip is active

>> Refer to page 4-4 for notes <<

Table 4-2. Programmable parameters, RFL 9300 Three-Terminal Charge Comparison System

No.	Display	Definition	Range	Step	Default	Setting
20	PH BIAS	Phase bias	1.0 to 8.0 A	0.5 A	8.0 A	
21	GND BIAS	Ground bias	1.0 to 2.25 A	0.25 A	2.25 A	
22	BIAS CTL	Bias control	ENABLE/DISABLE	. . .	ENABLE	
23	GND DLY	Ground delay	ENABLE/DISABLE	. . .	ENABLE	
24	DLAY SEC	Bias control and ground delay time	Bias: 50 to 1000 ms Ground: 50 ms to 30 s	50 ms Variable (1)	1000 ms 30 s	
25	FD PHASE	Local phase fault detector current	6 or 8 A	. . .	8 A	
26	FD GND	Local ground fault detector current	0.5 or 1.0 A	. . .	1.0 A	
27	BACKUP	System backup functions	ENABLE/DISABLE (See note 8)	. . .	DISABLE	
28	PH OC BU	Phase overcurrent backup	6 to 31.875 A	0.125 A	31.875 A	
29	G OC BU	Ground overcurrent backup	1 to 31 A	0.125 A	31 A	
30	PH TOC	Phase inverse time-overcurrent enable/disable	ENABLE/DISABLE	. . .	DISABLE	
31	P PICKUP	Phase inverse time-overcurrent pickup value	0.5 to 31.875 A	0.125 A	31.875 A	
32	PH CURVE	Phase inverse time-overcurrent curve select	See note 6	. . .	USA1	
33	PH DIAL	Phase inverse time-overcurrent dial setting	See note 6	. . .	SET 15.0	
34	GND TOC	Ground inverse time-overcurrent enable/disable	ENABLE/DISABLE	. . .	DISABLE	
35	G PICKUP	Ground inverse time-overcurrent pickup value	0.5 to 31.0 A	0.125 A	31.0 A	
36	G CURVE	Ground inverse time-overcurrent curve select	See note 7	. . .	USA1	
37	GND DIAL	Ground inverse time-overcurrent dial setting	See note 7	. . .	SET 15.0	
38	OVHD/UGD	Overhead or underground cable	OVHD or UGD	. . .	UGD	
39	OPEN CON	Open conductor action	ALARM or TRIP	. . .	ALARM	
41	CM ALM D	Communications alarm delay	ENABLE/DISABLE	. . .	ENABLE	
43	DEFAULT	Resets Parameter #'s 20 - 52 to default values	ENABLE/DISABLE	. . .	DISABLE (2)	
44	BEEPER	Enable/disable audible beeper	ENABLE/DISABLE	. . .	ENABLE (3)	
45	DISPLAY	Adjust display intensity	4 levels	. . .	Brightest (4)	
46	XMIT ADD1	Select transmit address 1	16 to 4079	1	0000	
47	XMIT ADD2	Select transmit address 2	16 to 4079	1	0000	
50	G B4 TRP	Guard before trip	ENABLE/DISABLE	. . .	ENABLE	
51	RS232 BD	Selects RS-232 baud rate	1200, 2400, 9600	. . .	9600	
52	RS232 PR	Selects RS-232 handshaking protocol	XON/XOFF or RTS/CTS	. . .	XON/XOFF	
141	SEL POLE	Selective pole relaying enable/disable	ENABLE/DISABLE	. . .	DISABLE *	
145	TRIP RLS	Selects trip release algorithm	3 modes	. . .	TRIP + 100	

* Only when single pole trip is active

>> Refer to page 4-4 for notes <<

Notes for Tables 4-1 and 4-2:

1. Bias control and ground delay settings will track each other from 50 ms to 750 ms. Above 750 ms, the ground delay varies in non-proportional steps:

Bias	**Ground**
800 ms	2 s
850 ms	5 s
900 ms	10 s
950 ms	15 s
1000 ms	30 s

2. When this parameter is enabled and the **[ENT]** key is pressed, the Display Controller requests that the PROGRAM mode security code (.248) be entered. Once it is, all parameter values will be reset to the default values listed above. These are the values the parameters are set to before the RFL 9300 leaves the factory.

3. When this parameter is set to ENABLE, the audible beeper can be used to notify the operator if an alarm condition exists. During prolonged alarm conditions, the user may wish to disable the beeper until the condition is corrected. It is recommended that this parameter remain enabled. Alarms may not be noticed if the display is in the READ or PROGRAM mode, or if the RFL 9300 is not being manned and the user is depending on the beeper to indicate an alarm condition.

4. When this parameter is shown, the **[8]** and **[0]** keys can be used to increase or decrease the display intensity (or brightness). When the setting is changed, the bottom line of the display will change to the new intensity, while the top line unit remains constant as a reference. When the **[ENT]** key is pressed, both lines assume the new intensity setting.

5. In dual-channel systems, either channel number may be displayed if COMM MODE (Parameter #48) is set to AUTO.

6. Settings for phase inverse time-overcurrent backup parameters:
(Parameters 31, 32, 33 are only programmable if parameter #30 is enabled.)

Phase inverse time-overcurrent Dial Setting when phase inverse time-overcurrent Curve Select is: USA 1, USA 2, USA 3 or USA 4	Phase inverse time-overcurrent Dial Setting when phase inverse time-overcurrent Curve Select is: IEC 1 , IEC 2, IEC 3 or IEC 4
SET 0.5 SET 1.0 SET 2.0 SET 3.0 SET 4.0 SET 5.0 SET 6.0 SET 8.0 SET 10.0 SET 12.0 SET 15.0	SET 0.05 SET .1 SET .2 SET .3 SET .4 SET .5 SET .6 SET .7 SET .8 SET .9 SET 1.0

7. Settings for ground inverse time-overcurrent backup parameters:
(Parameters 35, 36, 37 are only programmable if parameter #34 is enabled.)

Ground inverse time-overcurrent Dial Setting when ground inverse time-overcurrent Curve Select is: USA 1, USA 2, USA 3 or USA 4	Ground inverse time-overcurrent Dial Setting when ground inverse time-overcurrent Curve Select is: IEC 1, IEC 2, IEC 3 or IEC 4
SET 0.5 SET 1.0 SET 2.0 SET 3.0 SET 4.0 SET 5.0 SET 6.0 SET 8.0 SET 10.0 SET 12.0 SET 15.0	SET 0.05 SET .1 SET .2 SET .3 SET .4 SET .5 SET .6 SET .7 SET .8 SET .9 SET 1.0

8. Backup ENABLE/DISABLE is not a programmable parameter when stub-bus function is active (See 3.13).

4.2.2 GND BIAS - GROUND BIAS

Parameter #21 (GND BIAS) controls ground bias. It can be set anywhere from 1.0 to 2.25 amperes, in 0.25-amp steps. The error budget components for ground bias are the same as previously listed for phase bias (0.25 amperes for false differential current, 0.5 amperes for analog and digital resolution errors, and 0.25 ampere for a safety factor.)

Fortunately, most tapped load transformers are delta-connected on the high-side and grounded-wye-connected on the low-side. This blocks the flow of zero-sequence current, and permits a sensitive setting for the ground bias, even for lines with heavy tapped loads.

The same method used to calculate the net line charging current is used to calculate the ground bias calibration. Of course, this calculation is now based on **zero-sequence** capacitive current.

4.2.3 BIAS CTRL - BIAS CONTROL

Parameter #22 (BIAS CTL) is used for Bias Control. It can either be enabled or disabled. When enabled, the phase bias and ground bias levels are boosted for a preset interval (See paragraph 4.2.5).

Bias control is enabled to adapt the RFL 9300 to the characteristics of many applications. For example, underground cables and long overhead lines may have a large capacitive inrush current when first energized (See paragraph 4.2.19). This inrush appears as false differential to the RFL 9300. The inrush current may be rich in harmonic content.

High harmonics tend to prevail during line charging, because the limiting impedance is net capacitive. Even so, there may be certain applications where the characteristic of the inrush current may look to the RFL 9300 like a low-grade internal fault. (An example of this would be a very long line energized from a weak source.)

To prevent tripping in these cases, bias control should be enabled. This boosts the phase bias and ground bias levels by either 1.5 or 3.0 amperes for a preset interval. (The next setting controls this interval.)

Because of the safety margin and line charging current accommodation built into the phase bias and ground bias settings, bias control should not be needed in almost all applications. Unless it is needed, it should be disabled.

4.2.4 GND DLY - GROUND DELAY

Parameter #23 (GND DLY) controls the RFL 9300's ground trip delay function. It can be set to either ENABLE or DISABLE.

As explained in the discussion of tapped loads in Section 2 of this manual, some tap transformers will allow $3I_0$ to flow from the high-side to low-side faults. For these applications, this parameter may have to be enabled.

Whenever this parameter is enabled, all $3I_0$ trips are delayed by the time delay that was set by the GROUND DELAY parameter (50 ms to 30 seconds).

4.2.4.1 3IO TRIP ALGORITHM

When the RFL 9300 relay is configured for single-pole operation the GROUND DELAY parameter takes an additional role. In certain situations, the ground bias may be set to be much more sensitive than the phase bias. In the event that the 3IO controller calculates a trip, all three phase controllers will be commanded to trip in the event that none of them issues a trip signal by the time the GROUND DELAY timer expires. GROUND DELAY must be enabled in order to enable the 3IO trip algorithm. If the GROUND DELAY function is not enabled, trips calculated by the 3IO controller will have no effect in RFL 9300 single-pole trip applications.

4.2.5 DLAY SEC - TIME DELAY

Parameter #24 (DLAY SEC) is a time delay setting that controls two RFL 9300 functions: bias control (parameter #22) and ground delay (parameter #23). The following settings are available:

Setting	Bias Control	Ground Delay
.05/.05	50 ms	50 ms
.1/.1	100 ms	100 ms
.15/.15	150 ms	150 ms
.2/.2	200 ms	200 ms
.25/.25	250 ms	250 ms
.3/.3	300 ms	300 ms
.35/.35	350 ms	350 ms
.4/.4	400 ms	400 ms
.45/.45	450 ms	450 ms
.5/.5	500 ms	500 ms
.55/.55	550 ms	550 ms
.6/.6	600 ms	600 ms
.65/.65	650 ms	650 ms
.7/.7	700 ms	700 ms
.75/.75	750 ms	750 ms
.8/2	800 ms	2 s
.85/5	850 ms	5 s
.9/10	900 ms	10 s
.95/15	950 ms	15 s
1/30	1000 ms	30 s

Bias control provides security during capacitive inrush current. Ground delay provides security during inductive inrush current (such as for a low-side fault on a tapped line). Since both are “in-rush” events, a common timer is used.

Most applications will not require trip suppression for either inrush condition. This means that bias control and ground delay will both be disabled. If they are both disabled, the time delay setting will have no effect on RFL 9300 performance.

If either bias control or ground delay parameters are enabled, the time delay setting should be made long enough to override the inrush condition, plus a safety margin.

As of the date this manual was published, no guidelines have been established for those rare applications where a time delay setting must be made. These are unusual cases that are completely dependent on the parameters of the power system. Field measurements, EMTP-type studies, or TNA studies may be required on a case-by-case basis to determine the proper setting.

If the ground delay parameter is enabled specifically for the purpose of enabling the 3IO single-pole trip algorithm it is recommended that a setting of 50ms be used. Keep in mind that the ground delay timer does not start until the time a 3IO trip signal would have been issued in a three-pole application. This means that with a 50ms setting the timer may not expire until as much as 80 to 90ms after the fault. Remember that trip signals are calculated at the conclusion of positive half-cycles of line current. Should a positive half-cycle terminate just prior to the 50ms time-out it will be an additional 16ms before the 3IO trip will be transmitted to the 93B SV which must then pass the trip command to the phase controllers.

4.2.6 FD PHASE - PHASE FAULT DETECTOR

Parameter #25 (FD PHASE) controls the local phase overcurrent fault detector. It can be set to either 6 amperes or 8 amperes. It should be set above the maximum expected load, with a 10 to 15-percent safety margin. 6 amperes will be suitable for most applications. The phase overcurrent fault detector is triggered when the peak true CT current value exceeds the peak value of the setting i.e. 8.5A pk for a 6Arms setting and 11.25A for a 8Arms setting.

A high fault detector current setting does not compromise sensitivity, because the steady-state fault detector is supplemented by several current-change fault detectors that are very sensitive. The fault detectors are always monitoring the true CT current regardless of whether the relay is configured for 2-terminal or 3-terminal operation. These detectors require no settings, and include the following:

- Peak Change
- Pulse-Width Change
- Slope Change
- Polarity Change

4.2.7 FD GND - GROUND FAULT DETECTOR

Parameter #26 (FD GND) controls the local ground overcurrent fault detector current. It can be set to either 0.5 amperes or 1.0 amperes. It should be set above the maximum expected $3I_0$ due to unbalanced load. 0.5 amperes will be suitable for most applications. The ground overcurrent fault detector monitors the integral value of the true CT current in order to de-sensitize its response to transients.

4.2.8 BACKUP - SYSTEM BACKUP FUNCTIONS

Parameter #27 (BACKUP) controls the RFL 9300's system backup functions. It can either be enabled or disabled. There are four back-up functions:

1. High-Set Overcurrent (Instantaneous)

2. Inverse Time Overcurrent (See 4.2.11 and 4.2.15)

3. Loss-Of-Load

4. Switch-Into-Fault

All back-up functions, with the exception of the Phase and Ground Inverse Time Overcurrent functions, become active whenever the channel is lost and back-up has been enabled. The Phase and Ground Inverse Time Overcurrent functions have an additional Enable/Disable setting (Parameters #30 and #34). This allows the operator the option of disabling these functions while the rest of the backup functions are enabled. However if parameter #27 is disabled, the Phase and Ground Inverse Time Overcurrent functions are disabled, regardless of the settings of Parameters #30 and #34. The current values used by all backup functions are based on the integral of the absolute value of the true CT current samples (charge) calculated over the 8 ms interval that includes the latest sample. They do not reference the zero-crossings of the input current waveforms.

When stub-bus mode is active (89B disconnect switch applied to the relay) the RFL 9300 is forced into backup mode regardless of the setting of parameter #27. While this special case applies, only the High-Set Overcurrent (Instantaneous) function will become active. The Phase and Ground Inverse Time Overcurrent functions will only become active if they are enabled (i.e. parameters #30 or #40 are enabled).

For most applications, backup should be disabled. This is particularly true where there are other "truly redundant" line protection systems that operate in parallel with the RFL 9300. Backup is not required in applications where the RFL 9300 and the parallel protection do not have expected common failure modes.

4.2.9 PH OC BU - PHASE OVERCURRENT BACKUP

Parameter #28 (PH OC BU) is used to control the phase overcurrent backup trip setting. It can be set anywhere from 6.0 amperes to 31.875 amperes, in 0.125-ampere steps.

The phase overcurrent backup value should be set above the maximum expected contribution to an external fault. On very short lines, this contribution for bus faults may exceed the maximum available setting. An overtrip of the RFL 9300 overcurrent back-up for this rare event may be acceptable. Also, faults on adjacent lines close to the bus will usually produce enough infeed effect to prevent an overtrip.

4.2.10 G OC BU - GROUND OVERCURRENT BACKUP

Parameter #29 (G OC BU) controls the RFL 9300's ground overcurrent backup trip setting. It can be set anywhere from 1.0 ampere to 31.0 amperes, in 0.125 ampere steps.

The ground overcurrent backup value should be set above the maximum expected $3I_0$ contribution to an external fault. The comments regarding phase overcurrent back-up also apply to ground overcurrent back-up.

4.2.11 PH TOC - PHASE INVERSE TIME OVERCURRENT ENABLE/DISABLE

Parameter #30 (PH TOC) controls the RFL 9300's phase inverse time overcurrent backup function. This function can be enabled using parameter #30 only if the operator enables backup mode operation (parameter #27). See paragraph 6.7 for more information.

4.2.12 P PICKUP - PHASE INVERSE TIME OVERCURRENT PICKUP VALUE

Parameter #31 (P PICKUP) controls the RFL 9300's phase inverse time overcurrent pickup value. See paragraph 6.7 for more information.

4.2.13 PH CURVE - PHASE INVERSE TIME OVERCURRENT CURVE SELECT

Parameter #32 (PH CURVE) controls the RFL 9300's phase inverse time overcurrent curve select. See paragraph 6.7 for more information.

4.2.14 PH DIAL - PHASE INVERSE TIME OVERCURRENT DIAL SETTING

Parameter #33 (PH DIAL) controls the RFL 9300's phase inverse time overcurrent dial setting. See paragraph 6.7 for more information.

4.2.15 GND TOC - GROUND INVERSE TIME OVERCURRENT ENABLE/DISABLE

Parameter #34 (GND TOC) controls the RFL 9300's ground inverse time overcurrent backup function. This function can be enabled using parameter #34 only if the operator enables backup mode operation (parameter #27). See paragraph 6.7 for more information.

4.2.16 G PICKUP - GROUND INVERSE TIME OVERCURRENT PICKUP VALUE

Parameter #35 (G PICKUP) controls the RFL 9300's ground inverse time overcurrent pickup value. See paragraph 6.7 for more information.

4.2.17 G CURVE - GROUND INVERSE TIME OVERCURRENT CURVE SELECT

Parameter #36 (G CURVE) controls the RFL 9300's ground inverse time overcurrent curve select. See paragraph 6.7 for more information.

4.2.18 GND DIAL - GROUND INVERSE TIME OVERCURRENT DIAL SETTING

Parameter #37 (GND DIAL) controls the RFL 9300's ground inverse time overcurrent dial setting. See paragraph 6.7 for more information.

4.2.19 OVHD/UGD - OVERHEAD OR UNDERGROUND CABLE

Parameter #38 (OVHD/UGD) sets the RFL 9300 for use with overhead or underground cables. This parameter only has meaning if the Bias Control Function (parameter #22) is enabled. It should be set to "OVHD" if the protected line is an overhead line, or an underground line that is shorter than about 10 miles (16 km). This parameter should be set to "UGD" if the RFL 9300 is protecting an underground line that is longer than about 10 miles (16 km).

The "UGD" setting adds another 1.5 amperes of desensitization to the bias control, or a total of 3.0 amperes. This increment applies to both the phase bias and the ground bias. The following example shows how this works:

	Phase	**Ground**
Bias Setting:	2.0A	1.5A
Bias Control Increment:		
OVHD Setting:	1.5A	1.5A
UGD Setting:	3.0A	3.0A
Actual Bias During Bias Control Interval:		
OVHD Setting:	3.5A	3.0A
UGD Setting:	5.0A	4.5A

4.2.20 OPEN CON - OPEN CONDUCTOR

Parameter #39 (OPEN CON) determines how the RFL 9300 responds to open conductors in the protected line. It can be set to either ALARM or TRIP.

As explained in paragraph 3.16 of this manual, most open conductors also involve a ground fault. These conditions are detected by charge comparison. The rare case of an open conductor without a ground fault is detected in the RFL 9300 by a loss-of-load condition that persists for Zone 2 time (which is factory set at 500 ms).

In most applications, this parameter should be set to "TRIP." The exposure to an overtrip is very rare: an open conductor, not involving ground, on an adjacent line that has no other load or generation connected to the remote bus.

4.2.21 CM ALM D - COMMUNICATIONS ALARM DELAY

Parameter #41 (CM ALM D) controls the action of the RFL 9300's communications alarm relay. It does this be enabling or disabling a 5-second delay timer in the relay drive circuit.

If this parameter is set to ENABLE, the TX/RX indicator on the RFL 93 SV Supervisor Controller will light as soon as a communications failure is detected. Five seconds later, the communications alarm relay will change state; indicating the alarm. If this parameter is set to DISABLE, the indicator and relay will change state at the same time.

4.2.22 DC FILT - DC FILTER

Parameter #42 (DC FILT), when enabled, blocks operation for wide half-cycles (greater than 10 ms). For heavy tapped load applications, this parameter should be enabled. DC FILT is not displayed when the RFL 9300 is configured for 3-terminal operation.

4.2.23 DEFAULT - RESETTING TO DEFAULT

Parameter #43 (DEFAULT) resets all of the RFL 9300's programmable parameters to their most secure setting. Tables 4-1 and 4-2 show the factory default settings for each parameter. These settings are based on maximum security. During laboratory evaluation, you may want to use the factory default settings to make all settings as secure as possible.

Any time you reset to default, any parameter settings you have made will be erased from memory and permanently lost.

NOTE

This parameter is not displayed in the APRIL Read Settings menus of Figures 6-10 and 6-11, or the parameter settings list of Figure 6-24.

4.2.24 BEEPER - BEEPER CONTROL

Parameter #44 (BEEPER) controls the RFL 9300's audible beeper. When set to ENABLE, the beeper will sound during alarms, and occasionally during normal RFL 9300 operation. If this parameter is set to DISABLE, the beeper is silenced.

4.2.25 DISPLAY/INT. - DISPLAY INTENSITY CONTROL

Parameter #45 (DISPLAY/INT.) controls the brightness of the RFL 9300's display. It can be set to one of four brightness levels. It can be kept where it is for now; later, when the RFL 9300 is installed in the field, you may want to adjust the intensity to suit the ambient light conditions.

NOTE

This parameter is not displayed in the APRIL Read Settings menus of Figures 6-10 and 6-11, or the parameter settings list of Figure 6-24.

4.2.26 XMT ADD1 - TRANSMIT ADDRESS 1

Parameter #46 (XMT ADD1) is the address of the local unit. It is user selectable from 0016 to 4079. This address gets transmitted to the corresponding remote unit for address verification. The sum of the local address and the remote address must equal 4095. For example, if the local address is 4000, then the remote address must be 0095. The transmit address #1 feature of the RFL 9300 is disabled when XMT ADD1 = 0000.

4.2.27 XMT ADD2 - TRANSMIT ADDRESS 2

Parameter #47 (XMT ADD2) is the address of the local unit. It is user selectable from 0016 to 4079. This address gets transmitted to the corresponding remote unit for address verification. The sum of the local address and the remote address must equal 4095. For example, if the local address is 4000, then the remote address must be 0095. The transmit address #2 feature of the RFL 9300 is disabled when XMT ADD2 = 0000. XMT ADD2 is not displayed when the relay is configured for 2-terminal operation.

4.2.28 COM MODE - COMMUNICATIONS MODE

Parameter #48 (COM MODE) controls the RFL 9300's hot standby communications mode. It can be set to "AUTO" (automatic) or "MAN" (manual).

Whenever the RFL 9300 includes the "hot standby" redundant channel, the user is given the choice of switching channels automatically every 12 hours or switching only by manual control. (In both cases, the RFL 9300 will switch automatically whenever the channel in use fails).

If the two channels are considered to be of similar quality (equal availability, S/N ratio, etc), the AUTO setting should be used. If one of the channels is preferred, the MAN setting should be used. (An example of this is a privately-owned microwave backed up by a leased telephone line.) Here, the user would command the RFL 9300 to work on the microwave channel all the time. At regular intervals (like once a week), the RFL 9300 could be manually switched to the leased-line channel for a while to monitor the status of the standby channel. COM MODE is not displayed when the RFL 9300 is configured for 3-terminal operation.

Manual channel switching is controlled by Parameter #49 below.

4.2.29 ACT CHAN - ACTIVE CHANNEL SELECTION

Parameter #49 (ACT CHAN) allows the operator to command the RFL 9300 to work over a selected channel. It can be set to either "CH 1" (Channel 1) or "CH 2" (Channel 2).

After making this setting, the RFL 9300 will communicate continuously over the selected channel, if the COM MODE parameter described above is set to "MAN." If the COM MODE parameter is set to "AUTO," the channels will switch every 12 hours. This parameter can be set on RFL 9300s equipped with two modems, two direct digital interface modules or two fiber optic transceiver modules. It will not be displayed on units configured for 3-terminal operation.

4.2.30 G B4 TRP - GUARD BEFORE TRIP

Parameter #50 (G B4 TRP)

a. 2-terminal systems: Blocks trip until at least a total of 4 CCD or 8 WCM messages have been received in succession from the remote station without a permissive trip being calculated or until the Communications Controller signals that a clear channel has been established with the remote terminal. Guard Before Trip is active when the RFL 9300 comes “on-line” following initialization or after a communications outage. If a trip is calculated while the function is active the count of received control signal messages will be reset to zero and the trip enable sequence will be re-started.

b. 3-terminal systems: Blocks trip until at least a total of 8 control messages, either CCDs or WCMs or a mix of these two messages, have been received in succession from the remote stations without a permissive trip being calculated or until the Communications Controllers signal that a clear channel has been established with both remote terminals. Guard Before Trip is active when the RFL 9300 comes “on-line” following initialization or after a communications outage. If a trip is calculated while the function is active the count of received control signal messages will be reset to zero and the trip enable sequence will be re-started.

G B4 TRP can be set to either ENABLE or DISABLE.

This parameter should be disabled if the ability to enable trip quickly after a communications disruption takes precedence over the security afforded by this function.

4.2.31 RS232 BD - RS-232 BAUD RATE

Parameter #51 (RS232 BD) allows the operator to select one of three baud rates for the RFL 9300's RS-232 port: 1200, 2400, or 9600 baud. It should be set to match the baud rate of the equipment that will be connected to the RFL 9300 through the front panel or rear panel RS-232 connectors. If you're not sure, set Parameter #52 to "9600;" this will work in most cases.

NOTE

Parameter #51, Baud Rate, is not displayed in the APRIL menus shown in Figures 6-10 and 6-11. This means that Baud Rate can only be programmed via the RFL 9300 display panel.

4.2.32 RS232 PR - RS-232 PROTOCOL

Parameter #52 (RS232 PR) allows the operator to select the handshaking protocol for the RFL 9300's RS-232 port. Two protocols are available: XON/XOFF and RTS/CTS.

XON/XOFF handshaking is also called "software handshaking." It uses commands sent through the port to control data flow, and requires no additional cable connections. RTS/CTS handshaking is also called "hardware handshaking," and requires two additional cable connections. When RTS/CTS handshaking is used and the RFL 9300 is ready to receive characters, it raises the RTS line. The RFL 9300 will not transmit its characters until it sees the CTS line go high.

Parameter #52 should be set to match the protocol of the equipment that will be connected to the RFL 9300 through the front panel or rear panel RS-232 connectors. If you're not sure, set Parameter #52 to "XON/XOFF"; this will work in most cases.

NOTE

Parameter #52, RS-232 Protocol is not displayed in the APRIL menus shown in Figures 6-10 and 6-11. This means that RS-232 Protocol can only be programmed via the RFL 9300 display panel.

4.2.33 SEL POLE – SELECTIVE POLE RELAYING

Parameter #141 (SEL POLE) is used in single-pole applications. The standard single-pole algorithm trips only the faulted phase for single-line-to-ground faults, and trips all three phases for multiphase faults which occur within a 3 second interval. If Selective Pole Relaying is enabled only the faulted phases are tripped. This means that a fault could result in one, two or three phases being tripped. SEL POLE is not displayed unless the relay is configured for single-pole operation.

4.2.34 TRIP RLS – TRIP RELEASE

Parameter #145 (TRIP RLS) determines the method used by the Display Controller to release a latched output trip signal. Three methods of trip release are available:

1. Output trip will unlatch when both the internal trip and DC trip current sense signals are no longer active.

2. Output trip will be unlatched 100ms after the internal trip signal is no longer active.

3. Output trip will be released with 0ms delay when the internal trip signal becomes inactive.

(Note that the internal trip signals are supplied by the Phase Controllers)

SECTION 5: INSTALLATION

WARNING

THE RFL 9300 MUST BE PROPERLY GROUNDED BEFORE ATTEMPTING TO CONNECT INPUT POWER. IMPROPER GROUND CONNECTIONS MAY RESULT IN SYSTEM MALFUNCTIONS, EQUIPMENT DAMAGE, OR ELECTRICAL SHOCK.

TO GROUND THE RFL 9300, CONNECT A 16 AWG OR LARGER WIRE FROM THE GROUND STUD ON THE REAR OF THE CHASSIS (SEE FIGURE 5-2) TO A SOLID EARTH GROUND. THE GROUND WIRE SHOULD BE KEPT AS SHORT AND STRAIGHT AS POSSIBLE, TO KEEP ITS RESISTANCE AND INDUCTANCE TO A MINIMUM.

THE RFL 9300 HAS A HORIZONTAL BUS BAR ACROSS THE BACK OF THE UNIT. ITS PURPOSE IS TO KEEP ALL REAR PANEL MODULES AT THE SAME POTENTIAL. IT IS CRITICAL THAT ALL BUS BAR SCREWS BE INSTALLED AND TIGHTENED TO 20 INCH-POUNDS OF TORQUE (2.26 NEWTON-METERS) WHEN THE UNIT IS IN SERVICE.

CAUTION

Before attempting to make power connections, make sure the RFL 9300's power supply can operate at the available input supply voltage. This can be determined by checking the label on the power supply front panel. If the wrong voltage is connected to the power supply, component damage will result.

During normal system operation, the switching of relay contacts can produce voltage spikes. These spikes can travel down the relay output leads and induce currents in other leads. These induced currents can result in false trips. To reduce this possibility, use a shielded twisted pair for each input lead, and ground the shield at the RFL 9300 chassis only. As an added precaution, do not bundle input, output, and power leads into the same harness - keep them as far apart as possible.

NOTE

Specific terminals on the rear panel terminal blocks are noted by the terminal block number followed by a dash and the terminal number (TB1-1, TB1-2, TB1-3).

5.1 INTRODUCTION

This section contains installation instructions for the RFL 9300, including unpacking, mounting, and interconnection wiring.

5.2 UNPACKING

RFL 9300 equipment may be supplied as individual chassis or interconnected with other chassis or assemblies as part of a system. The following paragraphs provide unpacking instructions for individual chassis, and interconnected chassis. Use the instructions that apply to your equipment.

5.2.1 INDIVIDUAL CHASSIS

RFL 9300 units supplied as individual chassis are packed in their own shipping cartons:

1. Open each carton carefully to make sure the equipment is not damaged.

2. After the chassis is removed from the carton, carefully examine all packing material to make sure no items of value are discarded.

3. Carefully remove any packing materials inserted into the chassis to hold circuit cards in place during transit.

4. Make sure all front-panel modules are fully seated in the chassis.

5.2.2 INTERCONNECTED CHASSIS

RFL 9300 units ordered as part of a larger system may be interconnected with other chassis and mounted in a relay rack or cabinet. They may also be mounted on shipping rails for installation into a rack or cabinet at the customer's site. In such cases, the entire assembly is enclosed in a wood crate or delivered by air-ride van:

1. If the equipment is crated, carefully open the crate to avoid damaging the equipment.

2. Remove the equipment from the crate and carefully examine all packing materials to make sure no items of value are discarded.

3. Carefully remove any packing materials that were inserted into the individual chassis to hold circuit cards in place during transit.

4. Make sure all front-panel modules are fully seated in the chassis.

5.3 MOUNTING

After unpacking, RFL 9300 equipment must be securely mounted, using the procedures in the following paragraphs.

5.3.1 INDIVIDUAL CHASSIS

RFL 9300's housed in individual chassis have two mounting ears (one on each side). Hole sizes and spacings conform with EIA standards, so the RFL 9300 can be mounted in any standard 19-inch rack or cabinet. Complete chassis dimensions are shown in Figures 5-1 and 5-2.

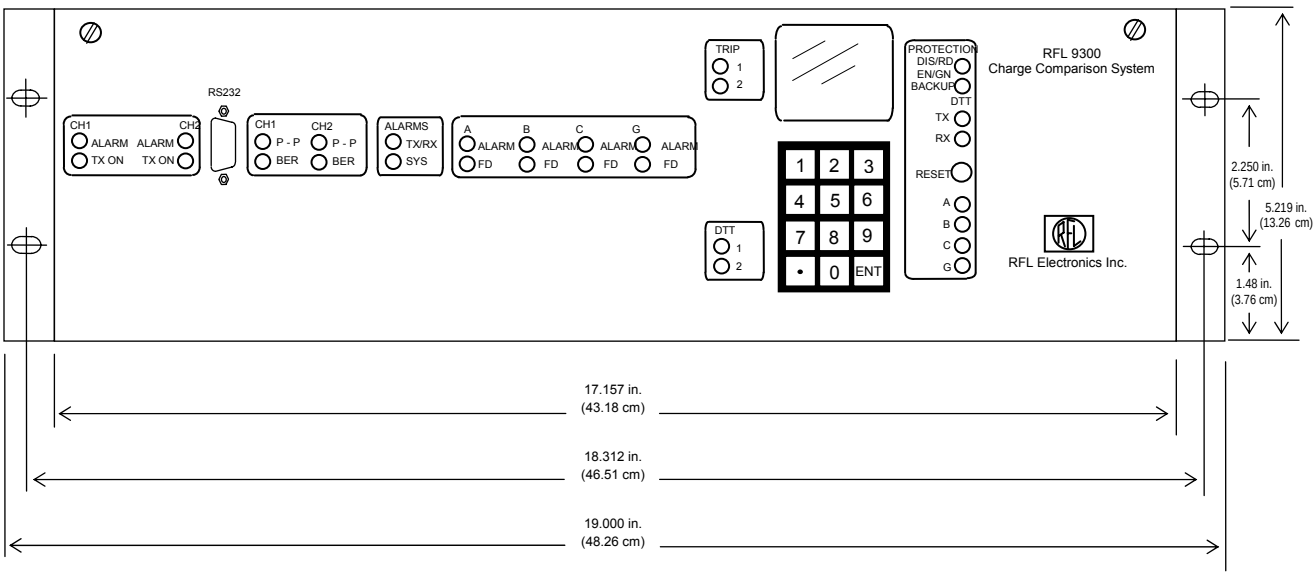


Figure 5-1. Mounting dimensions of RFL 9300 chassis without single pole option

WARNING

ON INITIAL INSTALLATION ENSURE THAT THE CPU AND DRIVER MODULES ARE FULLY SEATED INTO CONNECTORS BEFORE POWERING ON UNIT

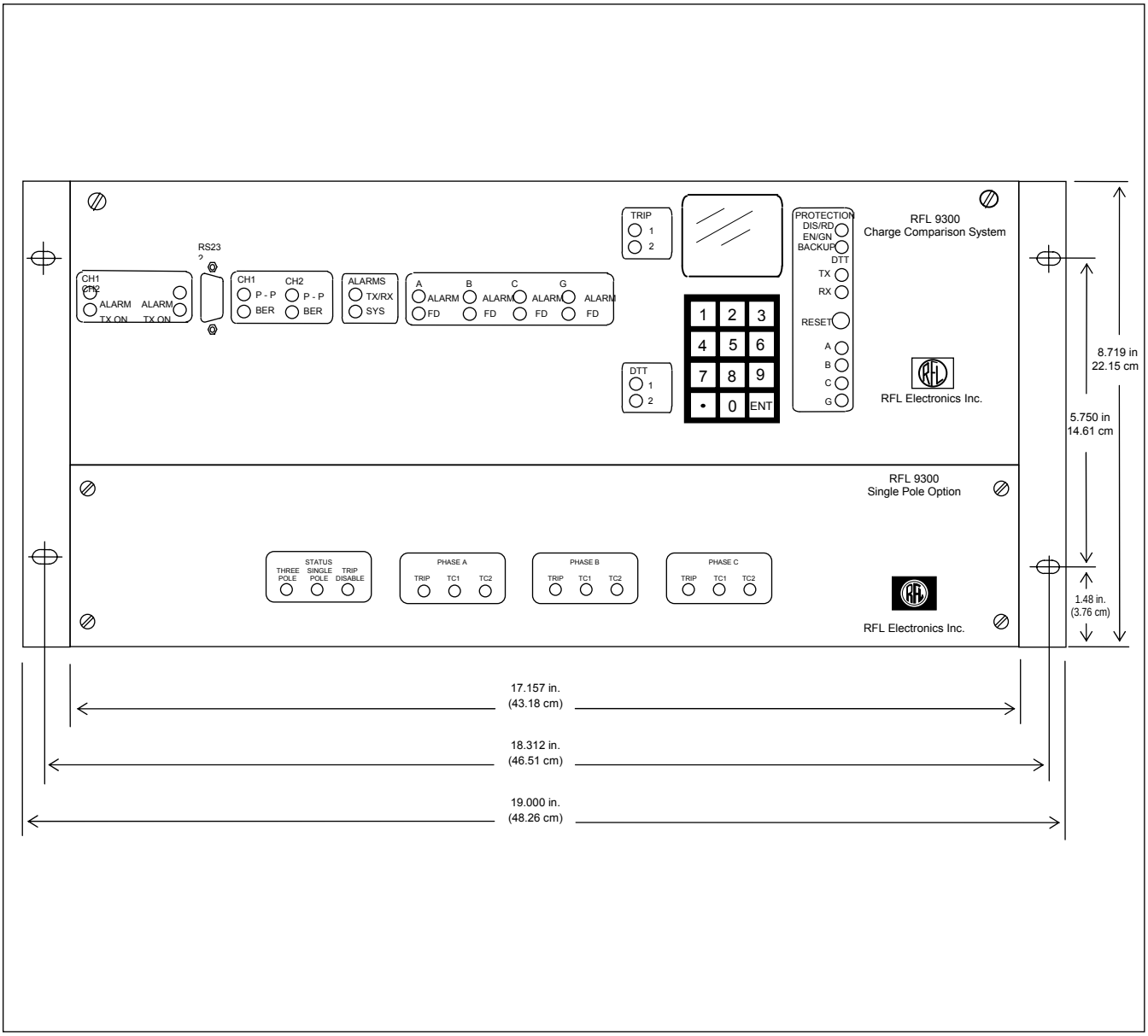


Figure 5-2. Mounting dimensions of RFL 9300 chassis with single pole option

CAUTION

Any installation using an enclosed cabinet with a swing-out rack must be securely fastened to the floor. This will prevent the cabinet from falling forward when the rack is moved outward.

5.3.2 INTERCONNECTED CHASSIS INSTALLED IN RACK OR CABINET

Systems mounted in racks or cabinets at the factory are to be placed in position and then bolted to the floor or wall, as appropriate, to secure the equipment in place. The type of hardware used will depend upon the particular surface to which the rack or cabinet is being mounted. Because of this, mounting hardware is not supplied with the rack or cabinet.

5.3.3 INTERCONNECTED CHASSIS MOUNTED ON SHIPPING RAILS

Equipment to be installed in a rack or cabinet at the customer's site is mounted on shipping rails at the factory. To remove the shipping rails and mount the equipment, proceed as follows:

1. Place the equipment as close to the front of the rack or cabinet as possible. Turn the equipment so the rear panels face the front of the rack or cabinet.
2. Remove all the screws securing the shipping rails to the equipment.
3. Slide the equipment into the rack or cabinet.
4. Install and tighten screws to all panels to secure the equipment in place.

5.4 VENTILATION

The RFL 9300's specified operating temperature range is as follows:

Horizontal-Mount Chassis: -20^{o}C to +60^{o}C (-4^{o}F to +140^{o}F).

Operation at higher temperatures may affect system reliability and performance. RFL 9300 terminals installed in enclosed cabinets should be ventilated to keep the temperature inside the cabinet within limits.

5.5 ELECTRICAL CONNECTIONS

The following paragraphs describe the electrical connections that must be made when installing the RFL 9300. The electrical connections consist of the following: connections between the RFL 9300 and the protected line, communications connections between the local and remote RFL 9300 terminals, and IRIG-B connections. Rear views of all three RFL 9300 configurations are shown in Figure 5-3. Figures 5-4 and 5-5 are **typical** wiring diagrams that show the electrical connections that must be made between the RFL 9300 and the current transformers on the protected line. Figure 5-6 shows an overview of a typical 2-terminal installation. Figure 5-7 shows an overview of a typical 3-terminal installation. For more details about the connections required in your application, refer to the "as supplied" drawings furnished with your RFL 9300.

Information is also provided in this section on making modem connections, fiber optic connections, direct digital connections, and IRIG-B connections. Use the instructions that apply to your equipment, and ignore the rest.

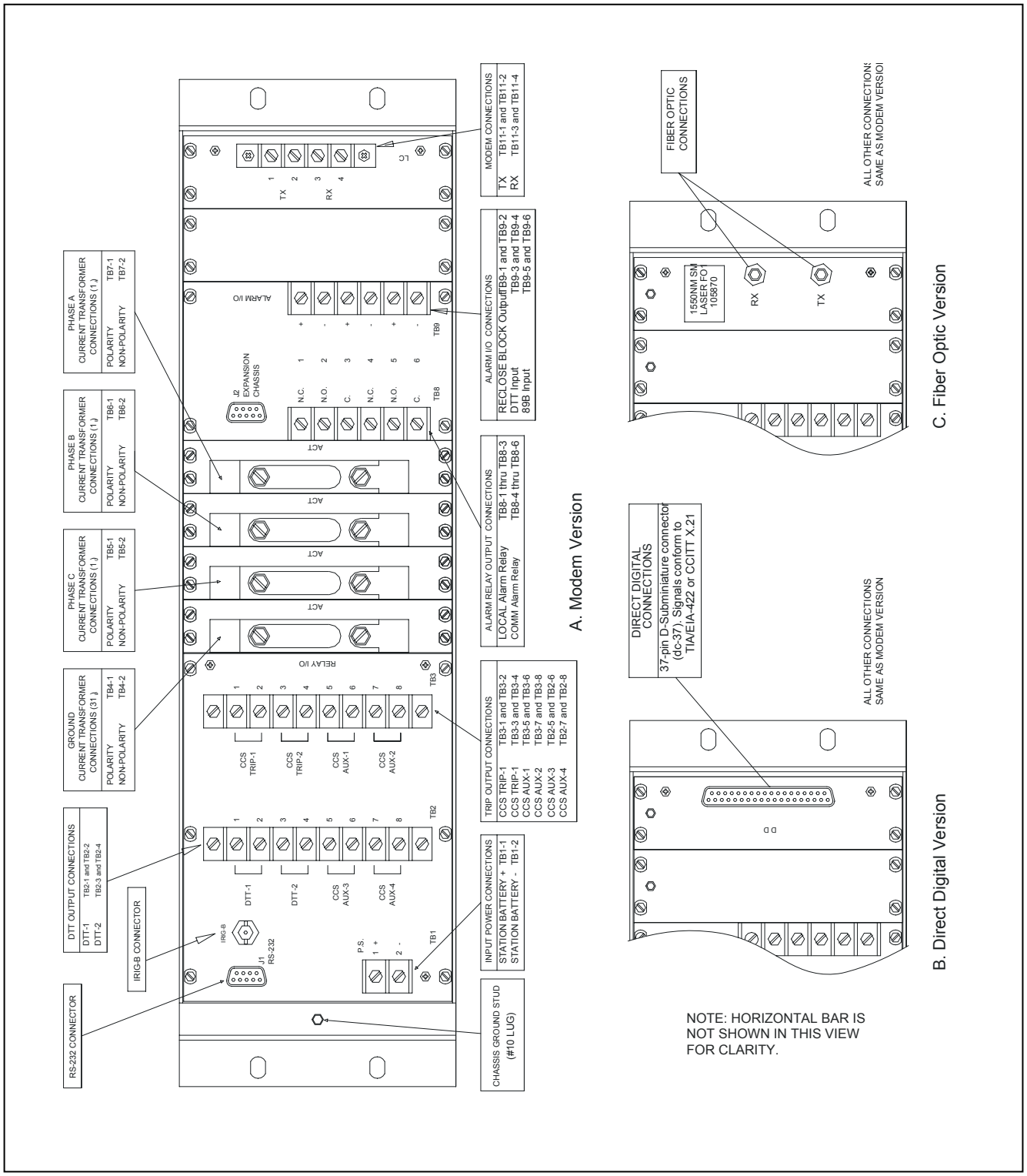


Figure 5-3. Rear view, typical RFL 9300 Charge Comparison System

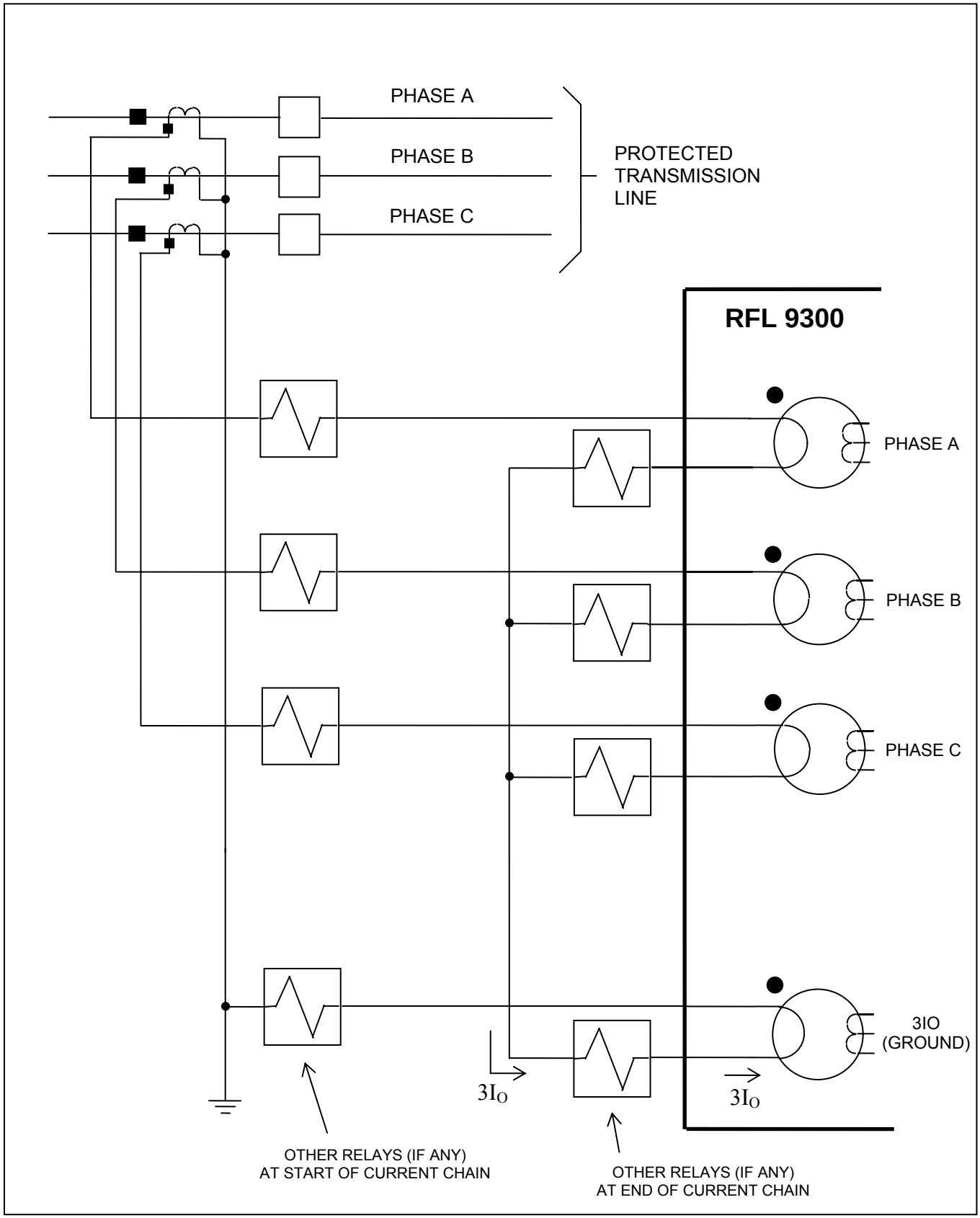


Figure 5-4. Electrical connections between RFL 9300 and current transformers on protected line

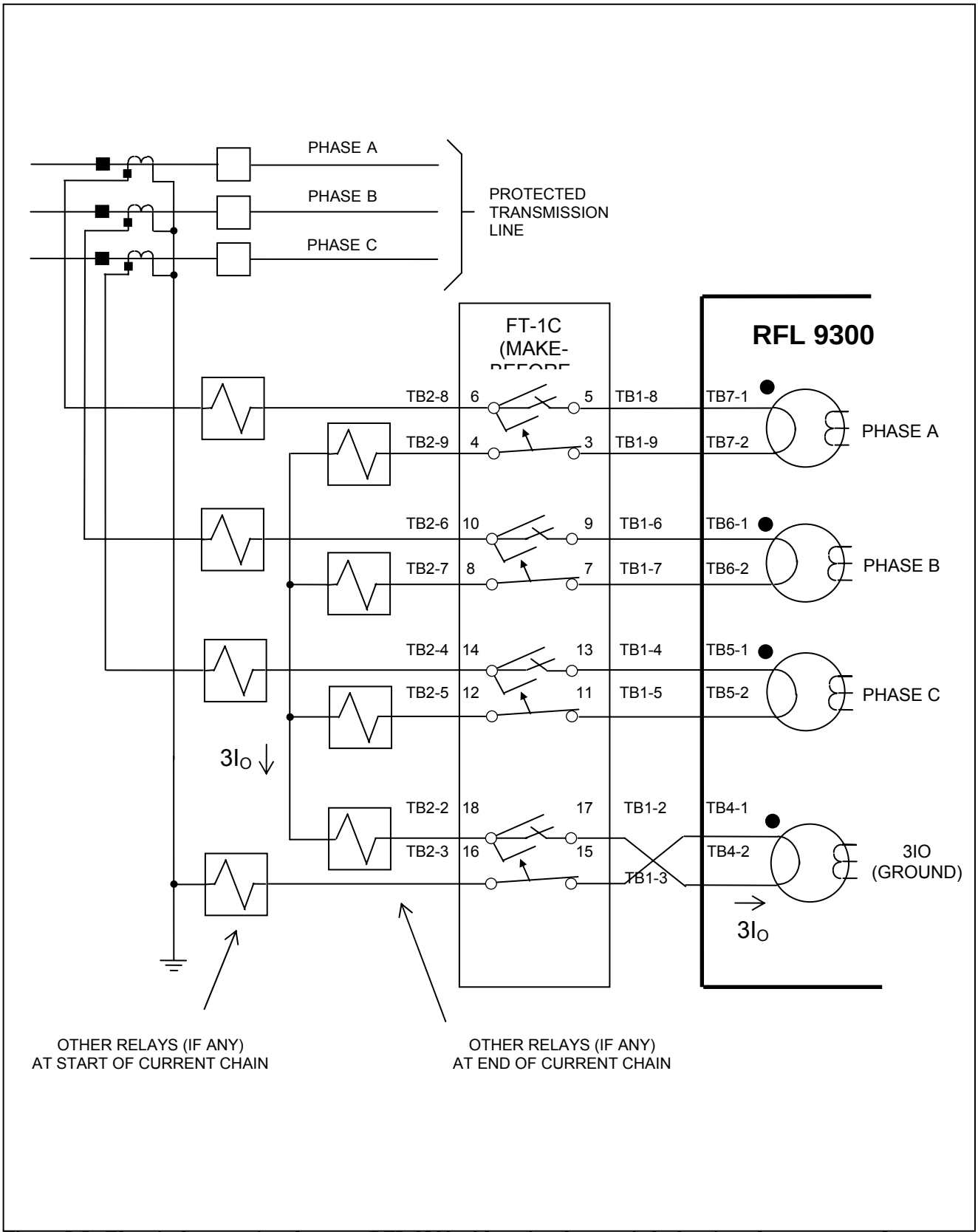


Figure 5-5. Electrical connections between RFL 9300 with optional test switch chassis and current transformers on protected line

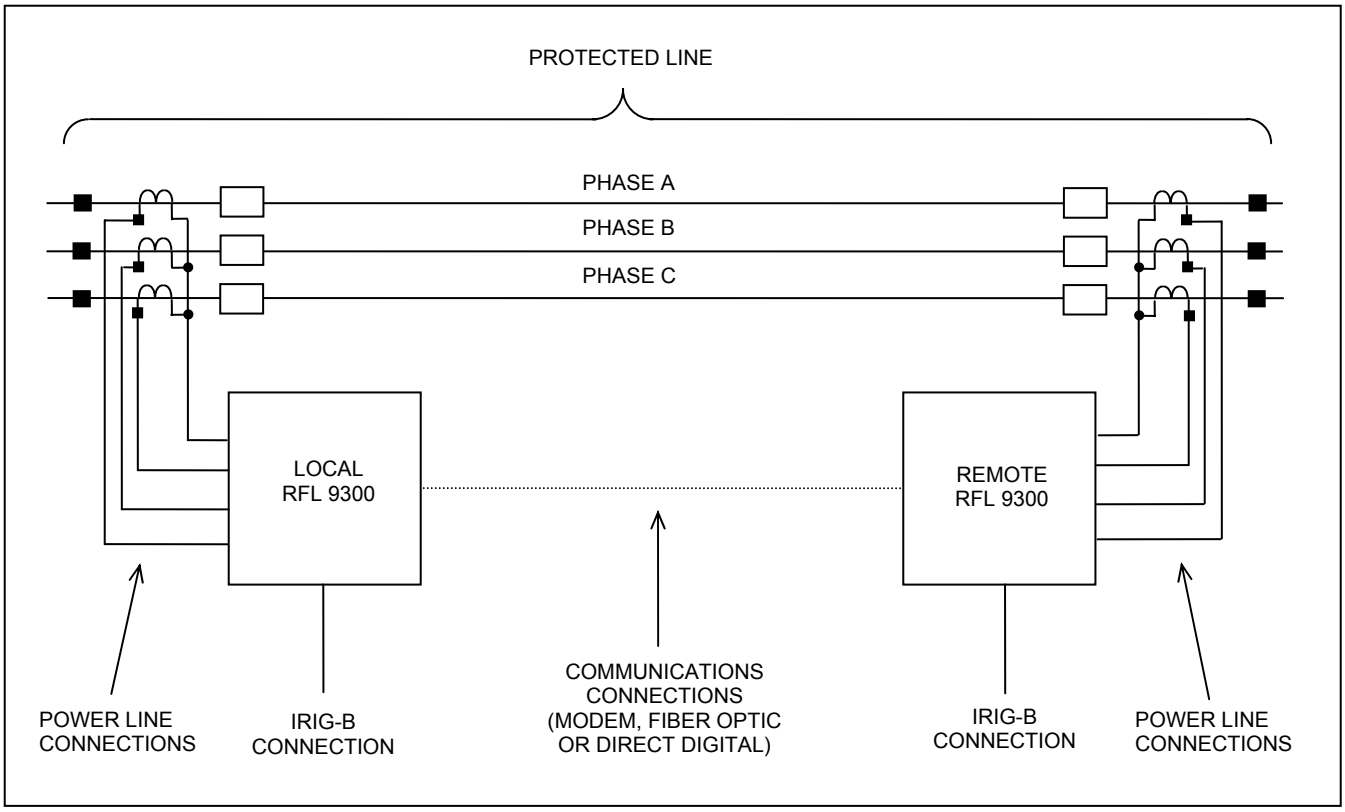


Figure 5-6. Overview of a typical 9300 two-terminal installation

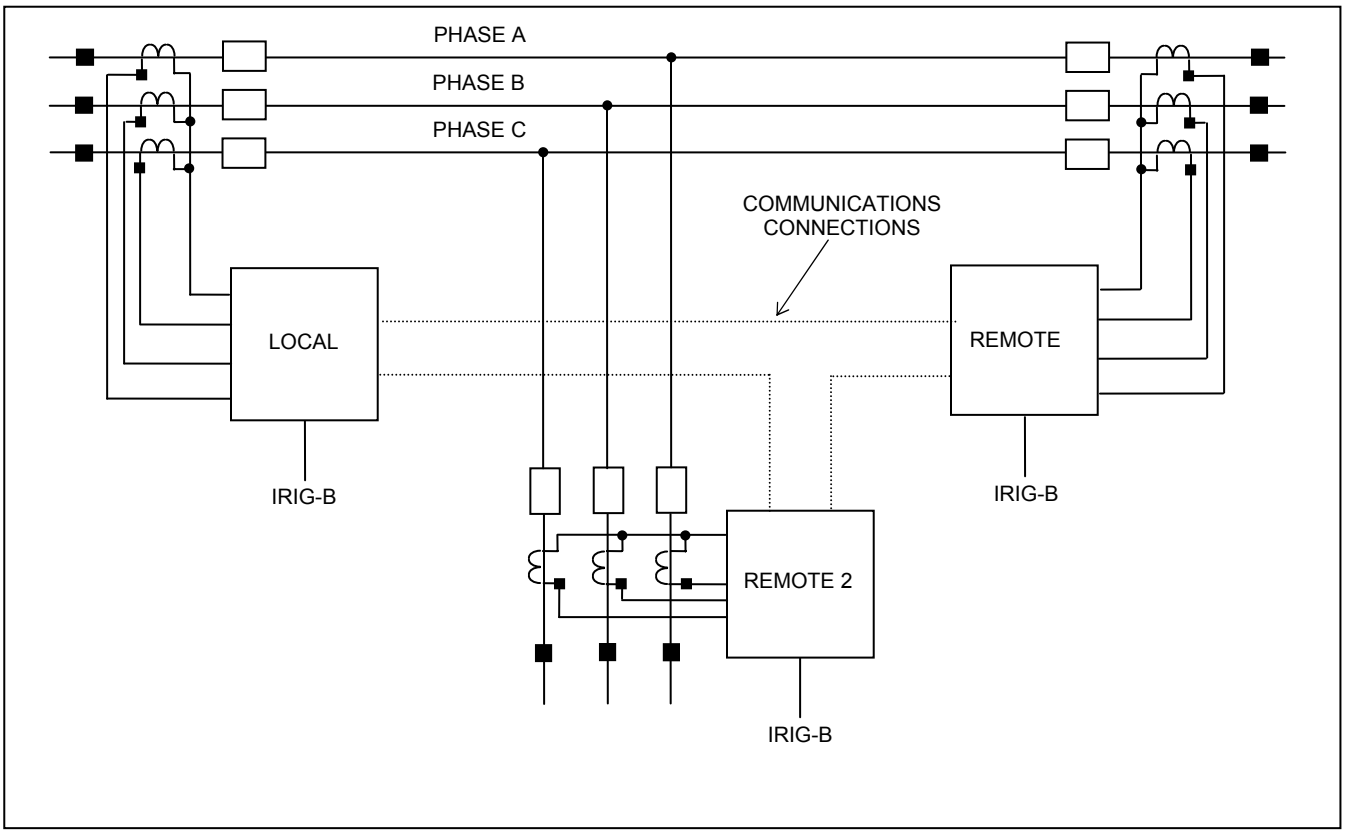


Figure 5-7. Overview of a typical RFL 9300 three-terminal installation

5.6 MODEM CONNECTIONS

The following paragraphs provide information for making connections to the RFL 9300's modem. Additional information can be found in Section 24, and in Appendix A at the back of this manual.

5.6.1 OUTPUT LEVEL CONTROL

There is a 21-turn potentiometer on the front of the RFL 93B MO Modem Module. This allows the transmit level to be adjusted. The transmitter output will be about +8 dBm when the potentiometer is fully clockwise, and about –20 dBm when it is fully counterclockwise.

5.6.2 MODEM I/O CONNECTIONS

Connections are made to the RFL 93B MO Modem Module through the 93 LC I/O Line Coupling Input/Output Module, which is directly behind the RFL 93B MO module. Shielded twisted pairs should be used when making connections between the 93 LC I/O and the telephone line.

Although the transformers in the RFL 93 LC I/O module are rated for 3750 Vac of isolation, the shields of the twisted pairs should be connected to the ground stud on the back of the RFL 9300 as shown in Figure 5-3. At the phone line junction box, the shields should be connected to the ground bus. This will provide an equipment ground as well as capacitive shielding.

If there is a significant ground potential difference between the RFL 9300 and the phone line junction box, high currents may flow through the shields. This could cause thermal damage to the cables. To prevent damage, a heavy copper connection should be made in parallel with the shields to carry the current.

5.6.3 PHONE LINE COMMUNICATIONS

If you are using a Type 3002 unconditioned leased line for communications between RFL 9300 units, ask your local telephone company for a SPOA line (Service Performance Objective Class A). This will guarantee communications before, during, and after a fault condition. Your local telephone company should be able to provide more information on telephone lines and SPOA line protection, or you can contact the factory. For more information on SPOA Class A, see Appendix B.

WARNING

YOUR RFL 9300 TERMINAL MAY BE EQUIPPED WITH FIBER OPTIC INPUT/OUTPUT MODULES THAT HAVE FIBER OPTIC EMITTER HEADS. FIBER OPTIC EMITTER HEADS USE A LASER LIGHT SOURCE THAT PRODUCE INVISIBLE RADIATION. FIBER OPTIC COMMUNICATION SYSTEMS ARE INHERENTLY SAFE IN NORMAL OPERATION BECAUSE ALL RADIATION IS CONTAINED IN THE SYSTEM. IT IS POSSIBLE DURING MAINTENANCE TO EXPOSE THE RADIATION BY REMOVING OR BREAKING THE FIBER. STARING DIRECTLY INTO THE LIGHT BEAM MAY RESULT IN PERMANENT EYE DAMAGE AND/OR BLINDNESS. NEVER LOOK DIRECTLY INTO THE LIGHT BEAM AND BE CAREFUL NOT TO SHINE THE LIGHT AGAINST ANY REFLECTIVE SURFACE.

THE LASER SOURCE IS A CLASS I LASER PRODUCT WHICH COMPLIES WITH APPLICABLE FDA, OSHA AND ANSI STANDARDS.

5.7 FIBER OPTIC CONNECTIONS

If your RFL 9300 is equipped with fiber optic modules, fiber optic pigtails must be connected to the fiber optic I/O modules at the rear of the chassis. Amphenol 906 Series fiber optic connectors (or their equivalent) are used with multimode fibers; Type ST connectors are used with singlemode fibers. The exact connector used will depend upon the fiber optic I/O modules that are installed in the RFL 9300, and the specific optic cable being used.

When connecting the fiber optic pigtails, make sure the connectors are properly aligned before tightening, and then fully tighten them. This will help minimize losses in the connector.

5.8 DIRECT DIGITAL CONNECTIONS

RFL 9300's equipped with one or more RFL 93 DD Direct Digital I/O Modules require shielded cables with a metallic DC-37 connector shell (37-pin D-subminiature). The shield ground (chassis ground) should be connected on both the RFL 9300 and on the digital communications equipment (DCE). A solid ground bus connection must be provided at the RFL 9300 and the DCE **that is independent of the shield ground connection**. High ground currents could damage the shield or disturb communications if a bus ground is not provided. The RFL 9300 and the DCE must be close to each other and on the ground mat; isolation must be established in the DCE-to-DCE interface. The cable should be of a multi-pair type rated for RS-422 communication, and must have both a foil and braided ground shield. The braided ground must connect to the metal case of the DC-37 connector and the chassis bus ground. An example of this type of cable is Belden Type 8165; this cable provides an overall shield plus a shield on each individual pair.

Pin assignments for the DC-37 connector are shown in Table 5-1.

5.9 IRIG-B CLOCK CONNECTIONS

IRIG-B signals are used to synchronize the internal real time clock of the RFL 9300 so that alarm events and trip events can be accurately time stamped. The IRIG-B clock source is connected to the rear panel of the RFL 9300. The IRIG-B signal enters the 9300 via a BNC connector on the Relay I/O module as shown in Figure 5-3.

Table 5-1. Pin assignment for DC-37 connector on RFL 93 DD I/O Direct Digital I/O Module

Pin No.	Signal Name	Description
1	SHLDGND	Shell ground (chassis ground)
19	GND	Signal ground
25	GND	Signal ground
7	+5V	+5-volt signal
4	SD A	TX DATA output + (RS-422)
22	SD B	TX DATA output -
5	ST A	SEND TIMING input + (RS-422)
23	ST B	SEND TIMING input -
6	RD A	RX DATA input + (RS-422)
24	RD B	RX DATA input -
8	RT A	RECEIVE TIMING input + (RS-422)
26	RT B	RECEIVE TIMING input -
33	/ALARM	EXTERNAL ALARM input (logic - level). Pull-up to +5V to drive alarm; low to signal ground

SECTION 6: FAMILIARIZATION

6.1 INTRODUCTION

The information in this section will familiarize you with how the RFL 9300 Charge Comparison System operates. All controls and indicators are shown and described. A basic start-up procedure appears in this section, and procedures are included for each of the RFL 9300's four display modes (STANDBY, READ, STARTUP and PROGRAM). Information is also given on accessing the RFL 9300 through its RS-232 interface.

Each of the modules listed below has a software version associated with it.

Parameter No.	Display	Module
103	SWID CC1	93B CC
104	SWID CC2	93B CC (1)
105	SWID SV	93B SV
106	SWID PCA	93B PC (Phase A)
107	SWID PCB	93B PC (Phase B)
108	SWID PCC	93B PC (Phase C)
109	SWID PCG	93B PC ($3I_0$)
110	SWID DC	93B DISPLAY

(1) This module is only present in RFL 9300s set up for use on three-terminal lines.

Use the READ screen on the RFL 9300 front panel (described later in this section), to determine the software versions that are in your equipment. These software versions reflect the latest software that was in effect at the time the unit was shipped.

6.2 CONTROLS AND INDICATORS

The front panel of the RFL 9300 contains controls and indicators which are used to prepare the RFL 9300 for use, and to monitor system functions. These controls and indicators are shown in Figure 6-1, and are described in Table 6-1. The RFL 9300 keypad is shown in Figure 6-2, and the functions of these keys are described in Table 6-2. Table 6-3 contains general information on the RFL 9300 modules and Figure 6-3 shows the locations of the modules in the RFL 9300 chassis.

6.3 START-UP PROCEDURES

6.3.1 START-UP PROCEDURE FOR A TWO-TERMINAL INSTALLATION

The following procedure is used to start up two RFL 9300 relays. They can either be installed at both ends of a protected line, or the units can be located side-by-side in a laboratory.

NOTE

It is possible to start up a single RFL 9300 that is communicating with itself (with its transmitter connected to its own receiver). This procedure is described in Section 8 of this manual.

The addressing feature can be disabled by setting the local and remote addresses to “0000”. See paragraph 6.6 for more information.

>> Text continues on page 6-7 <<

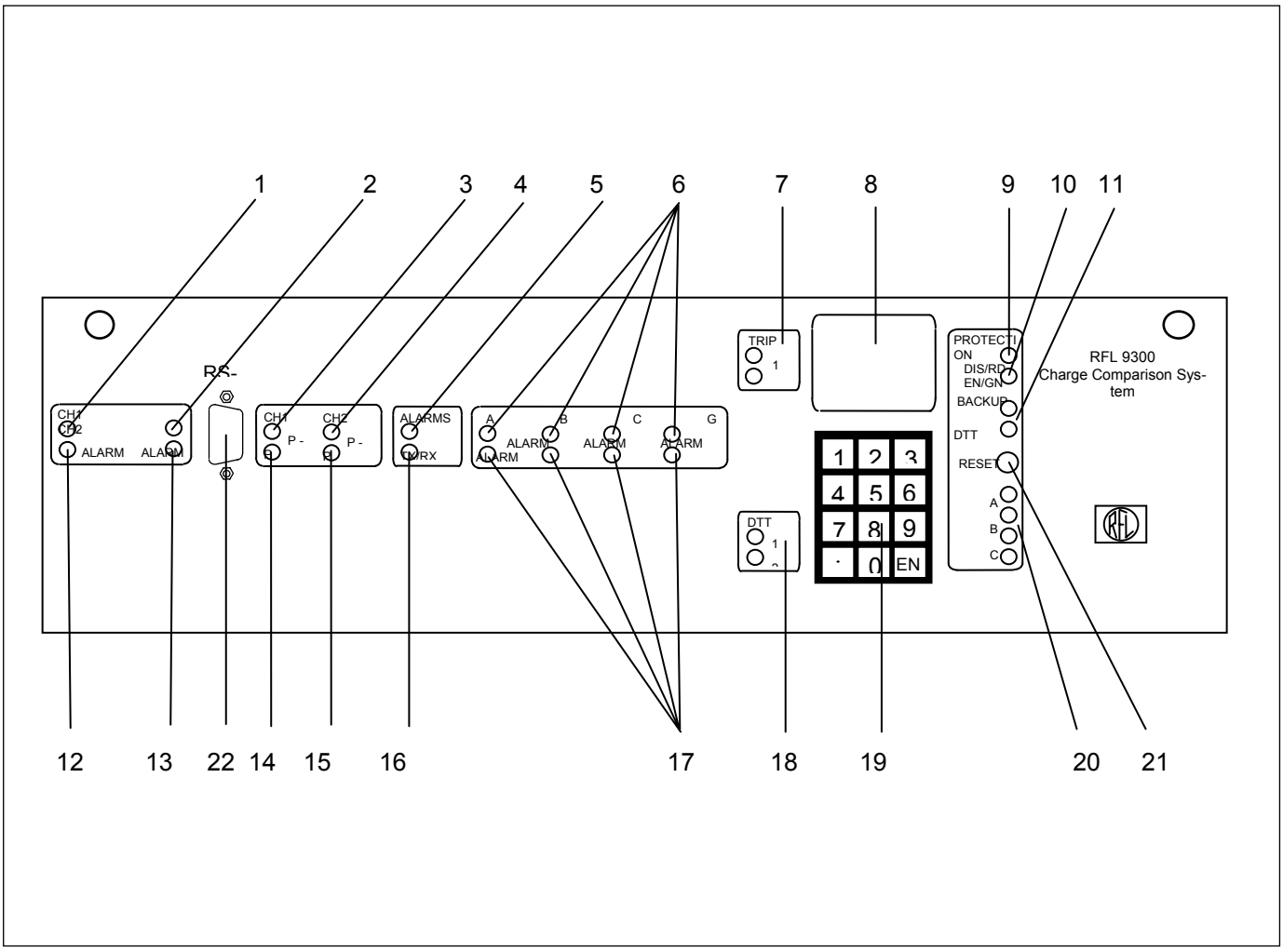


Figure 6-1. Controls and indicators, typical three-terminal RFL 9300 Charge Comparison System

Table 6-1. Controls and indicators, typical three-terminal RFL 9300 Charge Comparison System

Item	Description or Marking	Function
1	CH1 ALARM indicator	Lights when there is a failure in CH1 communication
2	CH2 ALARM indicator	Lights when there is a failure in CH2 communication
3	CH1 P-P indicator	Lights when a Channel 1 ping-pong test (round-trip delay measurement) is successful.
4	CH2 P-P indicator	Lights when a Channel 2 ping-pong test (round-trip delay measurement) is successful.
5	TX/RX ALARM indicator	Lights when a communications failure is detected.
6	ALARM indicators	Lights when a problem is detected in a specific phase controller module.
7	TRIP relay target indicators	Light when the CCS TRIP relay contacts are carrying dc trip currents of at least 0.2 ampere (STD.). These indicators are latched in non-volatile memory, and can only be reset by pressing the RES button. (Can also be reset through APRIL)
8	Alphanumeric display	Indicates operating status, parameter values, and alarm codes. The display contains 16 alphanumeric LED readouts, arranged in two eight-character lines. The top line displays either the mode or the selected operating parameters within each mode. The bottom line displays additional information about the mode or parameter appearing on the top line.
9	PROTECTION indicator	Lights green when protection is enabled; turns red when trip function outputs are disabled.
10	BACKUP indicator	Lights red when RFL 9300 backup is active.
11	DTT targets	Indicate direct transfer trip status: TX:Lights when DTT command is sent to remote unit. RX:Lights when DTT command is received from remote unit. These indicators are latched in non-volatile memory, and can only be reset by pressing the RESET button. (Can also be reset through APRIL)
12	CH1 TX ON indicator	Lights when the CH1 transmitter is functioning
13	CH2 TX ON indicator	Lights when the CH2 transmitter is functioning
14	CH1 BER indicator	Lights when the CH1 bit error rate (BER) is within limits.
15	CH2 BER indicator	Lights when the CH2 bit error rate (BER) is within limits. (Three-terminal systems only)
16	SYS ALARM indicator	Lights when a system problem not involving communications is detected.
17	FD indicators	Lights when fault detector for that phase produces an output.
18	DTT target indicators	Light when the DTT trip circuit carries dc currents of at least 0.1 ampere. These indicators are latched in non-volatile memory, and can only be reset by pressing the RESET button. (Can also be reset through APRIL)
19	Keypad	Used to enter security codes, parameter numbers and select parameter values. (See Figure 6-2 and Table 6-2 for more information on keypad functions.) If the RFL 9300 is in the PROGRAM mode or READ mode and the keypad is not used for 15 minutes, the RFL 9300 will automatically return to STANDBY mode.
20	TRIP indicators	Light to indicate the phase controller has issued a trip signal: A: Phase A trip. B: Phase B trip. C: Phase C trip. G: Ground ($3I_0$) trip. These indicators are latched in non-volatile memory, and can only be reset by pressing the RESET button. (Can also be reset through APRIL)
21	RESET button	Used to manually reset alarms. When this switch is pressed, all indicators on the display module (except PROTECTION and BACKUP) will light for three seconds to test their function before they are reset. After the indicators on the RFL 93B DISPLAY module go off, indicators 5, 6, 7 & 16 will light. If the RESET switch is pressed while the RFL 9300 is in the READ or PROGRAM mode, the RFL 9300 will return to the STANDBY mode. If the 9300 trip outputs are closed and the RESET button is pressed, “TRIP ACTIVE” will appear on the display.
22	RS-232 connector	Allows a user to connect a PC to access the RFL 9300. See paragraph 6.5 for more information

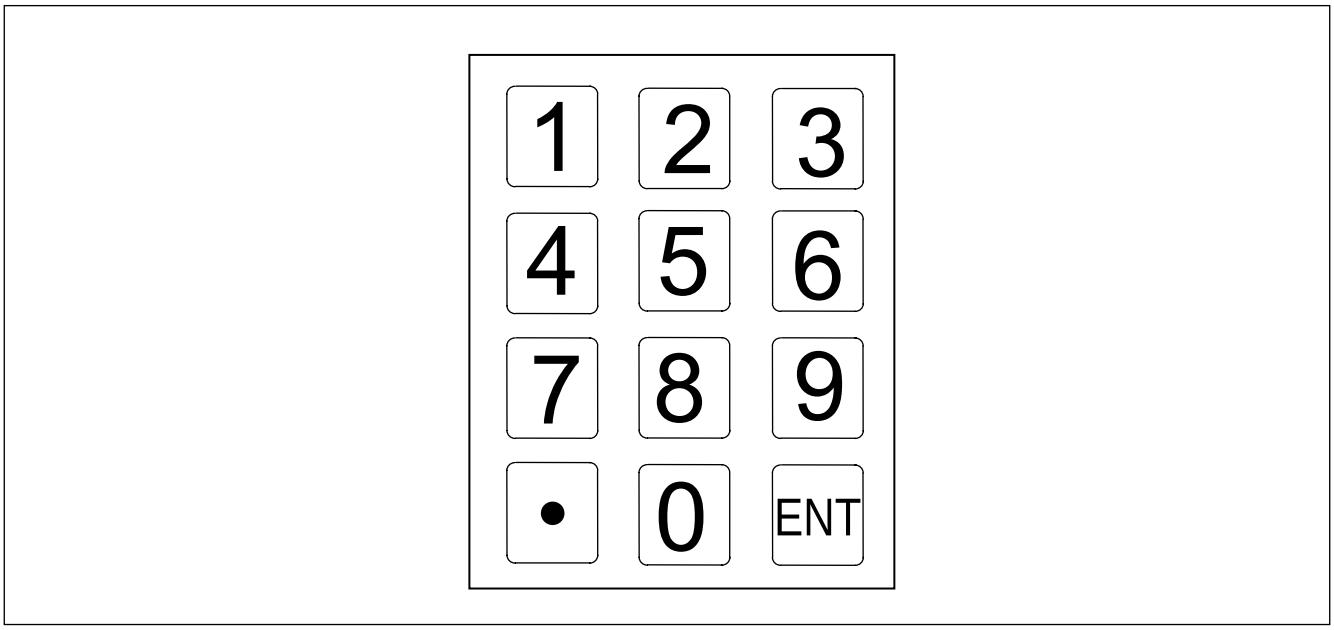


Figure 6-2. The RFL 9300 keypad

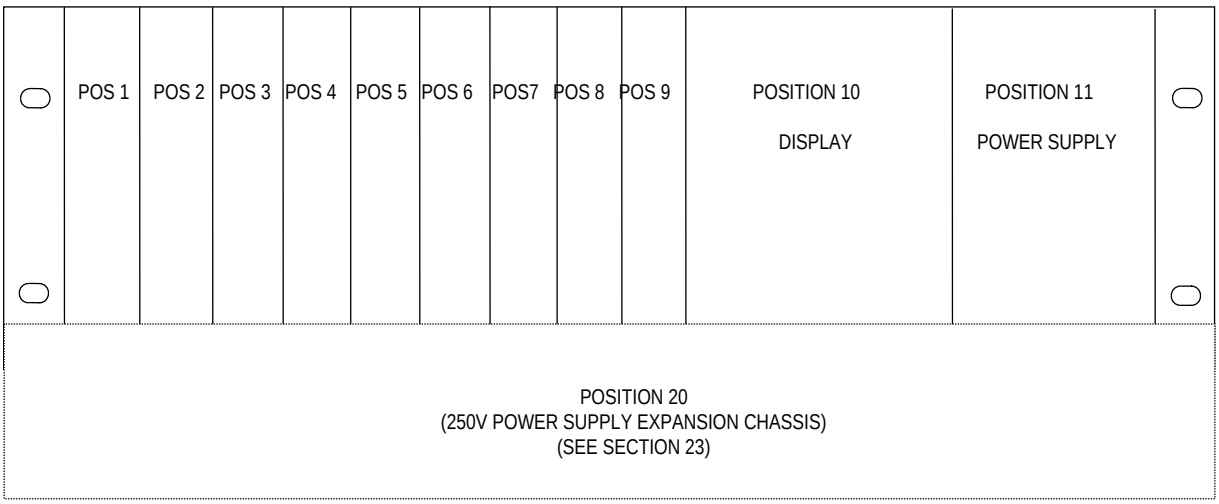
Table 6-2. Keypad functions, RFL 9300 Charge Comparison System

Key Marking	Function
[1] through **[9]**, **[0]**	Used to enter the security codes required to enter or exit some RFL 9300 display modes. Also used to enter t parameter numbers listed in Tables 6-5 or 6-6 (as applicable).
[8] and **[0]**	When not activated for numeric entry, these keys are used to scroll between option selections for each mode parameter displayed on the bottom line of the display.
[9]	When not activated for numeric entry, used to move backwards through the display parameters; works opposite from the **[ENT]** key, which moves forward through the parameters. (Changes made to settings are only accepted when the **[ENT]** key is used.)
[.]	Activates the numeric functions of the **[0]** through **[9]** keys.
[ENT]	Used to scroll between display modes. Once you have entered a display mode, the **[ENT]** key can be used to move from one display parameter to the next. The **[ENT]** key is also used to enter changes in these parameters.

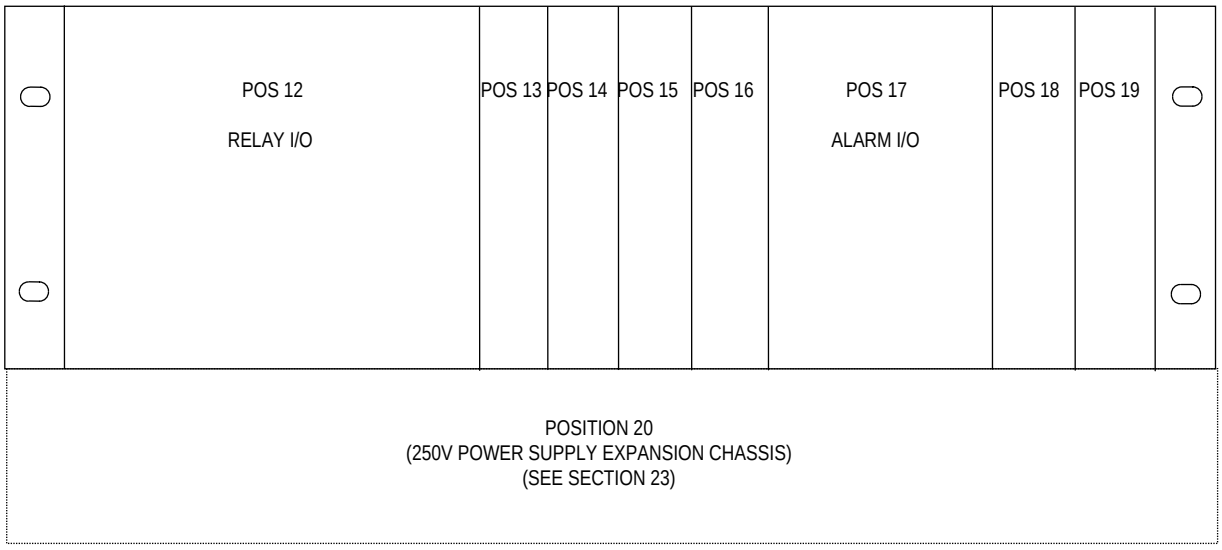
Table 6-3. RFL 9300 Module, General Information

Module Description	Model Number	Assembly Number	Module Position Numbers (See Figure 6-3)	Module location	Additional Information
Display Module	93B DISPLAY	106320 (HORIZ) 106320-1 (VERT)	10	Front	Section 9
Supervisor Controller Module	93B SV	106300-1	5	Front	Section 10
Auxiliary Current Transformer I/O Module	93B ACT I/O	106345-1, -5	13 - 16	Rear	Section 11
Phase Controller Module	93B PC	106370	6 thru 9	Front	Section 12
Communications Controller Module	93B CC (1)	106365	3	Front	Section 13
		BLANK	4	Front	
	93B CC (1)	106365	4	Front	
Modem Module	93B MO	106355	1 - 2	Front	Section 14
Line Coupler I/O Module	93 LC I/O	103835	18 - 19	Rear	Section 15
Direct Digital Interface I/O Module	93 DD I/O	103830-1	18 - 19	Rear	Section 16
Single Width Fiber Optic Transceiver Module (2)	93B FT/FR	106360	1 - 2	Front	Section 17
Single Width Fiber Optic I/O Modules	93 FT/FR I/O 8M 93 FT/FR I/O 13M 93 FT/FR I/O 13S 93 FT/FR I/O 13SL 93 FT/FR I/O 15SL	105850 105855 105860 105865 105870	18 - 19	Rear	Section 18
Power Supply Module	9300 PS 48/125 DC	106715-1	11	Front	Section 19
Relay I/O Module	93B RELAY I/O	106385	12	Rear	Section 20
Alarm I/O Module	93 ALARM I/O 93 ALARM I/O (24V)	104775-5 104775-6	17	Rear	Section 21
Short Haul Fiber Interface Module	93 SHFI	106340	18-19	Rear	Section 22
Fiber Service Unit	FSU 9V FSU 48V FSU 129V	105075-1 105075-2 105075-3	NA	External To Chassis	Section 22
G.703 Interface I/O Module	93 G.703	106730	18-19	Rear	Section 23
Single Pole Chassis	9300 SINGLE POLE TRIP	106700	NA	Below 9300 Chassis	Section 24
Chassis Assembly	9300B	105885	NA	NA	Section 25
Mother Board	93B INTER	105895	NA	Mounted inside Chassis Assembly	Section 25
RS-232 Front Panel Inter	RS-232	106775	NA	Behind Front Panel	Section 25
250V Power Supply Expansion Chassis	POWER CONV I/O 250VDC	105875	20	Mounted below Chassis Assembly	Section 26

1. Two-terminal installations use one 93B CC installed at each site in module position #3 with module position #4 blank. Three-terminal installations use two 93B CCs at each site, one installed in module position #3 and one installed in module position #4.
2. In a two-terminal system the transceiver in position 1 corresponds to the 93B CC in position 3. In a three-terminal system the transceiver in position 2 corresponds to the 93B CC module in position 4. In a two-terminal system with hot-standby, transceivers in positions 1 and 2 correspond to the 93B CC in position 3.



FRONT VIEW OF RFL 9300 WITH FRONT PANEL TILTED DOWN



REAR VIEW OF RFL 9300

Figure 6-3. RFL 9300 module position numbers

>>> Text continued from page 6-1 <<<

NOTE

The waiting times listed in the following procedure are for RFL 9300s equipped with modems. Some of these waiting times will be much shorter for units equipped with direct digital or fiber optic modules.

Perform all steps in the following procedure in the order presented.

1. Verify that all rear panel wiring was done according to the diagrams and information in Section 5 of this manual. If the RFL 9300 is equipped with fiber optic modules, make sure the fibers are also properly connected.

2. Establish voice communications with the operator at the remote terminal.

3. Verify that all system configuration jumpers on the Supervisor Module (93A SV) are in the correct positions as applicable (50 HZ or 60 HZ, Two-terminal, 1A or 5A, Single-pole or Three-pole tripping).

4. Turn on the **local** RFL 9300 by placing the POWER switch on the power supply module to the ON (up) position, and observe the following:

   a. All three indicators on the front of the power supply will light, indicating that the power supply is functioning normally. The words "Please Wait" will appear on the display. Red alarm indicators on the 93A SV and 93A PC modules will light, and the beeper will sound.

   b. The beeper can be shut off by disabling parameter #44 if desired (audio beeper enable/disable) by using the PROGRAM mode, as described in para. 6.4.4 later in this section.

   c. A green light will illuminate on the display controller (EN/GN = enable/green). This means that trip is enabled.

   d. After a few seconds, the word "ALARM" will flash on the top line of the display, and typically the numbers "16" , “34 or 35” and "46" will appear on the bottom line. The numbers may be different due to factory test settings. (A complete list of alarm codes appears in Table 6-4 of this section.)

   e. The local RFL 9300 will remain in this state as long as the remote RFL 9300 is turned off.

5. Program the **local** RFL 9300 transmit address as follows:

   a. On the display module keypad press the ENT key three times to get into the PROGRAM/DISABLE screen.

   b. Press the 8 key to get into the PROGRAM/ENABLE screen.

   c. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

   d. Press .248 ENT. This will get you into the PH BIAS screen in programming mode.

   e. Go to the XMT ADD1 screen by doing one of the following:

- Press the ENT key repeatedly until you get to the XMT ADD1 screen.
- Hold the ENT key down to scroll to the XMT ADD1 screen.
- Enter .46 ENT to get to the XMT ADD1 screen.

f. Press 8 to scroll up, or press 0 to scroll down to the desired transmit address for the local RFL 9300. Holding the key down will accelerate the rate at which the numbers change. After about 5 seconds the numbers will scroll by 100's. If you press 9 it will cancel the current setting and go back to the previous setting. The transmit address is user selectable from 0016 to 4079. This address gets transmitted to the corresponding remote unit for address verification.The sum of the local and remote addresses must equal 4095. For example, if the local unit transmit address is set to 4000, then the remote unit transmit address must be set to 0095.

g. For this procedure set the transmit address of the local RFL 9300 to 4000. Then press the ENT key.

h. To exit the programming mode press .0 ENT. This will get you to the EXIT screen. If the screen reads EXIT/DISABLE press the 8 key to get into the EXIT/ENABLE screen.

i. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

j. Press .248 ENT.

k. The word ALARM will still be displayed at the top line of the display, and typically the numbers "16" , "34 or 35" and "46" will still appear on the bottom line. This is because the remote RFL 9300 still has power OFF, and its transmit address has not been programmed. The numbers may be different due to factory test settings. (A complete list of alarm codes appears in Table 6-4 of this Section).

l. This completes the programming of the local unit transmit address.

6. Turn on the **remote** RFL 9300 by placing the POWER switch on the power supply module to the ON (up) position, and observe the following:

a. All three indicators on the front of the power supply will light, indicating that the power supply is functioning normally. The words "Please Wait" will appear on the display. Red alarm indicators on the 93A SV and 93A PC modules will light, and the beeper will sound.

b. The beeper can be shut off by disabling parameter #44 if desired (audio beeper enable/disable) by using the PROGRAM mode, as described in para. 6.4.4 later in this section.

c. A green light will illuminate on the display controller (EN/GN = enable/green). This means that trip is enabled.

d. After a few seconds, the word "ALARM" will flash on the top line of the display, and typically the number "16", will appear on the bottom line. The numbers may be different due to factory test settings. (A complete list of alarm codes appears in Table 6-4 of this section.)

e. The remote RFL 9300 will remain in this state as long as its transmit address has not been programmed.

7. Program the **remote** RFL 9300 transmit address as follows:

a. On the display module keypad press the ENT key three times to get into the PROGRAM/DISABLE screen. All red lights will go out on the display, supervisor and phase controllers.

b. Press the 8 key to get into the PROGRAM/ENABLE screen.

c. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

d. Press .248 ENT. This will get you into the PH BIAS screen in programming mode.

e. Go to the XMT ADD1 screen by doing one of the following:

- Press the ENT key repeatedly until you get to the XMT ADD1 screen.

- Hold the ENT key down to scroll to the XMT ADD1 screen.

- Enter .46 ENT to get to the XMT ADD1 screen.

f. Press 8 to scroll up, or press 0 to scroll down to the desired transmit address for the remote RFL 9300. Holding the key down will accelerate the rate at which the numbers change. After about 5 seconds the numbers will scroll by 100's. If you press 9 it will cancel the current setting and go back to the previous setting. The transmit address is user selectable from 0016 to 4079. This address gets transmitted to the corresponding local unit for address verification. The sum of the local and remote addresses must equal 4095. For example, if the local unit transmit address is set to 4000, then the remote unit transmit address must be set to 0095.

g. For this procedure set the transmit address of the remote RFL 9300 to 0095. Then press the ENT key. At this point the relay should go on-line.

h. To exit the programming mode press .0 ENT. This will get you to the EXIT screen. If the screen reads EXIT/DISABLE press the 8 key to get into the EXIT/ENABLE screen.

i. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

j. Press .248 ENT.

k. This completes the programming of the remote unit transmit address.

l. If you have programmed the local and remote transmit addresses correctly, both the local and remote RFL 9300 front panels will display the following:

- All red lights will be out on the display controller and supervisor.

- The audible alarm will be extinguished.

- A green light will illuminate on the display controller. (EN/GN = enable green) This means that trip is enabled.

- The messages on the display will be replaced with a series of dots that move across both lines of the display from left to right.

m. The RFL 9300's at both the local and remote locations are communicating with each other and are in a normal quiescent condition.

The system is now in a normal state, with the RFL 9300 units at both ends of the protected line up and running.

6.3.2 START-UP PROCEDURE FOR A THREE-TERMINAL INSTALLATION

The following procedure is used to start up an RFL 9300 three-terminal installation. One RFL 9300 can be installed at each terminal end of a three-terminal line, or three units can be located side-by-side in a laboratory. The terminals are referred to as local, remote 1 and remote 2.

NOTES

It is possible to start up a single RFL 9300 that is communicating with itself (with its transmitter connected to its own receiver). This procedure is described in Section 8 of this manual.

As an option a three-terminal installation can have the addressing feature disabled by setting the local, remote 1 and remote 2 addresses to “0000”. See paragraph 6.6 for more information.

The waiting times listed in the following procedure are for RFL 9300s equipped with modems. Some of these waiting times will be much shorter for units equipped with direct digital or fiber optic modules.

The terms “local”, “remote 1” and “remote 2” are only relative to the location of the operator. The location of the operator is defined as the “local” terminal.

Perform all steps in the following procedure in the order presented.

1. Verify that all rear panel wiring was done according to the diagrams and information in Section 5 of this manual. If the RFL 9300 is equipped with fiber optic modules, make sure the fibers are also properly connected.

2. Establish voice communications between the local terminal and the remote 1 terminal, and between the local terminal and the remote 2 terminal.

3. Verify that the system configuration jumpers on each of the three Supervisor Modules (93A SV) are set to the desired positions as applicable (1A or 5A, 50 HZ or 60 HZ, and 3T). The configuration jumpers can be viewed by the user by unscrewing the two captive thumbscrews on the RFL 9300 front panel and then lowering the panel to its full opened position. The Supervisor module is the fifth module from the left. More information on the Supervisor Module is provided in Section 10.

4. The POWER switch is located on the power supply module on the front right side of the RFL 9300 chassis. Open the front panel as described in step 3 to gain access to the POWER switch. Turn on the **local** RFL 9300 by placing the POWER switch on the power supply module to the ON (up) position, and observe the following:

    a. All three indicators on the front of the power supply will light, indicating that the power supply is functioning normally. The words "Please Wait" will appear on the display. Red alarm indicators on the 93A SV and 93A PC modules will light, and the beeper will sound. The front panel can now be closed.

    b. The beeper can be shut off, if desired, by entering the PROGRAM mode and disabling parameter #44 (audio beeper enable/disable) as described in para. 6.4.4.

    c. A green light will illuminate on the display controller (EN/GN = enable/green). This means that trip is enabled.

    d. After a few seconds, the word "ALARM" will flash on the top line of the display, and typically the numbers "16 or 17", “34 or 35” and "46" will appear on the bottom line. The numbers may be different due to factory test settings. (A complete list of alarm codes appears in Table 6-4 of this section.)

    e. The local RFL 9300 will remain in this state as long as the remote 1 and remote 2 terminals are turned OFF, and as long as the local terminal, and remote 1 and remote 2 terminal addresses have not been programmed.

5. Program the **local** RFL 9300 transmit addresses as follows:

a. In three-terminal installations, two transmit addresses (Tx1 and Tx2) must be programmed at each terminal. This means that a total of six transmit addresses must be programmed in a three-terminal installation as shown in Figure 6-28.

b. On the display module keypad press the ENT key three times to get into the PROGRAM/DISABLE screen.

c. Press the 8 key to get into the PROGRAM/ENABLE screen.

d. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

e. Press .248 ENT. This will get you into the PH BIAS screen in programming mode.

f. Go to the XMT ADD1 screen by doing one of the following:

- Press the ENT key repeatedly until you get to the XMT ADD1 screen.

- Hold the ENT key down to scroll to the XMT ADD1 screen.

- Enter .46 ENT to get to the XMT ADD1 screen.

g. Press 8 to scroll up, or press 0 to scroll down to the desired transmit address for the local RFL 9300. Holding the key down will accelerate the rate at which the numbers change. After about 5 seconds the numbers will scroll by 100's. If you press 9 it will cancel the current setting and go back to the previous setting. The transmit address is user select-able from 0016 to 4079. This address gets transmitted to the corresponding remote unit for address verification. The sum of the transmit address of a given terminal, and the transmit address of its "mate" must equal 4095. For example, if the transmit address (Tx1) of the local unit is set to 4055, then the transmit address (Tx1) of the remote 1 unit must be set to 0040.)

h. For this procedure set the transmit address (Tx1) of the local RFL 9300 to 4055.

i. Then press the ENT key to get to the XMT ADD2 screen. Set the transmit address (Tx2) of the local RFL 9300 to 0050. Then press the ENT key. (See Figure 6-28A.)

j. To exit the programming mode press .0 ENT. This will get you to the EXIT screen. If the screen reads EXIT/DISABLE press the 8 key to get into the EXIT/ENABLE screen.

k. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

l. Press .248 ENT.

m. The word ALARM will still be displayed at the top line of the display, and typically the numbers "16 or 17", "34 or 35" and "46" will still appear on the bottom line. The numbers may be different due to factory test settings. (A complete list of alarm codes appears in Table 6-4 of this Section).

n. The local RFL 9300 will remain in this state as long as the remote 1 and remote 2 terminals are turned OFF, and as long as the remote 1 and remote 2 terminal addresses have not been programmed.

o. This completes the programming of the local unit transmit addresses (Tx1 and Tx2).

6. Turn on the **remote 1** RFL 9300 by placing the POWER switch on the power supply module to the ON (up) position, and observe the following:

   a. All three indicators on the front of the power supply will light, indicating that the power supply is functioning normally. The words "Please Wait" will appear on the display. Red alarm indicators on the 93A SV and 93A PC modules will light, and the beeper will sound.

   b. The beeper can be shut off, if desired, by entering the PROGRAM mode and disabling parameter #44 (audio beeper enable/disable) as described in paragraph 6.4.4.

   c. A green light will illuminate on the display controller (EN/GN = enable/green). This means that trip is enabled.

   d. After a few seconds, the word "ALARM" will flash on the top line of the display, and typically the numbers "16 or 17", “34 or 35” and "46" will appear on the bottom line. The numbers may be different due to factory test settings. (A complete list of alarm codes appears in Table 6-4 of this section.)

   e. The remote RFL 9300 will remain in this state as long as remote 2 is turned off, and as long as remote1 and remote 2 transmit addresses have not been programmed.

7. Program the **remote 1** RFL 9300 transmit address as follows:

   a. On the display module keypad press the ENT key three times to get into the PROGRAM/DISABLE screen.

   b. Press the 8 key to get into the PROGRAM/ENABLE screen.

   c. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

   d. Press .248 ENT. This will get you into the PH BIAS screen in programming mode.

   e. Go to the XMT ADD1 screen by doing one of the following:

      - Press the ENT key repeatedly until you get to the XMT ADD1 screen.

      - Hold the ENT key down to scroll to the XMT ADD1 screen.

      - Enter .46 ENT to get to the XMT ADD1 screen.

   f. Press 8 to scroll up, or press 0 to scroll down to the desired transmit address for the remote RFL 9300. Holding the key down will accelerate the rate at which the numbers change. After about 5 seconds the numbers will scroll by 100’s. If you press 9 it will cancel the current setting and go back to the previous setting. The transmit address is user selectable from 0016 to 4079. This address gets transmitted to the corresponding local unit for address verification. The sum of the local and remote addresses must equal 4095. For example, if the local unit transmit address was set to 4055, then the remote unit transmit address must be set to 0040.

   g. For this procedure set the transmit address (Tx1) of the remote 1 RFL 9300 to 0040.

   h. Then press the ENT key to get to the XMT ADD2 screen. Set the transmit address (Tx2) of the remote 1 RFL 9300 to 4025. Then press the ENT key. (See Figure 6-28A.)

   i. To exit the programming mode press .0 ENT. This will get you to the EXIT screen. If the screen reads EXIT/DISABLE press the 8 key to get into the EXIT/ENABLE screen.

   j. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

k. Press .248 ENT.

l. After a few seconds, the word "ALARM" will flash on the top line of the display, and typically the numbers "16 or 17", “34 or 35” and "46" will appear on the bottom line. The numbers may be different due to factory test settings. (A complete list of alarm codes appears in Table 6-4 of this section.)

m. This completes the programming of the remote 1 transmit addresses.

8. Turn on the **remote 2** RFL 9300 by placing the POWER switch on the power supply module to the ON (up) position, and observe the following:

a. All three indicators on the front of the power supply will light, indicating that the power supply is functioning normally. The words "Please Wait" will appear on the display. Red alarm indicators on the 93A SV and 93A PC modules will light, and the beeper will sound.

b. If the beeper is annoying, it can be shut off by disabling parameter #44 (audio beeper enable/disable) by using the PROGRAM mode, as described in para. 6.4.4 later in this section.

c. A green light will illuminate on the display controller (EN/GN = enable/green). This means that trip is enabled.

d. After a few seconds, the word "ALARM" will flash on the top line of the display, and typically the numbers "16" and "17" will appear on the bottom line. The numbers may be different due to factory test settings. (A complete list of alarm codes appears in Table 6-4 of this section.)

e. The remote RFL 9300 will remain in this state as long as remote 1 and remote 2 transmit addresses have not been programmed.

9. Program the **remote 2** RFL 9300 transmit address as follows:

a. On the display module keypad press the ENT key three times to get into the PROGRAM/DISABLE screen.

b. Press the 8 key to get into the PROGRAM/ENABLE screen.

c. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

d. Press .248 ENT. This will get you into the PH BIAS screen in programming mode.

e. Go to the XMT ADD1 screen by doing one of the following:

- Press the ENT key repeatedly until you get to the XMT ADD1 screen.

- Hold the ENT key down to scroll to the XMT ADD1 screen.

- Enter .46 ENT to get to the XMT ADD1 screen.

f. Press 8 to scroll up, or press 0 to scroll down to the desired transmit address for the remote RFL 9300. Holding the key down will accelerate the rate at which the numbers change. After about 5 seconds the numbers will scroll by 100’s. If you press 9 it will cancel the current setting and go back to the previous setting. The transmit address is user selectable from 0016 to 4079. This address gets transmitted to the corresponding local unit for address verification. The sum of the local and remote addresses must equal 4095. For example, if the local unit transmit address is set to 4000, then the remote unit transmit address must be set to 0095.

g. For this procedure set the transmit address (Tx1) of the remote 2 RFL 9300 to 4045.

h. Then press the ENT key to get to the XMT ADD2 screen. Set the transmit address (Tx2) of the remote 2 RFL 9300 to 0070. Then press the ENT key. (See Figure 6-28A). At this point all relays should go on-line.

i. To exit the programming mode press .0 ENT. This will get you to the EXIT screen. If the screen reads EXIT/DISABLE press the 8 key to get into the EXIT/ENABLE screen.

j. Press the ENT key to enter the SEC CODE screen. (The 9300 is asking the operator for the security code)

k. Press .248 ENT.

l. This completes the programming of the remote 2 unit transmit address.

m. If you have programmed the local , remote 1 and remote 2 transmit addresses correctly, all three RFL 9300 front panels will display the following:

- All red lights will be out on the display controller and supervisor.

- The audible alarms will be extinguished.

- A green light will illuminate on the display controller. (EN/GN = enable green) This means that trip is enabled.

- The messages on the display will be replaced with a series of dots that move across both lines of the display from left to right.

n. All three RFL 9300's are communicating with each other and are in a normal quiescent condition.

The system is now in a normal state, with the RFL 9300 units at all three ends of the protected line up and running.

6.4 DISPLAY MODES

The RFL 9300 has four display modes:

STANDBY This is the RFL 9300's normal operating mode. The STANDBY mode is active whenever the RFL 9300 is not in any of the other modes.

READ The READ mode allows you to display all present parameter settings and readings. You move between parameters by pressing the **[ENT]** key and then the **[9]** key. This mode can be entered without a password.

STARTUP STARTUP mode allows you to display parameters required during Final Commissioning of the Relays. You can scroll through a list of parameters by using the **[ENT]** and **[9]** keys. This mode requires a password for entry and exit.

PROGRAM The PROGRAM mode allows you to change parameter settings. Once a programmable parameter is displayed, you can scroll through a list of its allowable settings by using the **[8]** and **[0]** keys. This mode requires a password for entry and exit. New parameter values are not accepted unless the **[ENT]** key is pressed when the selected value is displayed on the bottom line of the display.

For more information on the RFL 9300's display modes, refer to the following paragraphs in this manual:

STANDBY - para. 6.4.1
READ - para. 6.4.2
STARTUP - para. 6.4.3
PROGRAM - para. 6.4.4

6.4.1 THE STANDBY MODE

When the RFL 9300 is in the STANDBY mode, a pair of dots move across both lines of the display, from left to right if there is no alarm condition. If an alarm condition occurs, the word "ALARM" and one or more code numbers will appear on the display.

The RFL 9300 senses 28 different conditions that will cause an alarm. If one of these conditions exists, the word "ALARM" and a code number will appear on the display. If the beeper is enabled, it will sound intermittently. A list of alarm codes appears in Table 6-4. Note that several of these codes are reserved for future use, two of the codes (17 and 47) are not present in two-terminal systems, and that four codes (54-57) are only present in single-pole systems.

Table 6-4. Alarm codes for Two-Terminal and Three-Terminal RFL 9300 Charge Comparison System

Code	Condition
10	Local Display Controller Alarm: 9 seconds has elapsed without supervisor communications.
12	Local Display Controller Alarm: No acknowledgment from Supervisor Module in 200 ms.
13	Local Display Controller Alarm: Three non-acknowledgments (NAKs) from Supervisor Module.
14	Oscillography Controller Alarm: Display controller has lost communication with Oscillography Board.
15	Local Display Controller Alarm: Non-volatile RAM failure on Display Controller.
16	Transmit Address 1: Verification of Local and Remote addresses has failed.
17[(1)]	Transmit Address 2: Verification of Local and Remote addresses has failed.
20	Reserved for future use.
21	Reserved for future use.
22	Reserved for future use.
23	Reserved for future use.
24	Display Controller Trip Alarm: DTT dc trip current sensed for more than 500 ms.
25	Display Controller Trip Alarm: Current Sense circuit failure.
27	Display Controller Trip Alarm: DC trip current sensed for more than 500 ms.
30	Local Alarm From Supervisor Module: Local Charge Comparison Trip without fault detector - ground subsystem.
31	Local Alarm From Supervisor Module: Local Charge Comparison Trip without fault detector - Phase A.
32	Local Alarm From Supervisor Module: Local Charge Comparison Trip without fault detector - Phase B.
33	Local Alarm From Supervisor Module: Local Charge Comparison Trip without fault detector - Phase C.
34	Local Alarm From Supervisor Module: Parallel Port Alarm.
35	Local Alarm From Supervisor Module: Software Mismatch Alarm.
37	General Alarm: Remote #1 configuration mismatch.
40	Reserved for future use.
41	Reserved for future use.
42	Reserved for future use.
43	Reserved for future use.
44	Reserved for future use.
45	Local Alarm: Open conductor alarm.
46	General Alarm: System communications alarm.
47[(1)]	General Alarm: Remote #2 configuration mismatch
54[(2)]	Single-Pole Logic: General Alarm
55[(2)]	Single-Pole Trip Alarm: Phase A DC trip current sensed for more than 500ms
56[(2)]	Single-Pole Trip Alarm: Phase B DC trip current sensed for more than 500ms
57[(2)]	Single-Pole Trip Alarm: Phase C DC trip current sensed for more than 500ms
60	Phase A Controller: General Alarm
61	Phase B Controller: General Alarm
62	Phase C Controller: General Alarm
63	3IO Controller: General Alarm

[(1)] These codes not present in Two-terminal systems.
[(2)] These alarms only present in single-pole systems.

Alarm codes beginning with a "1" mean that a failure has been detected in the RFL 93A DISPLAY module. Codes beginning with a "2" mean that a failure has been detected in the trip relays' current sensors.

NOTE

Whenever the RESET switch is pressed, the LED indicators are tested as explained in Table 6-1 (Item 19). If you press the RESET switch, wait at least ten seconds before pressing it again; the RFL 9300 will not respond to the second press if you do not wait long enough.

Alarm codes beginning with a "3", "4" or “6” point out conditions detected in other modules in the RFL 9300. Alarm codes beginning with a “5” point out conditions detected in the RFL 9300 Single-Pole chassis. The alarms can only be cleared when the condition causing the alarm has returned to normal.

When all alarms are cleared, the display will return to the moving dot pattern, and the beeper will stop sounding.

6.4.2 THE READ MODE

The READ mode lets you view ac current values, time measurements, and RFL 9300 parameter settings. You cannot change any parameter settings in the READ mode; if you want to change a setting, you will have to enter the PROGRAM mode as described in para. 6.4.4.

6.4.2.1 ENTERING THE READ MODE

To enter the READ mode from the STANDBY mode, proceed as follows:

1. Press the **[ENT]** key once.
   The word "READ" will appear on the top line of the display, and the word "DISABLE" will appear on the bottom line.

2. Press the **[8]** key once.
   The word "ENABLE" will appear on the bottom line of the display.

3. Press the **[ENT]** key once.
   The name of the first parameter ("PNGPNG1") will appear on the top line of the display, with the measured delay (in milliseconds) on the bottom line.

6.4.2.2 DISPLAYING PARAMETERS

During the READ mode, over 100 different parameters can appear on the RFL 9300's display. Table 6-5 is a list of all RFL 9300 parameter codes and their definitions for two-terminal systems, and Table 6-6 is a list of all RFL 9300 parameter codes and their definitions for three-terminal systems.

Parameter #s 1 - 19 These parameters describe time and current quantities, and alarm status at the local and remote units. The time quantities are measured and computed by the RFL 93A CC Communications Controller Modules. The current quantities are computed by the RFL 93A PC Phase Controller Modules. These measurements are sent to the RFL 93A DISPLAY Module by the RFL 93A SV Supervisor Module, and are updated once a second. These are read-only values, and cannot be programmed.

Parameter #s 20 - 52 These parameters are programmable values except for parameter #40 (stub-bus). Their present values or settings can be displayed while in the READ mode. Their values or settings can only be changed when the local unit is in the PROGRAM mode as described in para. 6.4.4 of this manual.

Parameter #s 48 - 49 These parameters control the hot standby communications channel. If your RFL 9300 terminals are installed with a hot standby communications channel, setting Parameter #48 to AUTO will allow the RFL 9300 to switch automatically between channels every 12 hours. If Parameter #48 is set to MAN, the hot standby communications channel will be selected by Parameter #49. The hot standby feature is not applicable in 3-terminal mode. Units must be configured for 2-terminal only and each unit must have dual communication channels. When hot standby is active the user may not change the active channel through APRIL.

Parameter #s 51 - 52 These parameters control the baud rate and handshaking protocol for the RFL 9300's RS-232 serial port. They must be set to match the equipment being connected to the RS-232 port (J1) on the rear-panel relay I/O module. "2400 baud" and "XON/XOFF" should work in most applications. (See table 6-5 for more information.

Parameter #s 53 - 77 These parameters are the remote 1 unit's programmable variables. None of these values can be changed at the local unit. These values and settings are sent to the RFL 93A DISPLAY module by the remote 1 terminal, and are updated once a second.

Parameter #s 76 and 101 These parameters are the ping-pong (round-trip delay), trip status alarms and CDC conditions that exist at the remote unit. These are read-only values, and cannot be programmed at the local RFL 9300.

Parameter #s 78 - 101 These parameters are the remote 2 unit's programmable variables. None of these values can be changed at the local unit. These values and settings are sent to the RFL 93A DISPLAY module by the remote 2 terminal, and are updated once a second.

Parameter #s 103 - 110 These parameters list the software version for each module in the local RFL 9300. These are read-only parameters that cannot be changed in the field.

Parameter #s 111 or 0 These parameters are the EXIT parameters. They are used to leave any of the RFL 9300's display modes and return to the STANDBY mode.

Parameter #s 140 - 141 These are the local relay's single-pole-trip parameters. Single-pole trip active/inactive is jumper selectable on the 93B SV card (J5). Selective pole relaying is a programmable parameter. (see 4.2.33)

Parameter # 145 Trip release codes for the local relay. (see 4.2.34)

Parameter #s 160 - 161 Single-pole trip parameters for the remote 1 relay.

Parameter # 165 Trip release code for the remote 1 relay.

Parameter #s 180 - 181 Single-pole trip parameters for the remote 2 relay.

Parameter # 185 Trip release code for the remote 2 relay.

There are two methods for displaying parameters once you are in the READ mode. The first method is to press and hold the **[ENT]** key to scroll automatically through the parameter list shown in Table 6-5 or 6-6 (as applicable). If you go too far, you can press the **[9]** key to scroll back through the parameter list.

The second method is to manually enter the parameter number listed in Table 6-5 or 6-6 (as applicable). For example, if you want to display the remote phase bias parameter, proceed as follows:

1. Press the **[.]** key to access the keypad.

2. Press the **[5]**, **[3]**, and **[ENT]** keys to select Parameter #53 ("R1 PH BS" - Remote 1 Phase Bias).
   The parameter name ("R1 PH BS") will appear on the top line of the display, with the bias setting listed on the bottom line.

3. If you would like to display the next parameter (Parameter #54, "R1 GD BS" - Remote 1 Ground Bias), press the **[ENT]** key.
   The parameter name ("R1 GD BS") will appear on the top line of the display, with the bias level listed on the bottom line.

>> Text continues on page 6-25 <<

Table 6-5. READ mode parameters for RFL 9300 Two-Terminal Charge Comparison Systems

No.	Display	Definition
...	Moving dots	RFL 9300 is in STANDBY mode. Display controller parameter; not user-selectable.
0	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE. (1)
1	PngPng 1	Value of ping-pong (round-trip delay) for remote 1.
3	CDC 1	One-way Rx delay for remote 1.
5	LOC IA	Local Phase A current.
6	LOC IB	Local Phase B current.
7	LOC IC	Local Phase C current.
8	LOC 3I0	Local 3I0 current.
9	REM1 IA	Remote 1 Phase A current.
10	REM1 IB	Remote 1 Phase B current.
11	REM1 IC	Remote 1 Phase C current.
12	REM1 3I0	Remote 1 3I0 current.
17	RCV ADD1	Remote 1 Rx address. (2)
19	ALARMS	Present alarm status (four alarms).
20	PH BIAS	Phase bias. Programmable; see table 6-9 for more information.
21	GND BIAS	Ground bias. Programmable; see table 6-9 for more information.
22	BIAS CTL	Bias control. Programmable; see table 6-9 for more information.
23	GND DLY	Enable/disable ground delay. Programmable; see table 6-9 for more information.
24	DLAY SEC	Bias control and ground delay time (in seconds). Programmable; see table 6-9 for more information.
25	FD PHASE	Local phase fault detector current. Programmable; see table 6-9 for more information.
26	FD GND	Local ground fault detector current. Programmable; see table 6-9 for more information.
27	BACKUP	System backup functions. Programmable; see table 6-9 for more information.
28	PH OC BU	Phase overcurrent backup. Programmable; see table 6-9 for more information.
29	G OC BU	Ground overcurrent backup. Programmable; see table 6-9 for more information.
30	PH TOC	Local phase time-overcurrent backup. Programmable; see table 6-9 for more information.
31	P PICKUP	Local phase time-overcurrent pickup value. Programmable; see table 6-9 for more information.
32	PH CURVE	Local phase time-overcurrent curve select value. Programmable; see table 6-9 for more information.
33	PH DIAL	Local phase time-overcurrent dial setting value. Programmable; see table 6-9 for more information.
34	GND TOC	Local ground time-overcurrent backup. Programmable; see table 6-9 for more information.
35	G PICKUP	Local ground time-overcurrent pickup value. Programmable; see table 6-9 for more information.
36	G CURVE	Local ground time-overcurrent curve select value. Programmable; see table 6-9 for more information.
37	GND DIAL	Local ground time-overcurrent dial setting value. Programmable; see table 6-9 for more information.
38	OVHD/UGD	Overhead or underground cable. Programmable; see table 6-9 for more information.
39	OPEN CON	Open conductor action. Programmable; see table 6-9 for more information. (7)
40	STUB BUS	Stub bus active/inactive.
41	CM ALM D	Communications alarm delay. Programmable; see table 6-9 for more information.
42	DC FILT	Enable/disable dc filter. Programmable; see table 6-9 for more information.
43	DEFAULT	Re-program to factory default values. Programmable; see table 6-9 for more information. (4)
44	BEEPER	Enable/disable audible beeper. Programmable; see table 6-9 for more information. (5)
45	DISPLAY	Adjust display intensity. Programmable; see table 6-9 for more information. (6)
46	XMT ADD1	Transmit address to remote 1. Programmable; see table 6-9 for more information.
48	COM MODE	Selects hot standby communications mode. Programmable; see table 6-9 for more information.

>> Table continues on next page <<

>> Refer to page 6-24 for notes <<

Table 6-5 continued. READ mode parameters for RFL 9300 Two-Terminal Charge Comparison Systems

49	ACT CHAN	Selects channel for hot standby communications. Programmable; see table 6-9 for more information.
50	G B4 TRP	Enable/disable guard before trip. Programmable; see table 6-9 for more information.
51	RS232 BD	Selects RS-232 baud rate. Programmable; see table 6-9 for more information.
52	RS232PR	Selects RS-232 handshaking protocol. Programmable; see table 6-9 for more information.
53	R1 PH BS	Remote 1 phase bias.
54	R1 GD BS	Remote 1 ground bias.
55	R1 BS CL	Remote 1 bias control.
56	R1 GD DY	Remote 1 ground delay action.
57	R1 DLY S	Remote 1 time delay.
58	R1 FD PH	Remote 1 fault detector phase current.
59	R1 FD GD	Remote 1 fault detector ground current.
60	R1 BCKUP	Remote 1 backup functions.
61	R1 PH OC	Remote 1 phase overcurrent backup.
62	R1 GD OC	Remote 1 ground overcurrent backup.
63	R1 P TOC	Remote 1 phase inverse time-overcurrent backup.
64	R1 PPKUP	Remote 1 phase inverse time-overcurrent pickup value.
65	R1 PCURV	Remote 1 phase inverse time-overcurrent curve select value.
66	R1 PDIAL	Remote 1 phase inverse time-overcurrent dial setting value.
67	R1 G TOC	Remote 1 ground inverse time-overcurrent backup.
68	R1 GPKUP	Remote 1 ground inverse time-overcurrent pickup value.
69	R1 GCURV	Remote 1 ground inverse time-overcurrent curve select value.
70	R1 GDIAL	Remote 1 ground inverse time-overcurrent dial setting value.
71	R1 OH/UG	Remote 1 overhead or underground.
72	R1 OP/CN	Remote 1 open conductor action. (7)
73	R1 STUB	Remote 1 stub bus action.
74	R1 DCFIL	Remote 1 dc filter.
75	R1 GD TP	Remote 1 guard before trip.
76	R1 PNGPG	Remote 1 ping-pong (round-trip delay).
77	R1 CDC	Remote 1 channel delay compensation.
103	SWID CC1	Software version number for local communications controller in two-terminal systems.
104	SWID CC2	Software version number for second local communications controller in three-terminal systems.
105	SWID SV	Software version number for local supervisor module.
106	SWID PCA	Software version number for local Phase Controller "A" module.
107	SWID PCB	Software version number for local Phase Controller "B" module.
108	SWID PCC	Software version number for local Phase Controller "C" module.
109	SWID PCG	Software version number for local Phase Controller "G" module.
110	SWID DC	Software version number for local display module.
111	EXIT	Exit to STANDBY mode. Same as parameter #0. (1)
140	SGL POLE	Single-Pole trip – active/inactive
141	SEL POLE	Enable/Disable Selective pole relaying – Programmable; see table 6-9 for more information (8)
145	TRIP RLS	Trip release codes – Programmable; see table 6-9 for more information
160	RS1 POLE	Remote 1 single-pole trip – active/inactive
161	R1 SEL P	Remote 1 Selective pole relaying
165	TRP RLS 1	Remote 1 Trip release codes

>> Refer to page 6-24 for notes <<

Table 6-6. READ mode parameters for RFL 9300 Three-Terminal Charge Comparison Systems

No.	Display	Definition
...	Moving dots	RFL 9300 is in STANDBY mode. Display controller parameter; not user-selectable.
0	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE. (1)
1	PngPng 1	Value of ping-pong (round-trip delay) for remote 1.
2	PngPng 2	Value of ping-pong (round-trip delay) for remote 2.
5	LOC IA	Local Phase A current.
6	LOC IB	Local Phase B current.
7	LOC IC	Local Phase C current.
8	LOC 3I0	Local 3I0 current.
9	REM1 IA	Remote 1 Phase A current.
10	REM1 IB	Remote 1 Phase B current.
11	REM1 IC	Remote 1 Phase C current.
12	REM1 3I0	Remote 1 3I0 current.
13	REM2 IA	Remote 2 Phase A current.
14	REM2 IB	Remote 2 Phase B current.
15	REM2 IC	Remote 2 Phase C current.
16	REM2 3I0	Remote 2 3I0 current.
17	RCV ADD1	Remote 1 Rx address. (2)
18	RCV ADD2	Remote 2 Rx address. (3)
19	ALARMS	Present alarm status (four alarms).
20	PH BIAS	Phase bias. Programmable; see table 6-10 for more information.
21	GND BIAS	Ground bias. Programmable; see table 6-10 for more information.
22	BIAS CTL	Bias control. Programmable; see table 6-10 for more information.
23	GND DLY	Enable/disable ground delay. Programmable; see table 6-10 for more information.
24	DLAY SEC	Bias control and ground delay time (in seconds). Programmable; see table 6-10 for more information.
25	FD PHASE	Local phase fault detector current. Programmable; see table 6-10 for more information.
26	FD GND	Local ground fault detector current. Programmable; see table 6-10 for more information.
27	BACKUP	System backup functions. Programmable; see table 6-10 for more information.
28	PH OC BU	Phase overcurrent backup. Programmable; see table 6-10 for more information.
29	G OC BU	Ground overcurrent backup. Programmable; see table 6-10 for more information.
30	P TOC	Phase inverse time-overcurrent backup. Programmable; see table 6-10 for more information.
31	PPKUP	Phase inverse time-overcurrent pickup value. Programmable; see table 6-10 for more information.
32	PCURV	Phase inverse time-overcurrent curve select value. Programmable; see table 6-10 for more information.
33	PDIAL	Phase inverse time-overcurrent dial setting value. Programmable; see table 6-10 for more information.
34	G TOC	Ground inverse time-overcurrent backup. Programmable; see table 6-10 for more information.
35	GPKUP	Ground inverse time-overcurrent pickup value. Programmable; see table 6-10 for more information.
36	GCURV	Ground inverse time-overcurrent curve select value. Programmable; see table 6-10 for more information.
37	GDIAL	Ground inverse time-overcurrent dial setting value. Programmable; see table 6-10 for more information.
38	OVHD/UGD	Overhead or underground cable. Programmable; see table 6-10 for more information.
39	OPEN CON	Open conductor action. Programmable; see table 6-10 for more information. (7)
40	STUB BUS	Stub bus active/inactive.

>> Table continues on next page <<

>> Refer to page 6-24 for notes <<

Table 6-6 continued. READ mode parameters for RFL 9300 Three-Terminal Charge Comparison Systems

41	CM ALM D	Communications alarm delay. Programmable; see table 6-10 for more information.
43	DEFAULT	Re-program to factory default values. Programmable; see table 6-10 for more information. (4)
44	BEEPER	Enable/disable audible beeper. Programmable; see table 6-10 for more information. (5)
45	DISPLAY	Adjust display intensity. Programmable; see table 6-10 for more information. (6)
46	XMT ADD1	Transmit address to remote 1. Programmable; see table 6-10 for more information.
47	XMT ADD2	Transmit address to remote 2. Programmable; see table 6-10 for more information.
50	G B4 TRP	Enable/disable guard before trip. Programmable; see table 6-10 for more information.
51	RS232 BD	Selects RS-232 baud rate. Programmable; see table 6-10 for more information.
52	RS232PR	Selects RS-232 handshaking protocol. Programmable; see table 6-10 for more information.
53	R1 PH BS	Remote 1 phase bias.
54	R1 GD BS	Remote 1 ground bias.
55	R1 BS CL	Remote 1 bias control.
56	R1 GD DY	Remote 1 ground delay action.
57	R1 DLY S	Remote 1 time delay.
58	R1 FD PH	Remote 1 fault detector phase current.
59	R1 FD GD	Remote 1 fault detector ground current.
60	R1 BCKUP	Remote 1 backup functions.
61	R1 PH OC	Remote 1 phase overcurrent backup.
62	R1 GD OC	Remote 1 ground overcurrent backup.
63	R1 P TOC	Remote 1 phase inverse time-overcurrent backup.
64	R1 PPKUP	Remote 1 phase inverse time-overcurrent pickup value.
65	R1 PCURV	Remote 1 phase inverse time-overcurrent curve select value.
66	R1 PDIAL	Remote 1 phase inverse time-overcurrent dial setting value.
67	R1 G TOC	Remote 1 ground inverse time-overcurrent backup.
68	R1 GPKUP	Remote 1 ground inverse time-overcurrent pickup value.
69	R1 GCURV	Remote 1 ground inverse time-overcurrent curve select value.
70	R1 GDIAL	Remote 1 ground inverse time-overcurrent dial setting value.
71	R1 OH/UG	Remote 1 overhead or underground.
72	R1 OP/CN	Remote 1 open conductor action. (7)
73	R1 STUB	Remote 1 stub bus action.
75	R1 GD TP	Remote 1 guard before trip.
76	R1 PNGPG	Remote 1 ping-pong (round-trip delay).
78	R2 PH BS	Remote 2 phase bias.
79	R2 GD BS	Remote 2 ground bias.
80	R2 BS CL	Remote 2 bias control.
81	R2 GD DY	Remote 2 ground delay action.
82	R2 DLY S	Remote 2 time delay.

>> Table continues on next page <<

>> Refer to page 6-24 for notes <<

Table 6-6 continued. READ mode parameters for RFL 9300 Three-Terminal Charge Comparison Systems

83	R2 FD PH	Remote 2 fault detector phase current.
84	R2 FD GD	Remote 2 fault detector ground current.
85	R2 BCKUP	Remote 2 backup functions.
86	R2 PH OC	Remote 2 phase overcurrent backup.
87	R2 GD OC	Remote 2 ground overcurrent backup.
88	R2 P TOC	Remote 2 phase inverse time-overcurrent backup.
89	R2 PPKUP	Remote 2 phase inverse time-overcurrent pickup value.
90	R2 PCURV	Remote 2 phase inverse time-overcurrent curve select value.
91	R2 PDIAL	Remote 2 phase inverse time-overcurrent dial setting value.
92	R2 G TOC	Remote 2 ground inverse time-overcurrent backup.
93	R2 GPKUP	Remote 2 ground inverse time-overcurrent pickup value.
94	R2 GCURV	Remote 2 ground inverse time-overcurrent curve select value.
95	R2 GDIAL	Remote 2 ground inverse time-overcurrent dial setting value.
96	R2 OH/UG	Remote 2 overhead or underground.
97	R2 OP/CN	Remote 2 open conductor action. (7)
98	R2 STUB	Remote 2 stub bus action.
100	R2 GD TP	Remote 2 guard before trip
101	R2 PNGPG	Remote 2 ping-pong (round-trip delay).
103	SWID CC1	Software version number for local communications controller in two-terminal systems.
104	SWID CC2	Software version number for second local communications controller in three-terminal systems.
105	SWID SV	Software version number for local supervisor module.
106	SWID PCA	Software version number for local Phase Controller "A" module.
107	SWID PCB	Software version number for local Phase Controller "B" module.
108	SWID PCC	Software version number for local Phase Controller "C" module.
109	SWID PCG	Software version number for local Phase Controller "G" module.
110	SWID DC	Software version number for local display module.
111	EXIT	Exit to STANDBY mode. Same as parameter #0. (1)
140	SGL POLE	Single-Pole trip – active/inactive
141	SEL POLE	Enable/Disable Selective pole relaying – Programmable; see table 6-9 for more information (8)
145	TRIP RLS	Trip release codes – Programmable; see table 6-9 for more information
160	RS1 POLE	Remote 1 single-pole trip – active/inactive
161	R1 SEL P	Remote 1 Selective pole relaying
165	TRP RLS 1	Remote 1 Trip release codes
180	RS2 POLE	Remote 2 single-pole trip – active/inactive
181	R2 SEL P	Remote 2 Selective pole relaying
185	TRP RLS 2	Remote 2 Trip release codes

>> Refer to page 6-24 for notes <<

Notes for Tables 6-5 and 6-6:

1. The EXIT parameter (Parameter #0 or #111) may be enabled or disabled from any of the two active modes (READ or PROGRAM). If enabled, press the **[ENT]** key to return the RFL 9300 to the STANDBY mode. (The PROGRAM mode requires a security code before returning to the STANDBY mode). If the EXIT parameter is disabled, pressing the **[ENT]** key will direct the RFL 9300 to move to the parameter.

2. When all terminals are programmed correctly, the display will indicate “ADDR OK” or the mismatching address of Remote 1.

3. When all terminals are programmed correctly, the display will indicate “ADDR OK” or the mismatching address of Remote 2.

4. When this parameter is enabled and the **[ENT]** key is pressed, the Display Controller requests that the PROGRAM mode security code (.248) be entered. Once it is, all programmable parameter values will be reset to the default values listed in Table 6-9 or 6-10 (as applicable) of this section. These are the values the parameters are set to before the RFL 9300 leaves the factory.

5. When this parameter is set to ENABLE, the audible beeper can be used to notify the operator if an alarm condition exists. During prolonged alarm conditions, the user may wish to disable the beeper until the condition is corrected. It is recommended that this parameter remain enabled. Alarms may not be noticed if the display is in the READ or PROGRAM mode, or if the RFL 9300 is not being manned and the user is depending on the beeper to indicate an alarm condition.

6. When this parameter is shown, the **[8]** and **[0]** keys can be used to increase or decrease the display intensity (or brightness). When the setting is changed, the bottom line of the display will change to the new intensity, while the top line unit remains constant as a reference. When the **[ENT]** key is pressed, both lines assume the new intensity setting.

7. Open Conductor - Parameter #s 39, 72 and 97 – not available when single-pole trip is active.

8. Selective Pole relaying - Parameter #s 141, 161 and 181 – not available unless single-pole trip is active.

6.4.2.3 EXITING THE READ MODE

To exit the READ mode, proceed as follows:

1. Press the **[.]** key, followed by the **[0]** and **[ENT]** keys.
   The word "EXIT" will appear on the top line of the display, and the word "DISABLE" will appear on the bottom line of the display.

2. Press the **[8]** key once.
   The word "ENABLE" will appear on the bottom line of the display.

3. Press the **[ENT]** key.
   The RFL 9300 will return to the STANDBY mode, and the display will return to the moving dot pattern.

6.4.3 THE STARTUP MODE

The Startup Mode is used during field commissioning of the relays and requires a password for entry and exit. The Startup Mode parameters are shown in Tables 6-7 and 6-8. Refer to paragraph 8.4 for detailed information on the Startup Mode. Refer to Section 8 for detailed information on field commissioning.

6.4.3.1 ENTERING THE STARTUP MODE

To enter the STARTUP Mode from the STANDBY mode, proceed as follows:

1. Press the **[ENT]** key two times.
   The word "STARTUP" will appear on the top line of the display, and the word "DISABLE" will appear on the bottom line.

2. Press the **[8]** key once.
   The word "ENABLE" will appear on the bottom line of the display.

3. Press the **[ENT]** key.
   The message "SEC CODE" will appear on the display. This means that you must enter a security code before the RFL 9300 will enter the STARTUP Mode. Press the [.], [1], [3],[5] and [ENT] keys as the required security code.

The relay should now be in startup mode and the display will show that the Phase Sequence Test has begun. The relay will indicate a system alarm.

6.4.3.2 DISPLAYING PARAMETERS

Shown below is the parameter number for each displayed value and a brief description of its meaning.

001 - Ping Pong R1	Ping-pong delay for remote 1. Equal to one-half the round-trip delay.
002 - Ping Pong R2	Ping-pong delay for remote 2. Equal to 1/2 the round-trip delay. (3 terminal only)
003 - Sequence Test	Phase Sequence Test.
004 - Diff Cur Test	Differential Current Test.
005 - Local I A	Local Phase A current.
006 - Local I B	Local Phase B current.
007 - Local I C	Local Phase C current.
008 - Local 3I0	Local $3I_0$ current.
009 - Remote #1 I A	Remote #1 Phase A current.
013 - Remote #2 I A	Remote #2 Phase A current. (3 terminal only)

Table 6-7. STARTUP mode parameters for RFL 9300 Two-Terminal Charge Comparison Systems

No.	Display	Definition
...	Moving dots	RFL 9300 is in STANDBY mode. Display controller parameter; not user-selectable.
0	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE. (1)
1	PngPng 1	Value of ping-pong (round-trip delay) for remote 1.
3	SEQ TEST	Phase Sequence Test.
4	DIFF CURR	Differential Current Test
5	LOC IA	Local Phase A current.
6	LOC IB	Local Phase B current.
7	LOC IC	Local Phase C current.
8	LOC 3I0	Local 3I0 current.
9	REM1 IA	Remote 1 Phase A current.
111	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE. (1)

Table 6-8. STARTUP mode parameters for RFL 9300 Three-Terminal Charge Comparison Systems

No.	Display	Definition
...	Moving dots	RFL 9300 is in STANDBY mode. Display controller parameter; not user-selectable.
0	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE. (1)
1	PngPng 1	Value of ping-pong (round-trip delay) for remote 1.
2	PngPng 2	Value of ping-pong (round-trip delay) for remote 2.
3	SEQ TEST	Phase Sequence Test.
4	DIFF CURR	Differential Current Test
5	LOC IA	Local Phase A current.
6	LOC IB	Local Phase B current.
7	LOC IC	Local Phase C current.
8	LOC 3I0	Local 3I0 current.
9	REM1 IA	Remote 1 Phase A current.
13	REM2 IA	Remote 2 Phase A current.
111	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE. (1)

Notes for Tables 6-7 and 6-8:

1. The EXIT parameter (Parameter #0 or #111) may be enabled or disabled from any of the two active modes (READ or PROGRAM). If enabled, press the **[ENT]** key to return the RFL 9300 to the STANDBY mode. (The PROGRAM mode requires a security code before returning to the STANDBY mode). If the EXIT parameter is disabled, pressing the **[ENT]** key will direct the RFL 9300 to move to the parameter.

6.4.3.3 EXITING THE STARTUP MODE

To exit the STARTUP Mode, proceed as follows:

1. Press the **[.]** key, followed by the **[0]** and **[ENT]** keys.
   The word "EXIT" will appear on the top line of the display, with the word "DISABLE" on the bottom line.

2. Press the **[8]** key once.
   The word "ENABLE" will appear on the bottom line of the display.

3. Press the **[ENT]** key.
   The message "SEC CODE" will appear on the display. This means that you must enter a security code before the RFL 9300 will exit the STARTUP Mode. Press the [.], [1], [3],[5] and [ENT] keys to enter the required security code.

The RFL 9300 will go through a sequence similar to a front panel button reset that will last for about six seconds. All the lamps will illuminate for a few seconds. Then the RFL 9300 will return to the STANDBY mode, and the display will return to the moving dot pattern. The security code in step 2 is required because exiting the STARTUP Mode re-enables the system trip functions, and should not be done casually.

6.4.4 THE PROGRAM MODE

The PROGRAM mode allows you to change parameter settings. Tables 6-9 and 6-10 list all programmable RFL 9300 parameters, along with their codes, definitions and limits. Table 6-9 is for two-terminal units and Table 6-10 is for three-terminal units. Once a programmable parameter is displayed, you can scroll through a list of its allowable settings by using the **[8]** and **[0]** keys. The PROGRAM mode requires a password for entry.

6.4.4.1 ENTERING THE PROGRAM MODE

To enter the PROGRAM mode from the STANDBY mode, proceed as follows:

1. Press the **[ENT]** key three times.
   The word "PROGRAM" will appear on the top line of the display, and the word "DISABLE" will appear on the bottom line.

2. Press the **[8]** key once.
   The word "ENABLE" will appear on the bottom line of the display.

3. Press the **[ENT]** key once.
   The message "SEC CODE" will appear on the display. This means that you must enter a security code before the RFL 9300 will enter the PROGRAM mode. Press the [.], [2], [4], [8], and [ENT] keys to enter the required security code.

   Once the proper security code is entered, the name of the first programmable parameter ("PH BIAS") will appear on the top line of the display. The stored bias value (in amperes) will appear on the bottom line.

Table 6-9. Programmable parameters, RFL 9300 Two-Terminal Charge Comparison System

No.	Display	Definition	Range	Step	Default
20	PH BIAS	Phase bias	1.0 to 8.0 A	0.5 A	8.0 A
21	GND BIAS	Ground bias	1.0 to 2.25 A	0.25 A	2.25 A
22	BIAS CTL	Bias control	ENABLE/DISABLE	. . .	ENABLE
23	GND DLY	Ground delay	ENABLE/DISABLE	. . .	ENABLE
24	DLAY SEC	Bias control and ground delay time	Bias: 50 to 1000 ms Ground: 50 ms to 30 s	50 ms Variable (1)	1000 ms 30 s
25	FD PHASE	Local phase fault detector current	6 or 8 A	. . .	8 A
26	FD GND	Local ground fault detector current	0.5 or 1.0 A	. . .	1.0 A
27	BACKUP	System backup functions	ENABLE/DISABLE (8)	. . .	DISABLE
28	PH OC BU	Phase overcurrent backup	6 to 31.875 A	0.125 A	31.875 A
29	G OC BU	Ground overcurrent backup	1 to 31 A	0.125 A	31 A
30	PH TOC	Phase inverse time-overcurrent enable/disable	ENABLE/DISABLE	. . .	DISABLE
31	P PICKUP	Phase inverse time-overcurrent pickup value	0.5 to 31.875 A	0.125 A	31.875 A
32	PH CURVE	Phase inverse time-overcurrent curve select	See note 6	. . .	USA 1
33	PH DIAL	Phase inverse time-overcurrent dial setting	See note 6	. . .	SET 15.0
34	GND TOC	Ground inverse time-overcurrent enable/disable	ENABLE/DISABLE	. . .	DISABLE
35	G PICKUP	Ground inverse time-overcurrent pickup value	0.5 to 31.0 A	0.125 A	31.0 A
36	G CURVE	Ground inverse time-overcurrent curve select	See note 7	. . .	USA 1
37	GND DIAL	Ground inverse time-overcurrent dial setting	See note 7	. . .	SET 15.0
38	OVHD/UGD	Overhead or underground cable	OVHD or UGD	. . .	UGD
39	OPEN CON	Open conductor action	ALARM or TRIP	. . .	ALARM (9)
41	CM ALM D	Communications alarm delay	ENABLE/DISABLE	. . .	ENABLE
42	DC FILT	Dc filter for tapped load applications	ENABLE/DISABLE	. . .	ENABLE
43	DEFAULT	Resets Parameter #'s 20 - 52 to default values	ENABLE/DISABLE	. . .	DISABLE (2)
44	BEEPER	Enable/disable audible beeper	ENABLE/DISABLE	. . .	ENABLE (3)
45	DISPLAY	Adjust display intensity	4 levels	. . .	Brightest (4)
46	XMIT ADD1	Select transmit address 1	16 to 4095	1	0000
48	COM MODE	Selects hot standby communications mode	AUTO/MAN	. . .	AUTO
49	ACT CHAN	Selects channel for hot standby communications	CH 1/CH 2	. . .	(5)
50	G B4 TRP	Guard before trip	ENABLE/DISABLE	. . .	ENABLE
51	RS232 BD	Selects RS-232 baud rate	1200, 2400, 9600	. . .	1200
52	RS232 PR	Selects RS-232 handshaking protocol	XON/XOFF or RTS/CTS	. . .	XON/XOFF
141	SEL POLE	Single-Pole trip method	ENABLE/DISABLE(10)	. . .	DISABLE
145	TRIP RLS	Selects mode of trip release	3 choices (11)	. . .	TRIP+100

>> Refer to page 6-29 for notes <<

Table 6-10. Programmable parameters, RFL 9300 Three-Terminal Charge Comparison System

No.	Display	Definition	Range	Step	Default
20	PH BIAS	Phase bias	1.0 to 8.0 A	0.5 A	8.0 A
21	GND BIAS	Ground bias	1.0 to 2.25 A	0.25 A	2.25 A
22	BIAS CTL	Bias control	ENABLE/DISABLE	. . .	ENABLE
23	GND DLY	Ground delay	ENABLE/DISABLE	. . .	ENABLE
24	DLAY SEC	Bias control and ground delay time	Bias: 50 to 1000 ms Ground: 50 ms to 30 s	50 ms Variable (1)	1000 ms 30 s
25	FD PHASE	Local phase fault detector current	6 or 8 A	. . .	8 A
26	FD GND	Local ground fault detector current	0.5 or 1.0 A	. . .	1.0 A
27	BACKUP	System backup functions	ENABLE/DISABLE (8)	. . .	DISABLE
28	PH OC BU	Phase overcurrent backup	6 to 31.875 A	0.125 A	31.875 A
29	G OC BU	Ground overcurrent backup	1 to 31 A	0.125 A	31 A
30	PH TOC	Phase inverse time-overcurrent enable/disable	ENABLE/DISABLE	. . .	DISABLE
31	P PICKUP	Phase inverse time-overcurrent pickup value	0.5 to 31.875 A	0.125 A	31.875 A
32	PH CURVE	Phase inverse time-overcurrent curve select	See note 6	. . .	USA1
33	PH DIAL	Phase inverse time-overcurrent dial setting	See note 6	. . .	SET 15.0
34	GND TOC	Ground inverse time-overcurrent enable/disable	ENABLE/DISABLE	. . .	DISABLE
35	G PICKUP	Ground inverse time-overcurrent pickup value	0.5 to 31.0 A	0.125 A	31.0 A
36	G CURVE	Ground inverse time-overcurrent curve select	See note 7	. . .	USA1
37	GND DIAL	Ground inverse time-overcurrent dial setting	See note 7	. . .	SET 15.0
38	OVHD/UGD	Overhead or underground cable	OVHD or UGD	. . .	UGD
39	OPEN CON	Open conductor action	ALARM or TRIP	. . .	ALARM (9)
41	CM ALM D	Communications alarm delay	ENABLE/DISABLE	. . .	ENABLE
43	DEFAULT	Resets Parameter #'s 20 - 52 to default values	ENABLE/DISABLE	. . .	DISABLE (2)
44	BEEPER	Enable/disable audible beeper	ENABLE/DISABLE	. . .	ENABLE (3)
45	DISPLAY	Adjust display intensity	4 levels	. . .	Brightest (4)
46	XMIT ADD1	Select transmit address 1	16 to 4095	1	0000
47	XMIT ADD2	Select transmit address 2	16 to 4095	1	0000
50	G B4 TRP	Guard before trip	ENABLE/DISABLE	. . .	ENABLE
51	RS232 BD	Selects RS-232 baud rate	1200, 2400, 9600	. . .	1200
52	RS232 PR	Selects RS-232 handshaking protocol	XON/XOFF or RTS/CTS	. . .	XON/XOFF
141	SEL POLE	Single-Pole trip method	ENABLE/DISABLE(10)	. . .	DISABLE
145	TRIP RLS	Selects mode of trip release	3 choices (11)	. . .	TRIP+100

Notes for Tables 6-9 and 6-10:

1. Bias control and ground delay settings will track each other from 50 ms to 750 ms. Above 750 ms, the ground delay varies in non-proportional steps:

Bias	Ground
800 ms	2 s
850 ms	5 s
900 ms	10 s
950 ms	15 s
1000 ms	30 s

2. When this parameter is enabled and the **[ENT]** key is pressed, the Display Controller requests that the PROGRAM mode security code (.248) be entered. Once it is, all parameter values will be reset to the default values listed above. These are the values the parameters are set to before the RFL 9300 leaves the factory.

>> Notes continue on next page <<

Notes for Tables 6-9 and 6-10 (continued):

3. When this parameter is set to ENABLE, the audible beeper can be used to notify the operator if an alarm condition exists. During prolonged alarm conditions, the user may wish to disable the beeper until the condition is corrected. It is recommended that this parameter remain enabled. Alarms may not be noticed if the display is in the READ or PROGRAM mode, or if the RFL 9300 is not being manned and the user is depending on the beeper to indicate an alarm condition.

4. When this parameter is shown, the **[8]** and **[0]** keys can be used to increase or decrease the display intensity (or brightness). When the setting is changed, the bottom line of the display will change to the new intensity, while the top line unit remains constant as a reference. When the **[ENT]** key is pressed, both lines assume the new intensity setting.

5. In dual-channel systems, either channel number may be displayed if COMM MODE (Parameter #48) is set to AUTO.

6. Settings for phase inverse time-overcurrent backup parameters:
(Parameters 31, 32, 33 are only programmable if parameter #30 is enabled.)

Phase inverse time-overcurrent Dial Setting when phase inverse time-overcurrent Curve Select is: USA 1, USA 2, USA 3 or USA 4	Phase inverse time-overcurrent Dial Setting when phase inverse time-overcurrent Curve Select is: IEC 1, IEC 2, IEC 3 or IEC 4
SET 0.5 SET 1.0 SET 2.0 SET 3.0 SET 4.0 SET 5.0 SET 6.0 SET 8.0 SET 10.0 SET 12.0 SET 15.0	SET 0.05 SET .1 SET .2 SET .3 SET .4 SET .5 SET .6 SET .7 SET .8 SET .9 SET 1.0

7. Settings for ground inverse time-overcurrent backup parameters:
(Parameters 35, 36, 37 are only programmable if parameter #34 is enabled.)

Ground inverse time-overcurrent Dial Setting when ground inverse time-overcurrent Curve Select is: USA 1, USA 2, USA 3 or USA 4	Ground inverse time-overcurrent Dial Setting when ground inverse time-overcurrent Curve Select is: IEC 1, IEC 2, IEC 3 or IEC 4
SET 0.5 SET 1.0 SET 2.0 SET 3.0 SET 4.0 SET 5.0 SET 6.0 SET 8.0 SET 10.0 SET 12.0 SET 15.0	SET 0.05 SET .1 SET .2 SET .3 SET .4 SET .5 SET .6 SET .7 SET .8 SET .9 SET 1.0

8. Backup enable/disable is not a programmable parameter when the stub-bus function is active (see paragraph 3.13).

9. Open Conductor - Parameter #39 – not programmable when single-pole trip is active.

10. Selective Pole Relaying - Parameter #141 – programmable only when single-pole trip is active.

11. Three trip release methods are available - Parameter #145:

    CS+TRIP - Output trip will unlatch when both the internal Phase Controller trip and DC trip current sense signals are no longer active.

    TRIP+100 - Output trip will be unlatched 100ms after the internal Phase Controller trip signal is no longer active.

    TRIP + 0 - Output trip will be released with 0ms delay when the internal Phase Controller trip signal becomes inactive.

6.4.4.2 PARAMETER PROGRAMMING

Parameters must be displayed before they can be programmed. Two different methods can be used to display parameters. The first method is to use the **[ENT]** and **[9]** keys to scroll through the parameter list. The second method is to manually enter the parameter number listed in Tables 6-9 or 6-10 as applicable.

For example, if you want to select the local phase fault detector current, press the **[.]**, **[2]**, **[5]**, and **[ENT]** keys to select Parameter #25 ("FD PHASE" - Local Phase Fault Detector Current). Once the parameter is displayed, press the **[8]** or **[0]** keys until the desired value is displayed on the bottom line of the display. All programmable values and settings are factory preset; non-standard values cannot be entered.

When the desired phase fault detector value appears on the bottom line of the display, press the **[ENT]** key. This will send the new phase fault detector value to the RFL 93A SV Supervisor Module. The RFL 93A DISPLAY module saves the new setting in its non-volatile memory. The next parameter (Parameter #26, "FD GND" - Local Ground Fault Detector Current) will be displayed.

NOTE

Any new settings you make do not become active until you exit the PROGRAM mode. Until then, the RFL 9300 remains active under the old parameter settings.

6.4.4.3 EXITING THE PROGRAM MODE

To exit the PROGRAM mode, proceed as follows:

1. Press the **[.]** key, followed by the **[0]** and **[ENT]** keys.
   The word "EXIT" will appear on the top line of the display, with the word "DISABLE" on the bottom line.

2. Press the **[8]** key once.
   The word "ENABLE" will appear on the bottom line of the display.

3. Press the **[ENT]** key.
   The message "SEC CODE" will appear on the display. This means that you must enter a security code before the RFL 9300 will exit the PROGRAM mode. Press the [.], [2], [4],[8] and [ENT] keys to enter the required security code.

The RFL 9300 will return to the STANDBY mode, and the display will return to the moving dot pattern.

6.5 ACCESSING THE RFL 9300 FROM A PC OR TERMINAL

You can use the RS-232 connector on the rear of the RFL 9300 to access it from a dumb terminal or a personal computer equipped with a terminal emulator. Once connected, you can use APRIL (**A**synchronous **P**rogramming and **R**emote **I**nterrogation **L**anguage) to do any of the following:

1. View a list of parameter settings.
2. Change parameter settings as required.
3. Monitor RFL 9300 operation.
4. Review lists of alarms.
5. Review the sequence of events log.
6. Observe oscillographs of trip currents (only on a personal computer).

Because APRIL is menu-based, you do not have to memorize the commands. Help screens can always be displayed by pressing the **[H]** key.

To use APRIL, you will have to connect your terminal or PC to the front or rear panel RS-232 connectors. The rear panel connector is J1 on the relay I/O module, directly behind the power supply module. You can use a dumb terminal, or a PC or laptop computer with an RS-232 port running a terminal emulation program. You could also connect J1 to one of the ports on an RFL 9660 Digital Switch or a stand-alone modem, and access the RFL 9300 with APRIL from a remote site.

The rear panel RS-232 port is normally active. When the front panel RS-232 port is activated, the rear port will be automatically disconnected. The front port is activated by enabling the DTR line on pin 4 of the standard DB9 female connector. This will normally happen with any communication software running on a laptop or PC>

6.5.1 COMMUNICATION INFORMATION

The serial port on your terminal or computer must be configured the same as the RFL 9300's serial port. The settings are as follows:

Data Bits	8
Stop Bits	1
Parity	None
Baud Rate	1200, 2400, or 9600 baud
Handshaking:	XON/XOFF

"Baud rate" determines how fast data is sent through the RS-232 port. Three different settings are possible with the RFL 9300: 1200 baud, 2400 baud, and 9600 baud. 9600 baud will work in most cases, and is recommended.

When connecting your PC or laptop to the front panel RS-232 connector, use the straight through cable connections shown in Figure 6-4. When connecting your PC or laptop to the rear panel RS-232 connector, use the cable connections shown in Figure 6-5.

RTS/CTS handshaking is no longer supported by the RFL 9300.

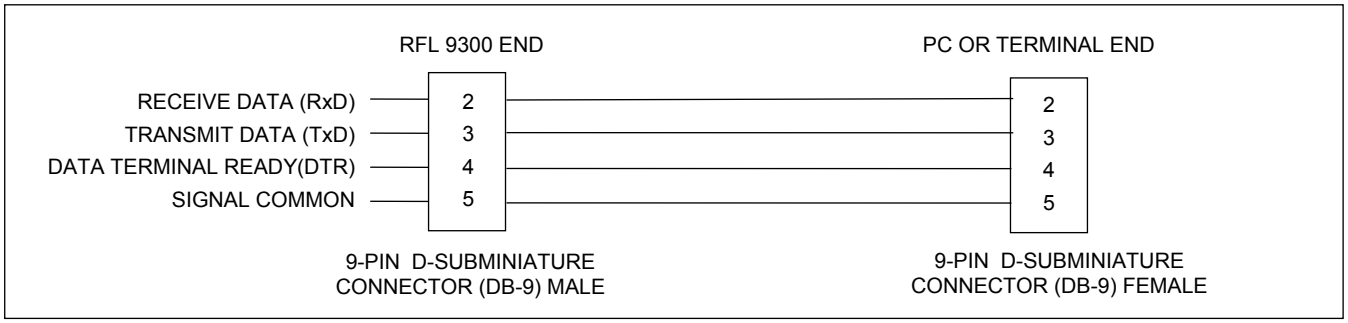


Figure 6-4. Front Panel RS-232 cable connections.

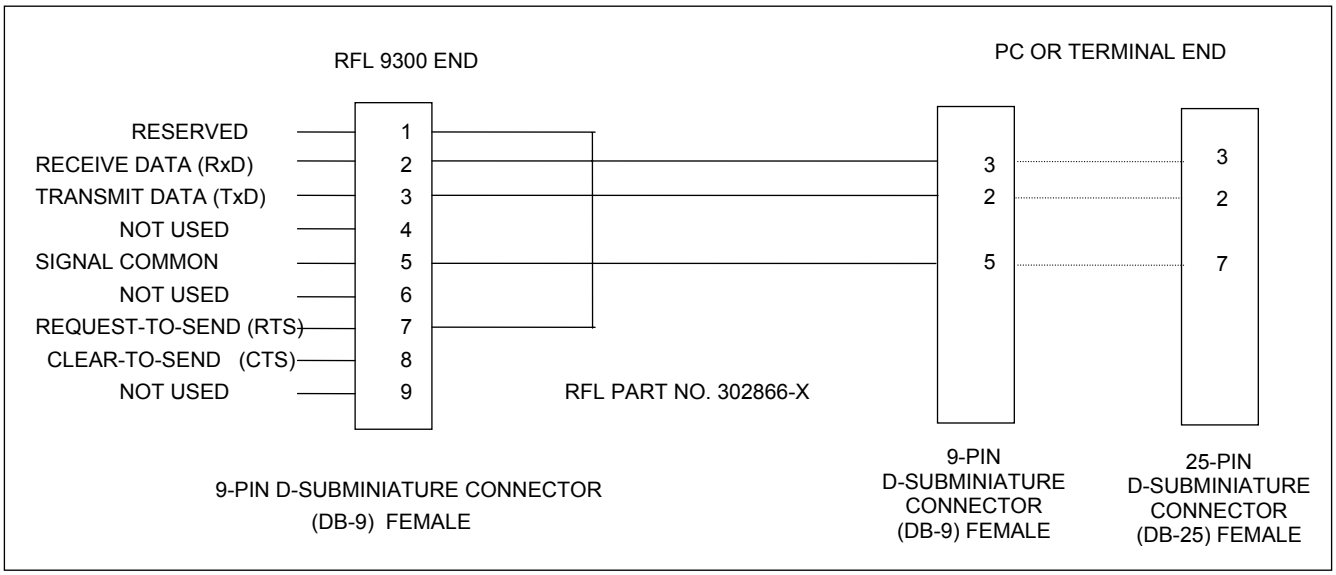


Figure 6-5. Cable connections between RFL 9300 and PC or terminal using XON/XOFF handshaking

In order to select the RFL 9300's baud rate and handshaking protocol, you must enter the programming mode using the keypad on the RFL 9300's display controller and change two of its parameter settings. To do this, use the following procedure:

1. Press the **[ENT]** key three times.
   The word "PROGRAM" will appear on the top line of the display, and the word "DISABLE" will appear on the bottom line.

2. Press the **[8]** key once.
   The word "ENABLE" will appear on the bottom line of the display.

3. Press the **[ENT]** key once.
   The message "SEC CODE" will appear on the display. This means that you must enter a security code before the RFL 9300 will enter the PROGRAM mode. Press the [.], [2], [4], [8], and [ENT] keys to enter the required security code.

If you enter the wrong security code, the word "PROGRAM" will appear on the top line of the display, and the word "DISABLE" on the bottom line. If this happens, repeat steps 2 and 3, making sure you enter the correct security code.

Once the proper security code is entered, the name of the first programmable parameter ("PH BIAS") will appear on the top line of the display. The stored bias value (in amperes) will appear on the bottom line.

4. Press the **[.]** key to access the keypad.

5. Press the **[5]**, **[1]**, and **[ENT]** keys to select Parameter #51 ("RS232 BD" - RS-232 Baud Rate).
   The parameter name ("RS232 BD") will appear on the top line of the display, with the baud rate listed on the bottom line.

   If you make a mistake entering the parameter number, press the [.] key before you press the [ENT] key, and then enter the correct parameter number.

6. Once the baud rate parameter is displayed, press the **[8]** or **[0]** keys until the desired value is displayed on the bottom line of the display.
   Three values can be selected: 1200 baud (the default setting), 2400 baud, and 9600 baud. Setting this parameter to 2400 baud will allow communications with most devices.

7. When the desired baud rate value appears on the bottom line of the display, press the **[ENT]** key.
   This will send the new baud rate value to the RFL 93B SV Supervisor Module. The RFL 93B DISPLAY module saves the new setting in its non-volatile memory.

   The next parameter (Parameter #52, "RS232 PR" - RS-232 Protocol) will be displayed. The parameter name ("RS232 PR") will appear on the top line of the display, with the handshaking method listed on the bottom line.

8. Once the protocol parameter is displayed, press the **[8]** or **[0]** keys until the desired value is displayed on the bottom line of the display.
   Two different protocol methods can be selected: "XON/XOFF" (the default setting) and "RTS/CTS." The RFL 9300 will always transmit an "XON" when activating the RS-232 port, and an "XOFF" when de-activating the port. This will occur about every 100 ms, with the port activated for about 68 ms of the 100-ms period.

   The RTS line will be activated every 100 ms for about 60 ms. If Parameter #52 is set for RTS/CTS handshaking, the CTS line must be active in order for the RS-232 port to be made functional.

9. When the desired protocol method appears on the bottom line of the display, press the **[ENT]** key.
   This will send the new protocol method to the RFL 93B SV Supervisor Module. The RFL 93B DISPLAY module saves the new setting in its non-volatile memory.

10. Press the **[.]** key, followed by the **[0]** and **[ENT]** keys.
    The word "EXIT" will appear on the top line of the display, with the word "DISABLE" on the bottom line.

11. Press the **[8]** key.
    The word "ENABLE" will appear on the bottom line of the display.

12. Press the **[ENT]** key.

The message "SEC CODE" will appear on the display. This means that you must enter a security code before the RFL 9300 will exit the PROGRAM mode. Press the [.], [2], [4], [8] and [ENT] keys to enter the required security code.

If you enter the wrong security code, the word "EXIT" will appear on the top line of the display, and the word "DISABLE" on the bottom line. If this happens, repeat steps 11 and 12, making sure you enter the correct security code.

The RFL 9300 will return to the STANDBY mode, and the display will return to the moving dot pattern.

6.5.2 VIEWING APRIL COMMANDS

Once you have connected a terminal to J1 (either directly or through an RFL 9660), press the **[ENTER]** key a few times. The RFL 9300 will send the following prompt to your terminal:

9300>

This means that you have accessed the RFL 9300, and can now use APRIL commands to view lists of parameter settings, alarm conditions, and other information. To view a list of the APRIL commands, press the **[H]** and **[ENTER]** keys:

9300>H [ENTER]

This tells the RFL 9300 to send a list of APRIL commands to your terminal. A typical APRIL command list appears in Figure 6-6.

```
RFL Electronics APRIL(t) Remote Communications, Version 2.1 (c) 1993, 1996
SUBSTATION 12
H - Display the main menu
A - Go to the alarms display
V - Go to the values display
P - Go to the programming menu (password required)
D - Go to the read settings menu
F - Go to the configuration and software version display
K - Go to the Remote Parameters display
U - Enter the update mode
X - Exit the update mode
S - Go to the sequence of events menu
9300>
```

Figure 6-6. APRIL commands for use with RFL 9300 (for two-terminal and three-terminal mode)

For more information on each APRIL command, refer to the paragraph number listed below.

Command	Meaning	Para.
H	Display the main menu	6.5.2
A	Go to the alarms display	6.5.3
V	Go to the values display	6.5.4
P	Go to the programming menu (password required)	6.5.11
D	Go to the read settings menu	6.5.5
F	Go to the configure and software version display	6.5.6
K	Go to the Remote Parameters display	6.5.7
U	Enter the update mode	6.5.8
X	Exit the update mode	6.5.8
S	Go to the sequence of events menu	6.5.9

6.5.3 VIEWING THE ALARMS DISPLAY

To view the current status of all RFL 9300 alarms, enter the "A" command.

Format: 9300>A [ENTER]

The "A" command tells the RFL 9300 to send a copy of the alarms display to your terminal. A typical alarm display for two-terminal mode is shown in Figure 6-7. A typical alarm display for three-terminal mode is shown in Figure 6-8.

#	ALARM	STATUS (I/A)	#	ALARM	STATUS (I/A)
010	DC 9 Seconds	I	012	DC No Ack 200ms	I
013	DC 3 NAKs	I	014	DC - OC No Comms	I
015	DC NV RAM Fail	I	016	Transmit Addr 1	I
024	DC DTT I	I	025	DC I Sense Ckt	I
027	DC 3Ph Trip I	I	030	SV LCCT Ground	I
031	SV LCCT A	I	032	SV LCCT B	I
033	SV LCCT C	I	034	SV Parallel Port	I
035	SV S/W Mismatch	I	037	SV/R1 Config Err	I
045	Open Conductor	I	046	System Comms	I
054	SPT Trip General	I	055	PH A SG Pole CS	I
056	PH B SG Pole CS	I	057	PH C SG Pole CS	I
060	PH A Cntrlr	I	061	PH B Cntrlr	I
062	PH C Cntrlr	I	063	3I0 Cntrlr	I

9300>

Figure 6-7. Typical alarm display for two-terminal mode

#	ALARM	STATUS (I/A)	#	ALARM	STATUS (I/A)
010	DC 9 Seconds	I	012	DC No Ack 200ms	I
013	DC 3 NAKs	I	014	DC - OC No Comms	I
015	DC NV RAM Fail	I	016	Transmit Addr 1	I
017	Transmit Addr 2	I	024	DC DTT I	I
025	DC I Sense Ckt	I	027	DC 3Ph Trip I	I
030	SV LCCT Ground	I	031	SV LCCT A	I
032	SV LCCT B	I	033	SV LCCT C	I
034	SV Parallel Port	I	035	SV S/W Mismatch	I
037	SV/R1 Config Err	I	045	Open Conductor	I
046	System Comms	I	047	SV/R2 Config Err	I
054	SPT Trip General	I	055	PH A SG Pole CS	I
056	PH B SG Pole CS	I	057	PH C SG Pole CS	I
060	PH A Cntrlr	I	061	PH B Cntrlr	I
062	PH C Cntrlr	I	063	3I0 Cntrlr	I
9300>					

Figure 6-8. Typical alarm display for three-terminal mode

The alarm display shows the code number for each alarm, a brief description of its meaning, and its status ("I" for "inactive," or "A" for "active"). Full descriptions for each alarm are as follows:

010 - DC 9 Seconds Local Display Controller Alarm: 9 seconds has elapsed without supervisor communications.

012 - DC No Ack 200ms Local Display Controller Alarm: No acknowledgment from Supervisor Module in 200 ms.

013 - DC 3 NAKs Local Display Controller Alarm: Three non-acknowledgments (NAKs) from Supervisor Module.

014 - DC - OC No Comms Local Oscillography Controller Alarm: Display Controller lost communication with oscillography board.

015 - DC NV RAM Fail Local Display Controller Alarm: Non-volatile RAM failure on Display Controller.

016 - Transmit Addr 1 General Alarm: Remote address 1 does not match local address or remote unit is not responding. (Local address plus remote address must equal 4095)

017 - Transmit Addr 2 General Alarm: Remote address 2 does not match local address or remote unit is not responding. (Local address plus remote address must equal 4095)

024 - DC DTT I Display Controller Trip Alarm: DC trip current sensed for more than 500ms

025 - DC I Sense Ckt Display Controller Trip Alarm: Current Sense circuit failure.

027 - DC 3Ph Trip I Display Controller Trip Alarm: Three-pole dc trip current sensed for more than 500ms.

030 - SV LCCT Ground Local Alarm From Supervisor Module: Local Charge Comparison Trip (calculated without active fault detector) 3I0 controller.

031 - SV LCCT A Local Alarm From Supervisor Module: Local Charge Comparison Trip (calculated without active fault detector) Phase A.

032 - SV LCCT B Local Alarm From Supervisor Module: Local Charge Comparison Trip (calculated without active fault detector) Phase B.

033 - SV LCCT C Local Alarm From Supervisor Module: Local Charge Comparison Trip (calculated without active fault detector) Phase C.

034 - SV Parallel Port Local Alarm From Supervisor Module: Parallel Port Alarm.

035 - SV S/W Mismatch Local Alarm From Supervisor Module: Software Mismatch Alarm.

037 - SV/R1 Config Err General Alarm From Remote 1 Supervisor Module: Configuration Mismatch of programmable jumpers.

045 - Open Conductor Local Alarm: Open conductor alarm.

046 - System Comms Remote/General Alarm: Communications to/from remote station are failed or impaired.

047 - SV/R2 Config Err General Alarm From Remote 2 Supervisor Module: Configuration Mismatch of programmable jumpers.

054 – SPT General Single-Pole logic general alarm. Problem on SP chassis detected by 93B SV. Problem with (or no) serial message sent by SP logic.

055 – PH A SG POLE CS Phase A single-pole trip alarm: Phase A dc trip current sensed for more than 500ms by SP logic, or Phase A dc trip current sensed without a Phase A trip signal being issued.

056 – PH B SG POLE CS Phase B single-pole trip alarm: Phase B dc trip current sensed for more than 500ms by SP logic, or Phase B dc trip current sensed without a Phase B trip signal being issued.

057 – PH C SG POLE CS Phase C single-pole trip alarm: Phase C dc trip current sensed for more than 500ms by SP logic, or Phase C dc trip current sensed without a Phase C trip signal being issued.

060 – PH A Cntrlr Phase A Controller general alarm: Fail bus test with 93B SV, bad communications with 93B SV, excessive channel delay detected, or system clock out of spec.

061 – PH B Cntrlr Phase B Controller general alarm: Fail bus test with 93B SV, bad communications with 93B SV, excessive channel delay detected, or system clock out of spec.

062 – PH C Cntrlr Phase C Controller general alarm: Fail bus test with 93B SV, bad communications with 93B SV, excessive channel delay detected, or system clock out of spec.

063 – 3I0 Cntrlr Phase 3I0 Controller general alarm: Fail bus test with 93B SV, bad communications with 93B SV, excessive channel delay detected, or system clock out of spec.

6.5.4 VIEWING THE VALUES DISPLAY

To view a list of all measured parameter values, enter the "V" command.

Format: 9300>V [ENTER]

The "V" command tells the RFL 9300 to send a copy of the most recently measured values to your terminal. A typical values display for modem communications is shown in Figure 6-9 for two-terminal mode, and in Figure 6-10 for three-terminal mode.

```
#          DESCRIPTION          VALUE
001        Ping Pong R1         018.0 ms
003        CDC Remote #1        018.0 ms
005        Local I A            01.50 amps
006        Local I B            01.50 amps
007        Local I C            01.50 amps
008        Local 3I0            00.00 amps
009        Remote #1 I A        01.50 amps
010        Remote #1 I B        01.50 amps
011        Remote #1 I C        01.50 amps
012        Remote #1 3I0        00.00 amps
017        Remote Address 1     Tx Addr Verified
077        R1 CDC               018.0 ms
076        R1 PingPong          018.0 ms
9300>
```

Figure 6-9. Typical values display for two-terminal mode

```
#          DESCRIPTION          VALUE
001        Ping Pong R1         004.0 ms
002        Ping Pong R2         004.0 ms
005        Local I A            02.00 Amps
006        Local I B            02.00 Amps
007        Local I C            02.00 Amps
008        Local 3I0            00.00 Amps
009        Remote #1 I A        05.00 Amps
010        Remote #1 I B        05.00 Amps
011        Remote #1 I C        05.00 Amps
012        Remote #1 3I0        00.00 Amps
013        Remote #2 I A        03.00 Amps
014        Remote #2 I B        03.00 Amps
015        Remote #2 I C        03.00 Amps
016        Remote #2 3I0        00.00 Amps
017        Remote Address 1     Tx Addr Verified
018        Remote Address 2     Tx Addr Verified
076        R1 PingPong          004.0 ms
101        R2 PingPong          004.0 ms
 9300
   >
```

Figure 6-10. Typical values display for three-terminal mode

The values display shows the code number for each measured value, a brief description of its meaning, and its measured value. Full descriptions for each measured value are as follows:

001 - Ping Pong R1 One-half the round-trip communications channel delay between local relay and remote 1 as measured by local relay.

002 - Ping Pong R2 One-half the round-trip communications channel delay between local relay and remote 2 as measured by local relay.

003 - CDC Remote #1 One way compensated communications channel delay for messages received from remote 1 – two-terminal systems only.

005 - Local I A Local Phase A current.

006 - Local I B Local Phase B current.

007 - Local I C Local Phase C current.

008 - Local 3I0 Local $3I_0$ current.

009 - Remote #1 I A Remote #1 Phase A current.

010 - Remote #1 I B Remote #1 Phase B current.

011 - Remote #1 I C Remote #1 Phase C current.

012 - Remote #1 3I0 Remote #1 $3I_0$ current.

013 - Remote #2 I A Remote #2 Phase A current.

014 - Remote #2 I B Remote #2 Phase B current.

015 - Remote #2 I C Remote #2 Phase C current.

016 - Remote #2 3I0 Remote #2 $3I_0$ current.

017 - Remote Address 1 Transmit address 1 verified.

018 - Remote Address 2 Transmit address 2 verified.

076 – R1 Ping Pong One-half the round-trip communications channel delay between remote 1 and local relay as measured by remote 1.

077 – R1 CDC One way compensated communications channel delay for messages received from local relay at remote 1 (two-terminal systems only).

101 - R2 Ping Pong One-half the round-trip communications channel delay between remote 2 and local relay as measured by remote 2.

6.5.5 READING PARAMETER SETTINGS

The "D" command tells the RFL 9300 to send a list of all parameter settings to your terminal. This list of settings is called the "read settings" menu.

Format: 9300>D [ENTER]

Typical read settings menus appear in Figures 6-11 through 6-14. All settings described in Section 4 of this manual are shown, but you can't change the displayed values. To change these values, you will have to enter the programming mode. (See para. 6.4.4 for more information.) The programming mode is password-protected, so only authorized persons can change the RFL 9300's parameter settings.

#	PARAMETER	SETTING	#	PARAMETER	SETTING
020	Phase Bias	.500 amps	021	Ground Bias	1.500 amps
022	Bias Control	Disable	023	Ground Delay	Enable
024	Bias/Ground Dly	.05/.05 sec	025	F. D. Phase	8.0 Amps
026	F. D. Ground	1.0 Amp	027	Backup (1)	Enable
028	Phase O/C Bkup	31.875 Amps	029	Ground O/C Bkup	31.000 Amps
030	Phase TOC (2)	Disable	031	Ph TOC Pickup	N/A
032	Ph TOC Curve	N/A	033	Ph TOC Dial	N/A
034	Ground TOC (3)	Disable	035	Gd TOC Pickup	N/A
036	Gd TOC Curve	N/A	037	Gd TOC Dial	N/A
038	Overhd/Undergd	Overhead	040	Stub Bus (1)	Inactive
041	Comms Alm Dly	Disable	042	DC Offset Filter	Enable
044	Beeper	Disable	046	Transmit Addr 1	4079
048	Comms Mode	Auto	049	Active Channel	1
050	Guard/Trip	Disable	120	Current Date	08/16/00
121	Current Time	09:25:23			
122	Reset Disp. Alrm	No	140	Single Pole	Active
141	Slctv Pole RL	Disable	145	Trip Release	CS+TRIP
999	System Label	Gen1			

9300>

Figure 6-11. Typical read settings menu for two-terminal single-pole mode

#	PARAMETER	SETTING	#	PARAMETER	SETTING
020	Phase Bias	1.500 Amps	021	Ground Bias	1.500 Amps
022	Bias Control	Disable	023	Ground Delay	Enable
024	Bias/Ground Dly	.05/.05 sec	025	F. D. Phase	8.0 Amps
026	F. D. Ground	1.0 Amp	027	Backup (1)	Enable
028	Phase O/C Bkup	31.875 Amps	029	Ground O/C Bkup	31.000 Amps
030	Phase TOC (2)	Disable	031	Ph TOC Pickup	N/A
032	Ph TOC Curve	N/A	033	Ph TOC Dial	N/A
034	Ground TOC (3)	Disable	035	Gd TOC Pickup	N/A
036	Gd TOC Curve	N/A	037	Gd TOC Dial	N/A
038	Overhd/Undergd	Overhead	039	Open Conductor	Alarm
040	Stub Bus (1)	Inactive	041	Comms Alm Dly	Disable
042	DC Offset Filter	Enable	044	Beeper	Disable
046	Transmit Addr 1	4079	048	Comms Mode	Auto
049	Active Channel	1	050	Guard/Trip	Disable
120	Current Date	08/16/00	121	Current Time	09:27:06
122	Reset Disp. Alrm	No	140	Single Pole	Inactive
145	Trip Release	CS+TRIP			
999	System Label	Gen1			

9300>

Figure 6-12. Typical read settings menu for two-terminal three-pole mode

#	PARAMETER	SETTING	#	PARAMETER	SETTING
020	Phase Bias	1.500 Amps	021	Ground Bias	1.500 Amps
022	Bias Control	Disable	023	Ground Delay	Enable
024	Bias/Ground Dly	.05/.05 sec	025	F.D. Phase	8.0 Amps
026	F.D. Ground	1.0 Amp	027	Backup (1)	Enable
028	Phase O/C Bkup	31.875 Amps	029	Ground O/C Bkup	31.000 Amps
030	Phase TOC (2)	Disable	031	Ph TOC Pickup	N/A
032	PhTOC Curve	N/A	033	Ph TOC Dial	N/A
034	Ground TOC (3)	Disable	035	Gd TOC Pickup	N/A
036	Gd TOC Curve	N/A	037	Gd TOC Dial	N/A
038	Overhd/Undergd	Overhead	040	Stub Bus (1)	Inactive
041	Comms Alm Dly	Disable	044	Beeper	Disable
046	Transmit Addr 1	4079	047	Transmit Addr 2	4075
050	Guard/Trip	Disable	120	Current Date	08/16/00
121	Current Time	09:29:27			
122	Reset Disp. Alrm	No	140	Single Pole	Active
141	Slctv Pole RL	Disable	145	Trip Release	CS+TRIP
999	System Label	Gen1			

9300>

Figure 6-13. Typical read settings menu for three-terminal single-pole mode

#	PARAMETER	SETTING	#	PARAMETER	SETTING
020	Phase Bias	1.500 Amps	021	Ground Bias	1.500 Amps
022	Bias Control	Disable	023	Ground Delay	Enable
024	Bias/Ground Dly	.05/.05 sec	025	F.D. Phase	8.0 Amps
026	F.D. Ground	1.0 Amp	027	Backup (1)	Enable
028	Phase O/C Bkup	31.875 Amps	029	Ground O/C Bkup	31.000 Amps
030	Phase TOC (2)	Disable	031	Ph TOC Pickup	N/A
032	PhTOC Curve	N/A	033	Ph TOC Dial	N/A
034	Ground TOC (3)	Disable	035	Gd TOC Pickup	N/A
036	Gd TOC Curve	N/A	037	Gd TOC Dial	N/A
038	Overhd/Undergd	Overhead	039	Open Conductor	Alarm
040	Stub Bus (1)	Inactive	041	Comms Alm Dly	Disable
044	Beeper	Disable	046	Transmit Addr 1	4079
047	Transmit Addr 2	4075	050	Guard/Trip	Disable
120	Current Date	08/16/00	121	Current Time	10:12:58
122	Reset Disp. Alrm	No	140	Single Pole	Inactive
145	Trip Release	CS+TRIP			
999	System Label	Gen1			

9300>

Figure 6-14. Typical read settings menu for three-terminal three-pole mode

The following NOTES apply to Figures 6-11 through 6-14:

1. If Stub-Bus (parameter #40) is active, Backup (parameter #27) will show a setting of SBACTIVE. This indicates that the relay has been placed in Backup Mode. See Section 3.13 for more information.
2. If parameter No. 030 is disabled, then parameter numbers 031, 032 and 033 will display N/A (not applicable).
3. If parameter No. 034 is disabled, then parameter numbers 035, 036 and 037 will display N/A (not applicable).

6.5.6 VIEWING CONFIGURATION AND SOFTWARE INFORMATION

The "F" command tells the RFL 9300 to send a configuration and software version display to your terminal. This display tells you how the RFL 9300 is configured, and what software version is being used in each of its controllers (communications controller(s), supervisor controller, phase controllers, and display controller).

Format: 9300>F [ENTER]

A typical configuration and software version display for two and three-terminal systems is shown in Figure 6-15.

```
#  DESCRIPTION       CONFIGURATION
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
130  Terminals       2
132  CT Full Scale   5 amps
133  Frequency       60 Hz
140  Single Pole     Active

#  MODULE            SOFTWARE VERSION
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
103  SW ID CC        009
104  SW ID CC2       009*
105  SW ID SV        007
106  SW ID PCA       009
107  SW ID PCB       009
108  SW ID PCC       009
109  SW ID PCG       009
110  SW ID DC        009
9300> _
```

*For a two-terminal system, the second communications module (CC2) is not installed and the software version for parameter #104 will indicate “Not Installed”

Figure 6-15. Typical configuration and software version display for two-terminal and three-terminal systems

The configuration and software version display shows the code number for each item, a brief description of its meaning, and its value. Full descriptions for each item are as follows:

130 - Terminals The RFL 9300's terminal configuration; "2" for two-terminal, or "3" for three-terminal.

132 - CT Full Scale The rating of the CT's being used to feed the RFL 9300; "1" for 1-amp CT's, or "5" for 5-amp CT's.

133 - Frequency The power system frequency; either 50 Hz or 60 Hz.

140 – Single Pole Single Pole mode; either active or inactive.

103 - SW ID CC1 The software version currently running on Communications Controller #1.

104 - SW ID CC2 The software version currently running on Communications Controller #2. If there is only one Communications Controller in the RFL 9300, the words "Not installed" will appear.

105 - SW ID SV The software version currently running on the Supervisor Controller.

106 - SW ID PCA The software version currently running on the Phase Controller Module monitoring Phase A.

107 - SW ID PCB The software version currently running on the Phase Controller Module monitoring Phase B.

108 - SW ID PCC The software version currently running on the Phase Controller Module monitoring Phase C.

109 - SW ID PCG The software version currently running on the Phase Controller Module monitoring $3I_0$.

110 - SW ID DC The software version currently running on the Display Controller.

6.5.7 REMOTE PARAMETERS DISPLAY

To view a list of the remote parameter settings, enter the “K” command.

Format: 9300>K[ENTER]

When the “K” command is entered, the screen on your terminal will be cleared and replaced by the REMOTE PARAMETERS screen. Typical Remote Parameters displays are shown in Figures 6-16 through 6-19.

#	PARAMETER	SETTING	#	PARAMETER	SETTING
053	R1 Phase Bias	1.500 Amps	054	R1 Ground Bias	1.500 Amps
055	R1 Bias Control	Disable	056	R1 Ground Delay	Enable
057	R1 Bias/Gnd Dly	.05/.05 sec	058	R1 FD Phase	8.0 Amps
059	R1 FD Ground	1.0 Amp	060	R1 Backup	Enable
061	R1 Ph O/C Bkup	31.875 Amps	062	R1 Gnd O/C Bkup	31.000 Amps
063	R1 Phase TOC	Disable	064	R1 Ph TOC Pickup	31.875 Amps
065	R1 Ph TOC Curve	N/A	066	R1 Ph TOC Dial	N/A
067	R1 Ground TOC	Disable	068	R1 Gd TOC Pickup	31.000 Amps
069	R1 Gd TOC Curve	N/A	070	R1 Gd TOC Dial	N/A
071	R1 Overhd/Undrgd	Overhead	073	R1 Stub Bus	Inactive
074	R1 DC Offset Flt	Enable	075	R1 Guard/Trip	Disable
076	R1 PingPong	004.0 ms			
077	R1 CDC	004.0 ms	160	R1 Single Pole	Active
161	R1 Slctv Pole RL	Disable	165	Trip Rls	TRIP+100
9300>					

Figure 6-16. Typical Remote Parameters Display for a two-terminal single-pole system

#	PARAMETER	SETTING	#	PARAMETER	SETTING
053	R1 Phase Bias	1.500 Amps	054	R1 Ground Bias	1.500 Amps
055	R1 Bias Control	Disable	056	R1 Ground Delay	Enable
057	R1 Bias/Gnd Dly	.05/.05 sec	058	R1 FD Phase	8.0 Amps
059	R1 FD Ground	1.0 Amp	060	R1 Backup	Enable
061	R1 Ph O/C Bkup	31.875 Amps	062	R1 Gnd O/C Bkup	31.000 Amps
063	R1 Phase TOC	Disable	064	R1 Ph TOC Pickup	31.875 Amps
065	R1 Ph TOC Curve	N/A	066	R1 Ph TOC Dial	N/A
067	R1 Ground TOC	Disable	068	R1 Gd TOC Pickup	31.000 Amps
069	R1 Gd TOC Curve	N/A	070	R1 Gd TOC Dial	N/A
071	R1 Overhd/Undrgd	Overhead	072	R1 Open Cond	Alarm
073	R1 Stub Bus	Inactive	074	R1 DC Offset Flt	Enable
075	R1 Guard/Trip	Disable	076	R1 PingPong	004.0 ms
077	R1 CDC	004.0 ms	160	R1 Single Pole	Inactive
165	R1 Trip Rls	TRIP+100			
9300>					

Figure 6-17. Typical Remote Parameters Display for a two-terminal three-pole system

#	PARAMETER	SETTING	#	PARAMETER	SETTING
053	R1 Phase Bias	1.500 Amps	054	R1 Ground Bias	1.500 Amps
055	R1 Bias Control	Disable	056	R1 Ground Delay	Enable
057	R1 Bias/Gnd Dly	.05/.05 sec	058	R1 FD Phase	8.0 Amp
059	R1 FD Ground	1.0 Amp	060	R1 Backup	Enable
061	R1 Ph O/C Bkup	31.875 Amps	062	R1 Gnd O/C Bkup	31.000 Amps
063	R1 Phase TOC	Disable	064	R1 Ph TOC Pickup	31.875 Amps
065	R1 Ph TOC Curve	N/A	066	R1 Ph TOC Dial	N/A
067	R1 Ground TOC	Disable	068	R1 Gd TOC Pickup	31.000 Amps
069	R1 Gd TOC Curve	N/A	070	R1 Gd TOC Dial	N/A
071	R1 Overhd/Undrgd	Overhead	073	R1 Stub Bus	Inactive
075	R1 Guard/Trip	Disable	076	R1 PingPong	004.0 ms
160	R1 Single Pole	Active	161	R1 Slctv Pole RL	Disable
165	R1 Trip Rls	TRIP+100			
078	R2 Phase Bias	1.500 Amps			
079	R2 Ground Bias	1.500 Amps	080	R2 Bias Control	Disable
081	R2 Ground Delay	Enable	082	R2 Bias/Gnd Dly	.05/.05 sec
083	R2 FD Phase	8.0 Amp	084	R2 FD Ground	1.0 Amp
085	R2 Backup	Enable	086	R2 Ph O/C Bkup	31.875 Amps
087	R2 Gnd O/C Bkup	31.000 Amps	088	R2 Phase TOC	Disable
089	R2 Ph TOC Pickup	31.875 Amps	090	R2 Ph TOC Curve	N/A
091	R2 Ph TOC Dial	N/A	092	R2 Ground TOC	Disable
093	R2 Gd TOC Pickup	31.000 Amps	094	R2 Gd TOC Curve	N/A
095	R2 Gd TOC Dial	N/A	096	R2 Overhd/Undrgd	Overhead
098	R2 Stub Bus	Inactive	100	R2 Guard/Trip	Disable
101	R2 PingPong	004.0 ms	180	R2 Single Pole	Active
181	R2 Slctv Pole RL	Disable	185	R2 Trip Rls	TRIP+100

9300>

Figure 6-18. Typical Remote Parameters Display for a three-terminal single-pole system

#	PARAMETER	SETTING	#	PARAMETER	SETTING
053	R1 Phase Bias	7.0 Amps	054	R1 Ground Bias	1.500 Amps
055	R1 Bias Control	Enable	056	R1 Ground Delay	Enable
057	R1 Bias/Gnd Dly	.90/10 sec	058	R1 FD Phase	8 Amp
059	R1 FD Ground	1 Amp	060	R1 Backup	Enable
061	R1 Ph O/C Bkup	31.875 Amps	062	R1 Gnd O/C Bkup	31.000 Amps
063	R1 Phase TOC	Enable	064	R1 Ph TOC Pickup	31.875 Amps
065	R1 Ph TOC Curve	USA1	066	R1 Ph TOC Dial	N/A
067	R1 Ground TOC	Enable	068	R1 Gd TOC Pickup	31.000 Amps
069	R1 Gd TOC Curve	USA1	070	R1 Gd TOC Dial	N/A
071	R1 Overhd/Undrgd	Underground	072	R1 Open Cond	Alarm
073	R1 Stub Bus	Inactive	075	R1 Guard/Trip	Disable
076	R1 PingPong	018.0 ms			
160	R1 Single Pole		165	R1 Trip Rls	TRIP+100
078	R2 Phase Bias	7.0 Amps	079	R2 Ground Bias	1.500 Amps
080	R2 Bias Control	Enable	081	R2 Ground Delay	Enable
082	R2 Bias/Gnd Dly	.90/10 sec	083	R2 FD Phase	8 Amp
084	R2 FD Ground	1 Amp	085	R2 Backup	Enable
086	R2 Ph O/C Bkup	31.875 Amps	087	R2 Gnd O/C Bkup	31.000 Amps
088	R2 Phase TOC	Enable	089	R2 Ph TOC Pickup	31.875 Amps
090	R2 Ph TOC Curve	IEC1	091	R2 Ph TOC Dial	N/A
092	R2 Ground TOC	Enable	093	R2 Gd TOC Pickup	31.000 Amps
094	R2 Gd TOC Curve	USA4	095	R2 Gd TOC Dial	N/A
096	R2 Overhd/Undrgd	Underground	097	R2 Open Cond	Alarm
098	R2 Stub Bus	Inactive	100	R2 Guard/Trip	Disable
101	R2 PingPong		180	R2 Single Pole	Inactive
185	R2 Trip Rls	019.5 ms			

9300>

Figure 6-19. Typical Remote Parameters Display for a three-terminal three-pole system

The Remote Parameters screen shows the code number for each item, a brief description of its meaning, and its setting. Full descriptions for each item are as follows:

053 - R1 Phase Bias Remote 1 Phase Bias setting in amperes. Can be set from 1.0 to 8.0 amperes in 0.5 ampere steps.

054 - R1 Ground Bias Remote 1 Ground Bias setting in amperes. Can be set from 1.0 to 2.25 amperes in 0.25 ampere steps.

055 - R1 Bias Control Remote 1 Bias Control. Can be enabled or disabled.

056 - R1 Ground Delay Remote 1 Ground Delay function. Can be enabled or disabled.

057 - R1 Bias/Gnd Dly Remote 1 Bias Control and Ground Delay time.

058 - R1 FD Phase Remote 1 Phase Overcurrent Fault Detector. Can be set to 6.0 or 8.0 amperes.

059 - R1 FD Ground Remote 1 Ground Overcurrent Fault Detector current. Can be set to 0.5 or 1.0 amperes.

060 - R1 Backup Remote 1 System Backup functions. Can be enabled or disabled.

061 - R1 Ph O/C Bkup Remote 1 Phase Overcurrent Backup function. Can be set from 6.0 to 31.875 amperes in 0.125 ampere steps.

062 - R1 Gnd O/C Bkup Remote 1 Ground Overcurrent Backup function. Can be set from 6.0 to 31.875 amperes in 0.125 ampere steps.

063 - R1 Phase TOC Remote 1 Phase Inverse Time-overcurrent function. Can be enabled or disabled. See note below.

064 - R1 Ph TOC Pickup Remote 1 Phase Inverse Time-overcurrent Pickup value. Can be set from 0.5 to 31.875 amperes in 0.125 ampere steps.

065 - R1 Ph TOC Curve Remote 1 Phase Inverse Time-overcurrent Curve select. Refer to note 6 on page 6-28 for settings.

066 - R1 Ph TOC Dial Remote 1 Phase Inverse Time-overcurrent Dial setting. Refer to note 6 on page 6-28 for settings.

067 - R1 Ground TOC Remote 1 Ground Inverse Time-overcurrent function. Can be enabled or disabled. See note below.

068 - R1 Gd TOC Pickup Remote 1 Ground Inverse Time-overcurrent Pickup value. Can be set from 0.5 to 31.0 amperes in 0.125 ampere steps.

069 - R1 Gd TOC Curve Remote 1 Ground Inverse Time-overcurrent Curve select. Refer to note 7 on page 6-28 for settings.

070 - R1 Gd TOC Dial Remote 1 Ground Inverse Time-overcurrent Dial setting. Refer to note 7 on page 6-28 for settings.

NOTE

If parameter No. 063 is disabled, then parameter numbers 065 and 066 will display N/A (not applicable).
If parameter No. 067 is disabled, then parameter numbers 069 and 070 will display N/A (not applicable).

071 - R1 Overhd/Undrgd	Remote 1 Overhead or Underground cables.
072 - R1 Open Cond	Remote 1 Open Conductor. Can be set to alarm or trip.
073 - R1 Stub Bus	Remote 1 Stub Bus status. Can be active or inactive (not programmable).
074 - R1 DC Offset Flt	Remote 1 DC Offset Filter. Can be set to enable or disable.
075 - R1 Guard/Trip	Remote 1 Guard before Trip. Can be set to enable or disable.
076 - R1 PingPong	Remote 1 PingPong Delay in ms from local to remote 1 as measured by remote 1.
077 - R1 CDC	Remote 1 Channel Delay Compensation in ms.
078 - R2 Phase Bias	Remote 2 Phase Bias setting in amperes. Can be set from 1.0 to 8.0 amperes in 0.5 ampere steps.
079 - R2 Ground Bias	Remote 2 Ground Bias setting in amperes. Can be set from 1.0 to 2.25 amperes in 0.25 ampere steps.
080 - R2 Bias Control	Remote 2 Bias Control. Can be enabled or disabled.
081 - R2 Ground Delay	Remote 2 Ground Delay function. Can be enabled or disabled.
082 - R2 Bias/Gnd Dly	Remote 2 Bias Control and Ground Delay time.
083 - R2 FD Phase	Remote 2 Phase Overcurrent Fault Detector. Can be set to 6.0 or 8.0 amperes.
084 - R2 FD Ground	Remote 2 Ground Overcurrent Fault Detector current. Can be set to 0.5 or 1.0 amperes.
085 - R2 Backup	Remote 2 System Backup functions. Can be enabled or disabled.
086 - R2 Ph O/C Bkup	Remote 2 Phase Overcurrent Backup function. Can be set from 6.0 to 31.875 amperes in 0.125 ampere steps.
087 - R2 Gnd O/C Bkup	Remote 2 Ground Overcurrent Backup function. Can be set from 6.0 to 31.875 amperes in 0.125 ampere steps.
088 - R2 Phase TOC	Remote 2 Phase Inverse Time-overcurrent function. Can be enabled or disabled. See note below.
089 - R2 Ph TOC Pickup	Remote 2 Phase Inverse Time-overcurrent Pickup value. Can be set from 0.5 to 31.875 amperes in 0.125 ampere steps.
090 - R2 Ph TOC Curve	Remote 2 Phase Inverse Time-overcurrent Curve select. Refer to note 6 on page 6-28 for settings.

091 - R2 Ph TOC Dial Remote 2 Phase Inverse Time-overcurrent Dial setting. Refer to note 6 on page 6-28 for settings.

092 - R2 Ground TOC Remote 2 Ground Inverse Time-overcurrent function. Can be enabled or disabled. See note below.

093 - R2 Gd TOC Pickup Remote 2 Ground Inverse Time-overcurrent Pickup value. Can be set from 0.5 to 31.0 amperes in 0.125 ampere steps.

094 - R2 Gd TOC Curve Remote 2 Ground Inverse Time-overcurrent Curve select. Refer to note 7 on page 6-28 for settings.

095 - R2 Gd TOC Dial Remote 2 Ground Inverse Time-overcurrent Dial setting. Refer to note 7 on page 6-28 for settings.

096 - R2 Overhd/Undrgd Remote 2 Overhead or Underground cables.

097 - R2 Open Cond Remote 2 Open Conductor. Can be set to alarm or trip.

098 - R2 Stub Bus Remote 2 Stub Bus status. Can be active or inactive (not programmable).

100 - R2 Guard/Trip Remote 2 Guard before Trip. Can be set to enable or disable.

101 - R2 PingPong Remote 2 PingPong Delay in ms from local to remote 2 as measured by remote 2.

160 - R1 Single-Pole Single-pole status at remote 1. Can be active or inactive. (Jumper selectable using jumper J5 on 93B SV at remote 1)

161 - R1 Selective Pole Selective pole relaying status at remote 1. Can be enabled or disabled. This parameter is only available when single-pole trip is active.

165 - R1 Trip Release Code Determines algorithm used by the Display Controller at remote 1 to determine when output trip signal should be unlatched. Three algorithms are available See note 11 on page 6-30 for details.

180 - R2 Single Pole Single-pole status at remote 2. Can be active or inactive. (Jumper selectable using jumper J5 on 93B SV at remote 2)

181 - R2 Selective Pole Selective pole relaying status at remote 2. Can be enabled or disabled. This parameter is only available when single-pole trip is active.

185 - R2 Trip Release Code Determines algorithm used by the Display Controller at remote 2 to determine when output trip signal should be unlatched. Three algorithms are available See note 11 on page 6-30 for details.

NOTE

If parameter No. 088 is disabled, then parameter numbers 090 and 091 will display N/A (not applicable).
If parameter No. 092 is disabled, then parameter numbers 094 and 095 will display N/A (not applicable).

6.5.8 THE UPDATE MODE

The update mode places a display on your terminal that is constantly updated to show up-to-date information about RFL 9300 operation. This mode is entered by using the "U" command.

Format: 9300>U [ENTER]

When the "U" command is entered, the screen on your terminal will be cleared, and replaced by the UPDATE screen shown in Figure 6-20 for a two-terminal system and Figure 6-21 for a three-terminal system. This is a display of all the measured parameter values. The displayed values are updated about once a second when operating at 2400 baud. This screen can be used to monitor RFL 9300 operation. To exit the update mode, press the **[X]** key, followed by the **[ENTER]** key. The screen on your terminal will be cleared, and the "9300>" prompt will re-appear.

```
Value Update - Type 'X<CR>' to Stop
001  Ping Pong #1              004.0 ms
003  CDC #1                    004.0 ms
005  Local I A                 00.00 amps
006  Local I B                 00.00 amps
007  Local I C                 00.00 amps
008  Local 3I0                 00.00 amps
009  Remote #1 I A             00.00 amps
010  Remote #1 I B             00.00 amps
011  Remote #1 I C             00.00 amps
012  Remote #1 3I0             00.00 amps
017  Remote Address 1          Tx Addr verified
077  R1 CDC                    004.0 ms
076  R1 PingPong               004.0 ms
9300>
```

Figure 6-20. Typical UPDATE screen for a two-terminal system

```
Value Update - Type 'X<CR>' to Stop
001      Ping Pong #1              004.0 ms
002      Ping Pong #2              004.0 ms
005      Local  I A                00.00 Amps
006      Local  I B                00.00 Amps
007      Local  I C                00.00 Amps
008      Local  I 3I0              00.00 Amps
009      Remote #1 I A             00.00 Amps
010      Remote #1 I B             00.00 Amps
011      Remote #1 I C             00.00 Amps
012      Remote #1 I 3I0           00.0 Amps
013      Remote #2 I A             00.00 Amps
014      Remote #2 I B             00.00 Amps
015      Remote #2 I C             00.00 Amps
016      Remote #2 I 3I0           00.00 Amps
017      Remote Address 1          Tx Addr verified
018      Remote Address 2          Tx Addr verified
076      R1 PingPong               004.0 ms
101      R2 PingPong               004.0 ms
9300>
```

Figure 6-21. Typical UPDATE screen for a three-terminal system

6.5.9 VIEWING THE SEQUENCE OF EVENTS LOGS

The RFL 9300 maintains a list of the last five alarm events and the last five trip events that took place during system operation. The alarm events are stored in the “alarm sequence of events log” and the trip events are stored in the “trip sequence of events log”. To view these logs, first use the “S” command to get into the sequence of events menu as shown in Figure 6-22.

Format: 9300>S [ENTER]

SEQUENCE OF EVENTS MENU

H - Display sequence of events help
A - Display the Alarm sequence of events
T - Display the Trip sequence of events
F - Force an Oscillography event
O - Output Oscillography trip event to Port
R - Reset all events
Q - Leave sequence of events menu

Figure 6- 22. Sequence of events menu

When the "A" command is entered, the alarm sequence of events log is sent to your terminal. A typical alarm sequence of events display is shown in Figures 6-23 and 6-24. This is a two-page display; it stops at the end of each page, so you can view the information. When you're finished looking at the first page, press any key to view the second page.

When the "T" command is entered, the trip sequence of events log is sent to your terminal. A typical trip sequence of events display is shown in Figure 6-25. This is a one-page display.

Each action that causes a record to be stored in the RFL 9300's memory is called an "event." These include alarms, trips, and direct transfer trips. The RFL 9300's alarm sequence-of-events log can store five alarm events, and the trip sequence of events log can store five trip events. The five most recent of each event type will be stored; earlier events are cleared from the log as new events occur.

Each alarm event can store up to four alarms. Once an alarm event has begun, subsequent alarms can be added to that event until it contains four alarms. The event is ended when all the alarms are cleared.

The trip events will display all tripped phases. When a trip event has begun, subsequent phase trips will be added to that event. The event will end when all the trips are cleared.

Each event is time-tagged in hours, minutes, seconds and milliseconds (ms). The battery backed, real time clock that generates the time-tags is started at the factory before the RFL 9300 is shipped. The clock can be adjusted by the user in the field by using the RS-232 port. If IRIG-B is used, this clock will be automatically synchronized to the IRIG-B signal.

```
Alarm Event One:
   Alarm    1   34  SV Parallel Port
   Alarm    2   46  System Comms
   Alarm    3   no alarm
   Alarm    4   no alarm
   Start of First Alarm          06/19/95        10:37:04        340 ms
   End of Last Alarm             06/19/95        10:37:07        538 ms

Alarm Event Two:
   Alarm    1   46  System Comms
   Alarm    2   no alarm
   Alarm    3   no alarm
   Alarm    4   no alarm
   Start of First Alarm          06/13/95        09:55:43        332 ms
   End of Last Alarm             06/19/95        10:37:07        538 ms

Alarm Event Three:
   Alarm    1   34  SV Parallel Port
   Alarm    2   46 System Comms
   Alarm    3   no alarm
   Alarm    4   no alarm
   Start of First Alarm          06/13/95        09:55:14        648 ms
   End of Last Alarm             06/13/95        09:55:38        610 ms
 -- press any key --
```

Figure 6-23. Typical alarm sequence of events display – page 1

```
Alarm Event Four:
   Alarm    1   34  SV Parallel Port
   Alarm    2   46 System Comms
   Alarm    3   no  alarm
   Alarm    4   no  alarm
   Start of First Alarm          06/13/95        09:06:29        318 ms
   End of Last Alarm             06/13/95        09:06:35        040 ms

Alarm Event Five:
   Alarm    1   34  SV Parallel Port
   Alarm    2   46 System Comms
   Alarm    3   no  alarm
   Alarm    4   no  alarm
   Start of First Alarm          06/07/95        10:59:24        498 ms
   End of Last Alarm             06/07/95        10:59:28        906 ms

Current Time                     01/01/96        04:46:04        148 ms

9300-S>
```

Figure 6-24. Typical alarm sequence of events display – page 2

```
Trip Event One:
   Phase A Trip    Strong Feed
   Phase B Trip    Strong Feed
   Start of Event              05/09/95        11:10:17        234 ms
   End of Event                05/09/95        15:06:10        382 ms

Trip Event Two:
   User Forced Trip Event
   Start of Event              05/09/95        08:37:56        044 ms
   End of Event                05/09/95        11:09:39        768 ms

Trip Event Three:
   Phase C Trip
   Start of Event              05/08/95        17:22:47        320 ms
   End of Event                05/08/95        17:24:00        874 ms

Trip Event Four:
   3IO Trip
   Start of Event              05/08/95        17:13:05        782 ms
   End of Event                05/08/95        17:22:40        970 ms

Trip Event Five:
   DTT Sent
  Start of Event               05/08/95        16:50:03        716 ms
   End of Event                05/08/95        17:22:40        970 ms

Current Time                   06/19/95        11:20:10        664 ms
9300-S>
```

Figure 6-25. Typical trip sequence of events display – page 1

```
-001,   -002,   -069,   +062,   062
+027,   -001,   -002,   -001,   031
     :       :       :       :       :
     :       :       :       :       :
     :       :       :       :       :
+058,   -001,   -098,   -001,   062
-001    -128,   -065,   -001,   255
--Output Oscillography trip event

9300-S>
```

Figure 6-26. Typical Oscillography data table

6.5.10 VIEWING OSCILLOGRAPHY DATA

In addition to storing alarm and trip events, the RFL 9300 also stores oscillography data for the trip events, which can be viewed by the user. The stored oscillography data contains twelve cycles of all four measured trip currents which consist of six cycles of pre-trip data and six cycles of post trip data.

To view the raw oscillography data the user must first enter the sequence of events menu as shown in Figure 6-22. When the "O" command is entered, you will be prompted to enter the number of the trip event that you want to view (1-5). When the desired trip event number is entered, a table will be displayed which contains the raw oscillography data. A typical oscillography data table can be seen in Figure 6-26, which consists of five columns. From left to right, the columns contain Phase A data, Phase B data, Phase C data, 3I0 data, and the algorithm code.

To view the oscillograms, the raw oscillography data must be downloaded using a terminal emulation program and then plotted using a graphics program. The following example uses Microsoft Windows Terminal to download the oscillography data, and uses Microsoft Excel to plot the oscillography data. These instructions must be modified if other software packages are used.

6.5.11 DOWNLOADING AND GRAPHING AN OSCILLOGRAPHY RECORD

To download and graph an oscillography record, do the following:

1. Establish communication between the RFL 9300 and your PC or laptop using Microsoft Windows Terminal. When communication has been established the RFL 9300 will send the following prompt to your PC:

   9300>

2. Type "S" [Enter] to enter the sequence of events menu as shown in Figure 6-22.

3. Type "O" [Enter] to download the oscillography record from the RFL 9300 oscillography board to the PC or laptop.

4. Click on "TRANSFERS".

5. Click on "RECEIVE TEXT FILE".

6. Enter a new filename using the following format: XXXX.TXT. For example you can name the file OSC1.TXT. Then press the [ENTER] key.

7. Enter the # of the desired record and then press the [ENTER] key. The oscillography data table will be displayed as shown in Figure 6-26.

8. Click on "STOP" after the record is complete.

The oscillography record is graphed using Microsoft Excel. A diskette containing a Microsoft Excel macro is provided by RFL to perform this task. The diskette also contains a file with instructions on how to use the Microsoft Excel macro under the filename README.TXT. A typical oscillography data plot is shown in Figure 6-27.

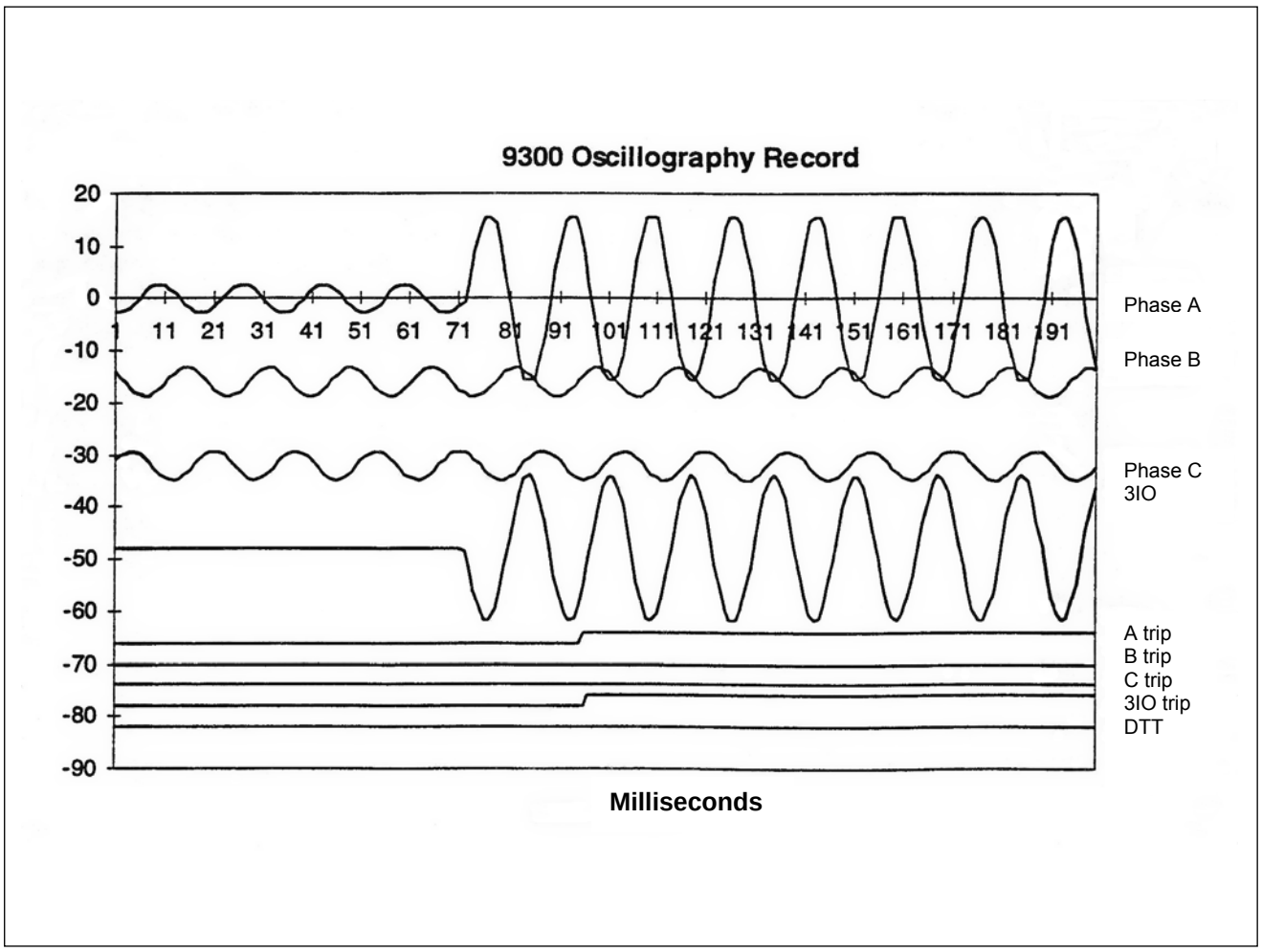


Figure 6-27. A typical oscillography data plot

6.5.12 PROGRAMMING THE RFL 9300 WITH A PC OR TERMINAL

You can use APRIL and your terminal to program the RFL 9300. All programming functions that are normally done using the keypad on the RFL 9300's display module can be done using a terminal. To use your PC or terminal to program the RFL 9300, use the "P" command.

Format: 9300>P [ENTER]

The "P" command tells the RFL 9300 to send a list of all programming commands to your terminal. Since using the programming commands will affect how the RFL 9300 operates, the "P" command is password-protected. When you enter the "P" command, the following prompt appears:

9300> enter password:

Either enter the super-user password ("CDLNRW") or the password that has been stored in the RFL 9300's memory. The RFL 9300 gives you three chances to enter the correct password. After the third incorrect password is entered, the RFL 9300 enters a lock-out mode. This mode will last for about five minutes, during which you will not be able to enter the programming mode.

If the proper password is entered, a programming menu similar to the one shown in Figure 6-28 will appear.

```
H - Display programming help
Q - Leave programming menu
SV - Save new settings
C - Change password (superuser authorization required)
D - Display present settings and parameter numbers
## - Edit this specific number parameter
9300-P> _
```

Figure 6-28. Typical programming menu

You are now in the programming mode, as indicated by the "9300-P>" prompt on your screen. You may now use the programming commands to re-program the RFL 9300. For more information on each programming command, refer to the paragraph numbers listed below.

Programming Command	Meaning	Para.
H	Display programming help	6.5.12
Q	Leave programming menu	6.5.12.4
SV	Save new settings	6.5.12.3
C	Change password	6.5.12.1
D	Display current settings and parameter numbers	6.5.12.2

6.5.12.1 CHANGING THE PASSWORD

You can use the "C" command to change the second password that can be used to enter the programming mode.

Format: 9300-P>C [ENTER]

When you enter the "C" command, the RFL 9300 sends the following prompt to your terminal:

enter super-user:

Enter the super-user password ("CDLNRW"), and then press **[ENTER]**. The following prompt will appear:

Current password is (current password)
enter new password:

Enter the new password, and then press **[ENTER]**. The following prompt will appear:

repeat new password:

Enter the new password again, and then press **[ENTER]**. The following prompt will appear:

password modified

The new password is now stored in the RFL 9300's non-volatile RAM memory.

6.5.12.2 DISPLAYING PARAMETER SETTINGS

To view a list of all current parameter settings, use the "D" command.

Format: 9300-P>D [ENTER]

When you enter the "D" command, the RFL 9300 sends a list of all current parameter settings to your terminal. A typical parameter settings list for a three-terminal system is shown in Figure 6-29.

9300-P>D

#	PARAMETER	SETTING	#	PARAMETER	SETTING
020	Phase Bias	1.500 Amps	021	Ground Bias	1.500 Amps
022	Bias Control	Disable	023	Ground Delay	Enable
024	Bias/Ground Dly	.05/.05 sec	025	F.D. Phase	8.0 Amps
026	F.D. Ground	1.0 Amp	027	Backup (1)	Enable
028	Phase O/C Bkup	31.875 Amps	029	Ground O/C Bkup	31.000 Amps
030	Phase TOC (2)	Disable	031	Ph TOC Pickup	N/A
032	PhTOC Curve	N/A	033	Ph TOC Dial	N/A
034	Ground TOC (3)	Disable	035	Gd TOC Pickup	N/A
036	Gd TOC Curve	N/A	037	Gd TOC Dial	N/A
038	Overhd/Undergd	Overhead	040	Stub Bus (1)	Inactive
041	Comms Alm Dly	Disable	044	Beeper	Disable
046	Transmit Addr 1	4079	047	Transmit Addr 2	4075
050	Guard/Trip	Disable	120	Current Date	08/16/00
121	Current Time	09:29:27			
122	Reset Disp. Alrm	No	140	Single Pole	Active
141	Slctv Pole RL	Disable	145	Trip Release	CS+TRIP
999	System Label	Gen1			

9300-P>

Figure 6-29. Typical parameter settings list for a three-terminal system

NOTE
If parameter No. 030 is disabled, then parameter numbers 031, 032 and 033 will display N/A (not applicable).
If parameter No. 034 is disabled, then parameter numbers 035, 036 and 037 will display N/A (not applicable).

To re-program any of the values shown on the programming menu, type in the number in the "#" column, and then press **[ENTER]**. The parameter will be displayed, with information about its setting below it. Type in the new setting, and then press **[ENTER]**.

EXAMPLE:

To change the phase bias setting from 1.5 amperes to 3.0 amperes, type in the following:

9300-P> 20 [ENTER]

The Phase Bias parameter will be displayed, with information about its setting below it.

020 Phase Bias 1.5 amps
[1.0:8.0](in 0.5 increments)> _

The first number in the brackets indicates the lowest value allowed for this parameter; in this case, 1.0. The second number is the highest allowed value; in this case, 8.0. The statement in the parentheses indicates the incremental steps permitted; in this case, 0.5 (1.5, 2.0, 2.5, etc).

To set the phase bias to 3.0 amperes, type in "3.0," and then press **[ENTER]**. The Phase Bias parameter will be re-displayed, set to the new value. Settings must be saved in accordance with paragraph 6.5.12.3, or they will be lost.

020 Phase Bias 3.0 amps

EXAMPLE:

The RESET DISP. ALRM parameter is usually set to "NO." This is the reset for the display controller alarm and LED signal. It is the same as pressing the RESET switch on the front of the display controller. To reset the RFL 9300 using your terminal, type in the following:

9300-P> 122 [ENTER]

The Reset Disp. Alrm parameter will be displayed, with information about its setting below it.

122 Reset Disp. Alrm No
[Y:N]> _

Type in "Y," and then press **[ENTER]**. The Reset Disp. Alrm parameter will be re-displayed, set to the new value.

122 Reset Disp. Alrm Yes

The display controller alarms will be reset when the parameter changes are saved, and the target indicators will be turned off. If a trip is active when the reset is attempted, the reset will be ignored. (See para. 6.5.12.3 for more information on saving parameters.)

The "System Label" is an identifier that appears on the second line of the APRIL command list. This list appears each time you issue an "H" command when you are not in the Programming Mode. In the screens shown in this manual, the System label has been set to "SUBSTATION 12."

EXAMPLE:

To change the System Label, type in the following:

9300-P> 999 [ENTER]

The System Label parameter will be displayed, with information about its setting below it.

999 System Label SUBSTATION 12
[any string]> _

Type in whatever you want the new System Label to be. It can be any combination of letters or numbers up to 25 characters long. When you are finished, press the **[ENTER]** key. The System Label parameter will be re-displayed, set to the new value.

999 System Label SUBSTATION 12A

6.5.12.3 SAVING NEW SETTINGS

The "SV" command saves any new settings you made while in the programming mode:

Format: 9300-P>SV [ENTER]

The "SV" command tells the RFL 9300 to store all the changes in its non-volatile RAM memory. Once the changes are stored, the "9300-P>" prompt will re-appear.

Before you enter the "SV" command, the RFL 9300 operates according to the old parameter settings. Once the "SV" command is entered, the new settings will be in effect.

The new parameter settings can be verified by re-issuing the "D" command to display the parameter settings list. (For more information on the "D" command, go to para. 6.5.5)

6.5.12.4 LEAVING THE PROGRAMMING MODE

Whenever you are finished programming the RFL 9300, use the "Q" command:

Format: 9300-P>Q [ENTER]

The "Q" command tells the RFL 9300 to leave the programming mode and return to the normal "9300>" prompt. If you changed any setting while in the programming mode, be sure to use the "SV" command described above to save the changes before invoking the "Q" command; otherwise, your changes will be lost.

6.5.13 RETURNING TO NORMAL RFL 9300 OPERATION

Once you are finished accessing the RFL 9300 using APRIL, make sure you have returned to the "9300>" prompt:

1. If you were in the Programming Mode, press the **[Q]** and **[ENTER]** keys to return to the "9300>" prompt.

2. If you were in the Update Mode, press the **[X]** and **[ENTER]** keys to return to the "9300>" prompt.

When the "9300>" prompt is displayed, simply disconnect your PC or terminal from the RFL 9300's RS-232 connector. If you accessed the RFL 9300 through an RFL 9660 Digital Switch, type in the deselect code (normally "BYE") to deselect the port, and then enter the "Q" command to terminate the session. (Refer to the RFL 9660 Instruction Manual for more information.)

6.6 RFL 9300 ADDRESSING

6.6.1 TWO-TERMINAL ADDRESSING

In two-terminal systems RFL 9300s are installed in pairs, where one unit is installed at each end of a protected power line. Some RFL 9300 installations may have more than one pair of 9300s connected to a common network. The RFL 9300 has an addressing feature which insures that the local 9300 will only communicate with its corresponding remote 9300. The addressing feature can be enabled or disabled by the user depending on the type of installation. An advantage of disabling the addressing feature is to reduce traffic on the communication line between the local and remote units. Figure 6-30 is an example of an installation where addressing must be used. In this example, addressing will insure that RFL 9300 local #1 will only communicate with RFL 9300 remote #2, and that RFL 9300 local #2 will only communicate with RFL 9300 remote #2. Figure 6-31 shows examples of two installations where addressing is not required. As a general rule, if there is a possibility of the 9300 communications channel being disconnected, re-routed or looped back on itself, then addressing should be used.

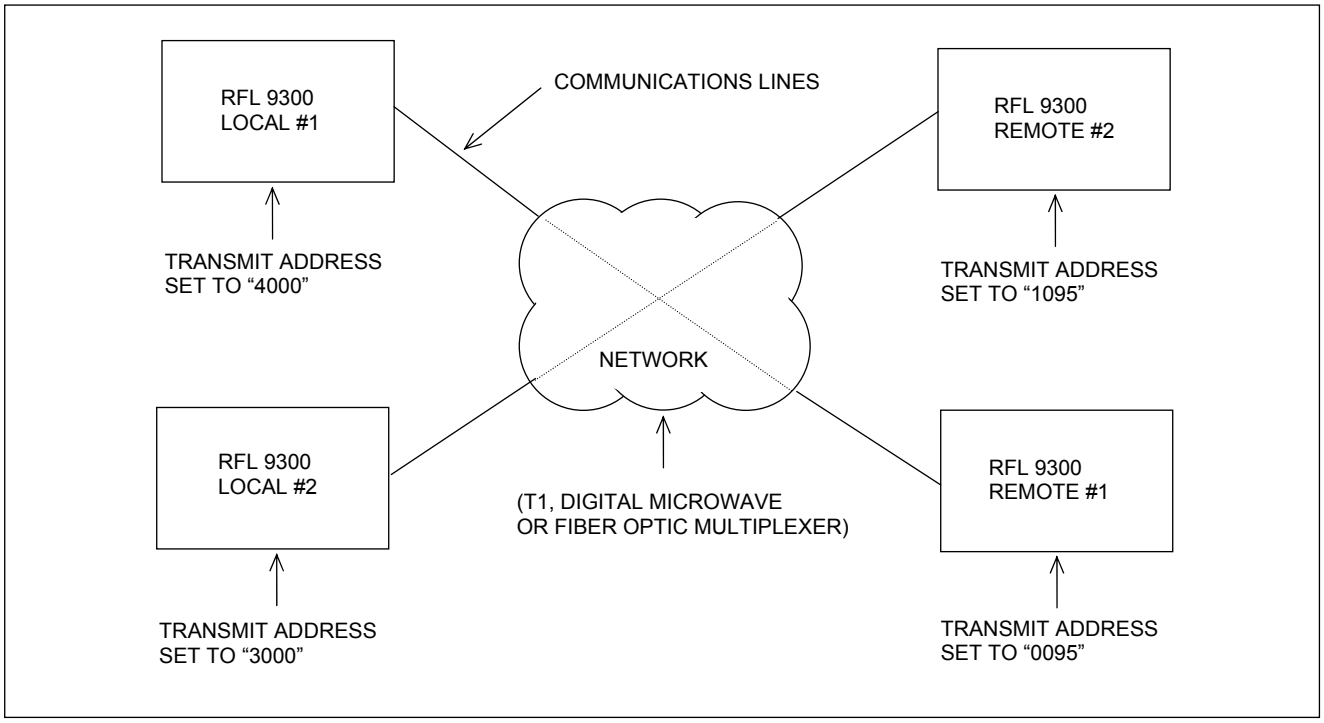


Figure 6-30. A typical two-terminal installation where addressing is required

RFL 9300 transmit addresses are user selectable from “0016” to “4079” and are set to different values at the local and remote units. The sum of the local and remote addresses must equal 4095. For example, if the local address is set to “4000” then the remote address must be set to “0095”. The address programmed at the local unit is transmitted to the remote unit for address verification. If the correct address is not verified, an address alarm will be displayed on the 9300 front panel.

When addressing is not required, the user can disable the addressing feature of the RFL 9300 by setting the transmit addresses of both the local and remote 9300s to “0000”. For more information, refer to the start-up procedure at the beginning of this section.

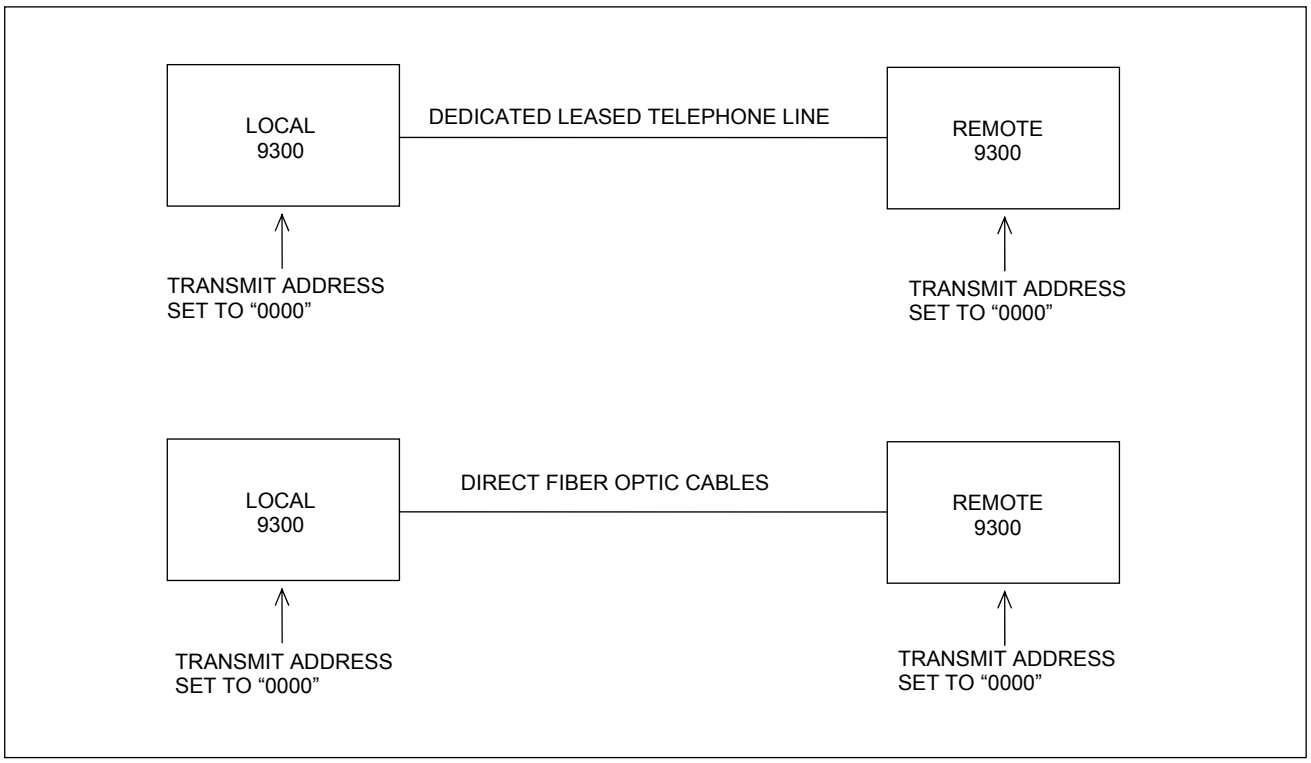


Figure 6-31. A typical two-terminal installation where addressing is not required

6.6.2 THREE-TERMINAL ADDRESSING

Three-terminal addressing is similar in principle to two-terminal addressing as described in para. 6.6.1 with the exception that the units are installed in sets of three, where one unit is installed at each leg of a protected power line. One of the units is arbitrarily referred to as the local unit and the other two are referred to as remote 1 and remote 2. Figure 6-32 shows a typical installation using three-terminal addressing. Note that two transmit addresses (TX1 and TX2) must be programmed at each terminal. This means that a total of six transmit addresses must be programmed for a three-terminal installation. There are a few simple rules that must be followed when addressing a three-terminal installation:

1. Addresses under 0016 are not allowed.
2. The TX1 and TX2 addresses must be different at each site.
3. The TX1 address of a given site and the TX1 address of its “mate” must add up to 4095.

For step-by-step three-terminal addressing instructions, refer to para. 6.3.2.

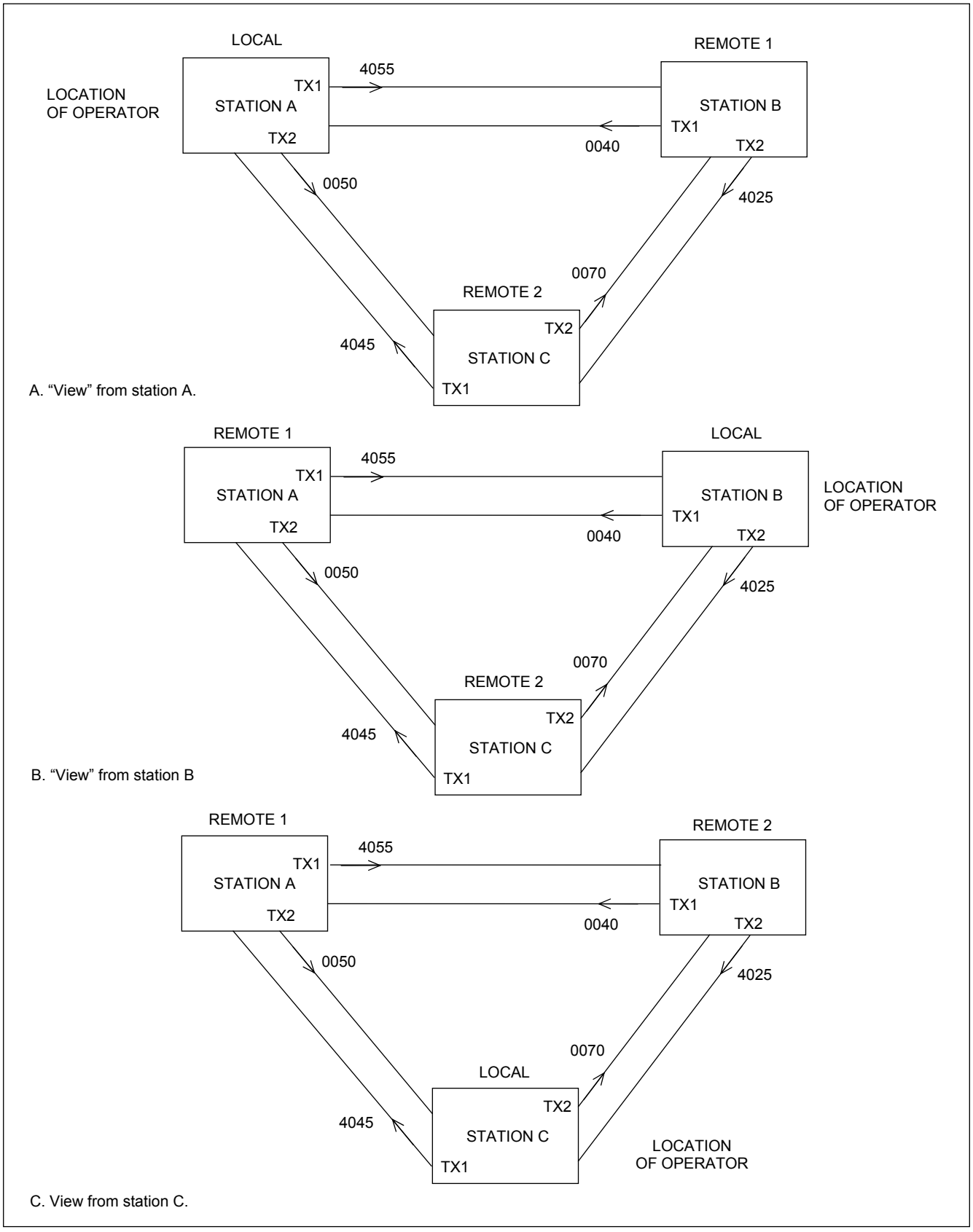


Figure 6-32. Typical RFL 9300 three-terminal addressing scheme

6.7 DESCRIPTION OF INSTANTANEOUS OVERCURRENT BACKUP TRIP ALGORITHM and INVERSE TIME OVERCURRENT BACKUP TRIP ALGORITHM

The 9300 now implements an Inverse Time Overcurrent Backup Trip Algorithm (for Phase and Ground) in addition to the Instantaneous Overcurrent BackupTrip Algorithm (for Phase and Ground). These trip algorithms are used only when the relay is in Backup Mode.

6.7.1 INSTANTANEOUS OVERCURRENT BACKUP TRIP ALGORITHM

Instantaneous Overcurrent Backup is always active in Backup Mode. This algorithm is implemented in the relay using parameter #28 for phase and #29 for ground. The range of values for Phase Overcurrent Backup (PH OC BU) is 6.0 amps to 31.875 amps. The range of values for Ground Overcurrent Backup (G OC BU) is 1.0 amps to 31 amps.

This instantaneous overcurrent function will enable trip during backup mode operations when two conditions are met. First if the current exceeds the setting entered and second if the phase controller executing the overcurrent algorithm has an active fault detector and there is at least one more fault detector active at the local station.

6.7.2 INVERSE TIME OVERCURRENT BACKUP TRIP ALGORITHM

The Inverse Time Overcurrent Backup Trip Algorithm for phase and ground will be active during Backup Mode only if the user has enabled the feature using parameter #30 for phase and/or #34 for ground (3I0). If no further parameters are selected, the Inverse Time Overcurrent Backup Trip Algorithm will use default settings for the pickup value.

The phase controller executing the Inverse Time Overcurrent Backup Trip Algorithm will enable trip if the current remains above the pickup level until the TOC timer times out even without an active fault detector.

THIS IS A FUNDAMENTAL CHANGE IN CCS OPERATION WHICH WOULD OTHERWISE REQUIRE TWO ACTIVE FAULT DETECTORS TO ENABLE TRIP IN EITHER THE INSTANTANEOUS OVERCURRENT BACKUP MODE ALGORITHM OR IN THE PERMISSIVE TRIP ALGORITHM.

6.7.3 SETTING UP THE INVERSE TIME OVERCURRENT FUNCTION

The inverse time overcurrent feature can be enabled using the front panel display/keypad or via April Software from a terminal or personal computer.

The Phase Time Overcurrent function is set for all three Phase Controllers, Phase A Phase B and Phase C simultaneously as a group.

The Ground Time Overcurrent function for the 3I0 Controller is set separately and is completely independent of the status or settings of the Phase Time Overcurrent function.

This allows the user to enable either the ground or phase time overcurrent functions separately or use them in conjunction with each other with the same or different pickup values, dial settings and curves.

6.7.3.1 SETTING THE PHASE TIME OVERCURRENT PARAMETERS

The operator must enter the following parameters in programming mode:

1. Parameter #30 PH TOC	set to ENABLE.
2. Parameter #31 P PICKUP	set to the pickup value.
3. Parameter #32 PH CURVE	set to selected curve.
4. Parameter #33 PH DIAL	set to desired time dial setting.

The range of pickup values is 0.5 amps to 31.875 amps in 0.125 amp steps.

The operator may select from eight curves arranged in two groups.
There are 4 USA curves and 4 IEC curves.

USA CURVES	IEC CURVES
USA1 - Moderately Inverse	IEC1 - Standard Inverse
USA2 - Inverse	IEC2 - Very Inverse
USA3 - Very Inverse	IEC3 - Extremely Inverse
USA4 - Extremely Inverse	IEC4 - Long Time Backup

Each curve can have one of eleven different time dial settings.
The time dial settings available for the USA curves are: 0.5, 1, 2 , 3, 4, 5, 6, 8, 10, 12 and 15.

The time dial settings available for the IEC curves are: 0.05, 0.1, 0.2 , 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9 and 1.0 .

Note that the reset function for this trip algorithm is instantaneous. The reset time is not programmable by the operator.

6.7.3.2 SETTING THE GROUND TIME OVERCURRENT PARAMETERS

The operator must enter the following parameters in programming mode:

1. Parameter #34 GND TOC	set to ENABLE
2. Parameter #35 G PICKUP	set to the pickup value.
3. Parameter #36 GND CURVE	set to selected curve.
4. Parameter #37 GND DIAL	set to desired time dial setting.

The range of pickup values is 0.5 amps to 31 amps in 0.125 amp steps.

The operator may select from eight curves arranged in two groups.
There are 4 USA curves and 4 IEC curves.

USA CURVES	IEC CURVES
USA1 - Moderately Inverse	IEC1 - Standard Inverse
USA2 - Inverse	IEC2 - Very Inverse
USA3 - Very Inverse	IEC3 - Extremely Inverse
USA4 - Extremely Inverse	IEC4 - Long Time Backup

Each curve can have one of eleven different time dial settings.
The time dial settings available for the USA curves are: 0.5, 1, 2 , 3, 4, 5, 6, 8, 10, 12 and 15.

The time dial settings available for the IEC curves are: 0.05, 0.1, 0.2 , 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9 and 1.0 .

Note that the reset function for this trip algorithm is instantaneous. The reset time is not programmable by the operator.

The TOC status will be supplied to the phase controllers using the Phase Time Overcurrent Status Message (63H) and to the 3I0 controller using the 3I0 Time Overcurrent Status Message (64H) .

Each curve has a reference time dial setting stored in a lookup table. The reference dial setting for each USA curve (USA1-USA4) is the 0.5 setting. The reference setting for each IEC curve (IEC1-IEC4) is the 0.05 setting. The remaining dial settings are calculated from the reference settings. Each point on these curves represents a multiple of pickup (M) that has a trip delay time constant associated with it. The following multiples of pickup, M, are used for each dial setting:

1.5 , 2 through 30 (integer values only)

The time constant selected from a lookup table is a 16 bit value with each bit representing 2 milliseconds. The maximum time constant allowed for any dial setting is 65530 * 2 ms = 131.06 seconds. Any dial setting /M combination that exceeds this will be truncated at the maximum value of 131.06 seconds. Refer to the TOC Curves shown in Figures 6-33 through 6-40.

The contents of a 16 bit register will be used to determine if the input current has exceeded the pickup value. This register holds the integral sum of the input current samples over the previous 8 ms. The value represents a running 8 ms average of the input current. If the input current exceeds the pickup point the TOC timer will be started.

From this point on the TOC timer will be updated at 2 ms intervals. Using the true integral value, buffers the overcurrent algorithms from the effects of current spikes and glitches, but does not eliminate the DC offset present in fault current waveforms. However this is alleviated to some degree as the M value integer is recalculated on a 16 ms basis for as long as the TOC timer remains active. This will insure the time delay is adjusted to the fault current changes. Once this calculation is completed, the time delay is obtained from the selected dial setting curve and stored in a 16 bit TOC delay timer register.

If 1<M<1.5 the TOC timer updates will stop but the timer will not reset. If M calculates to a value < 1.0 the function will terminate and the TOC timer will instantaneously reset to 0 (reset function).

If the fault current continues to be detected until the time recorded by the TOC timer exceeds the delay time stored in the delay timer, a trip signal will be issued.

6.8 TIME-OVERCURRENT CURVE EQUATIONS

Both US and IEC time-overcurrent curves are provided in the RFL 9300 relay. Use the PROGRAM mode to select the curve characteristics you desire. These time curve equations are valid for all time-overcurrent elements. Plots showing operating time versus multiples of pickup current are shown on the following pages. The equations and curves apply while the product of the multiples of pickup and pickup setting is less than $32 \times I_{(nominal)}$ amps, secondary.

6.8.1 EQUATIONS FOR US CURVES

t_M = curve operating time in seconds

TD = time dial setting

M = multiples of pickup. For curve operating time (t_M), M > 1.

Curve USA1: Moderately Inverse - See Figure 6-33

$$t_M = TD \left[0.0226 + 0.0104/(M^{0.02} - 1) \right]$$

Curve USA2: Inverse - See Figure 6-34

$$t_M = TD \left[0.180 + 5.95/(M^2 - 1) \right]$$

Curve USA3: Very Inverse - See Figure 6-35

$$t_M = TD \left[0.0963 + 3.88/(M^2 - 1) \right]$$

Curve USA4: Extremely Inverse - See Figure 6-36

$$t_M = TD \left[0.0352 + 5.67/(M^2 - 1) \right]$$

6.8.2 EQUATIONS FOR IEC CURVES

t_M = curve operating time in seconds

TD = time dial setting

M = multiples of pickup. For curve operating time (t_M), M > 1.

Curve IEC1: Standard Inverse - See Figure 6-37

$$t_M = TD\ [\ 0.14/(M^{0.02} - 1)\ ]$$

Curve IEC2: Very Inverse - See Figure 6-38

$$t_M = TD\ [\ 13.5/(M - 1)\ ]$$

Curve IEC3: Extremely Inverse - See Figure 6-39

$$t_M = TD\ [\ 80.0/(M^2 - 1)\ ]$$

Curve IEC4: Long Time Backup - See Figure 6-40

$$t_M = TD\ [\ 120.0/(M - 1)\ ]$$

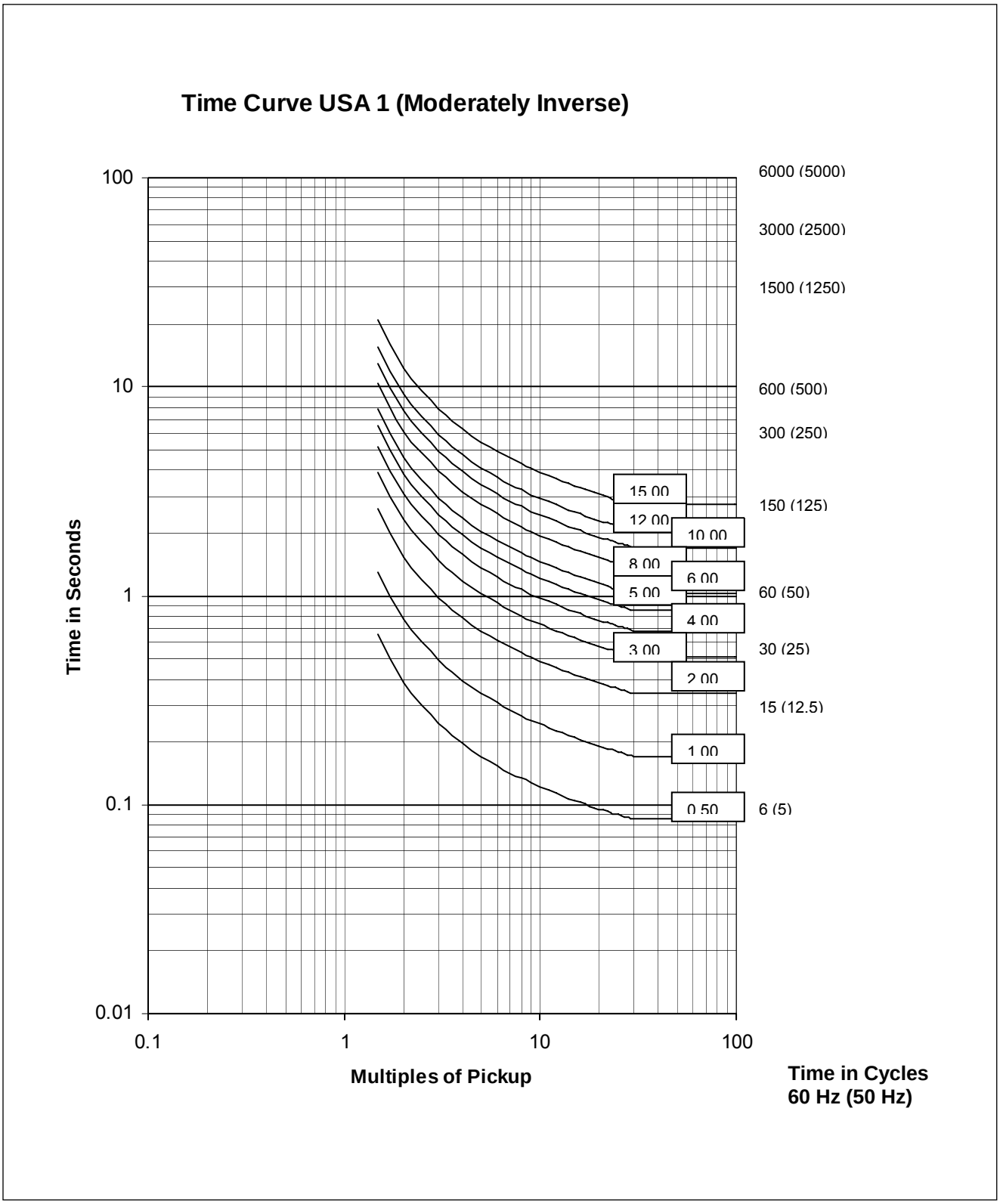


Figure 6-33. Time Curve USA 1

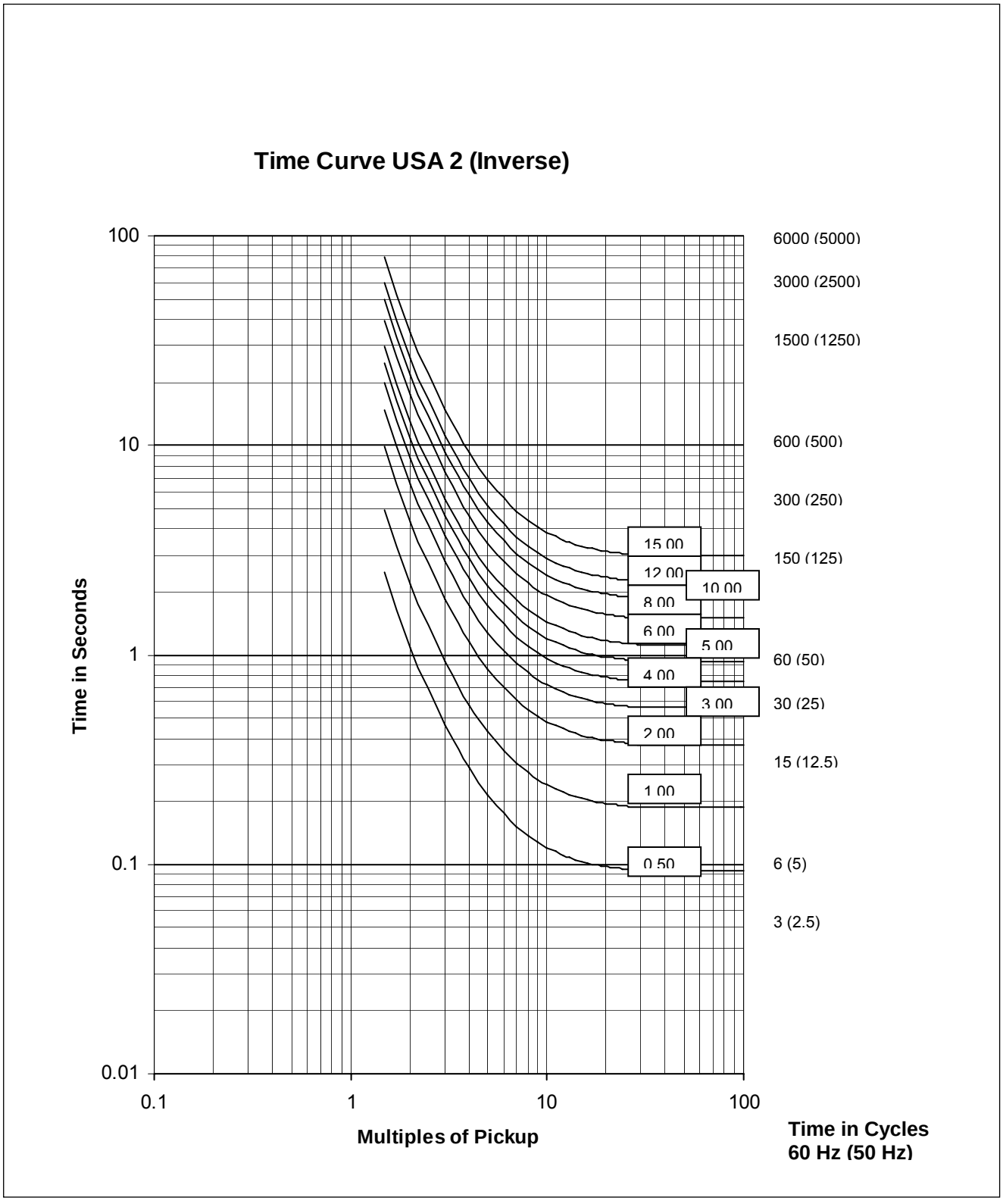


Figure 6-34. Time Curve USA 2

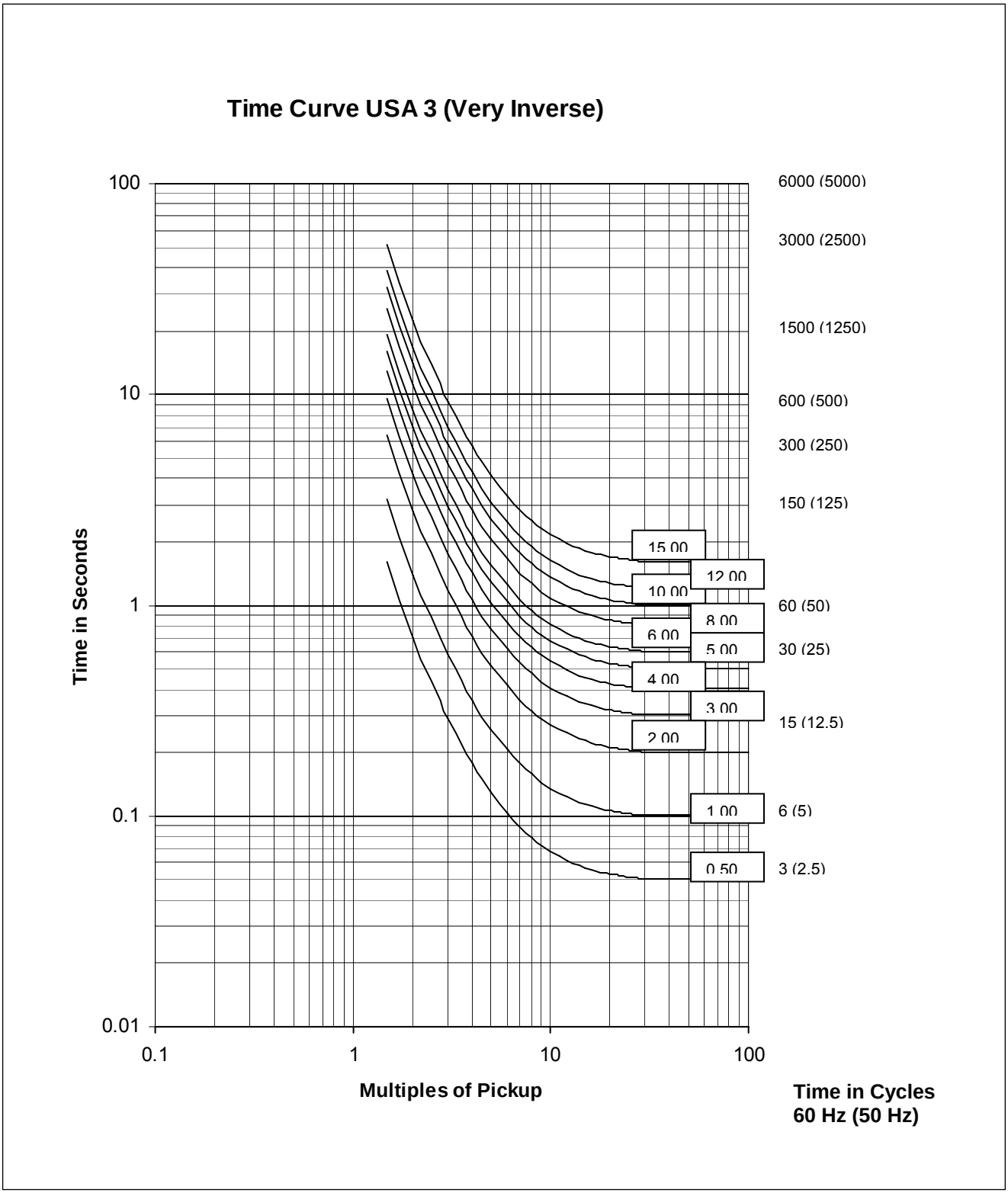


Figure 6-35. Time Curve USA 3

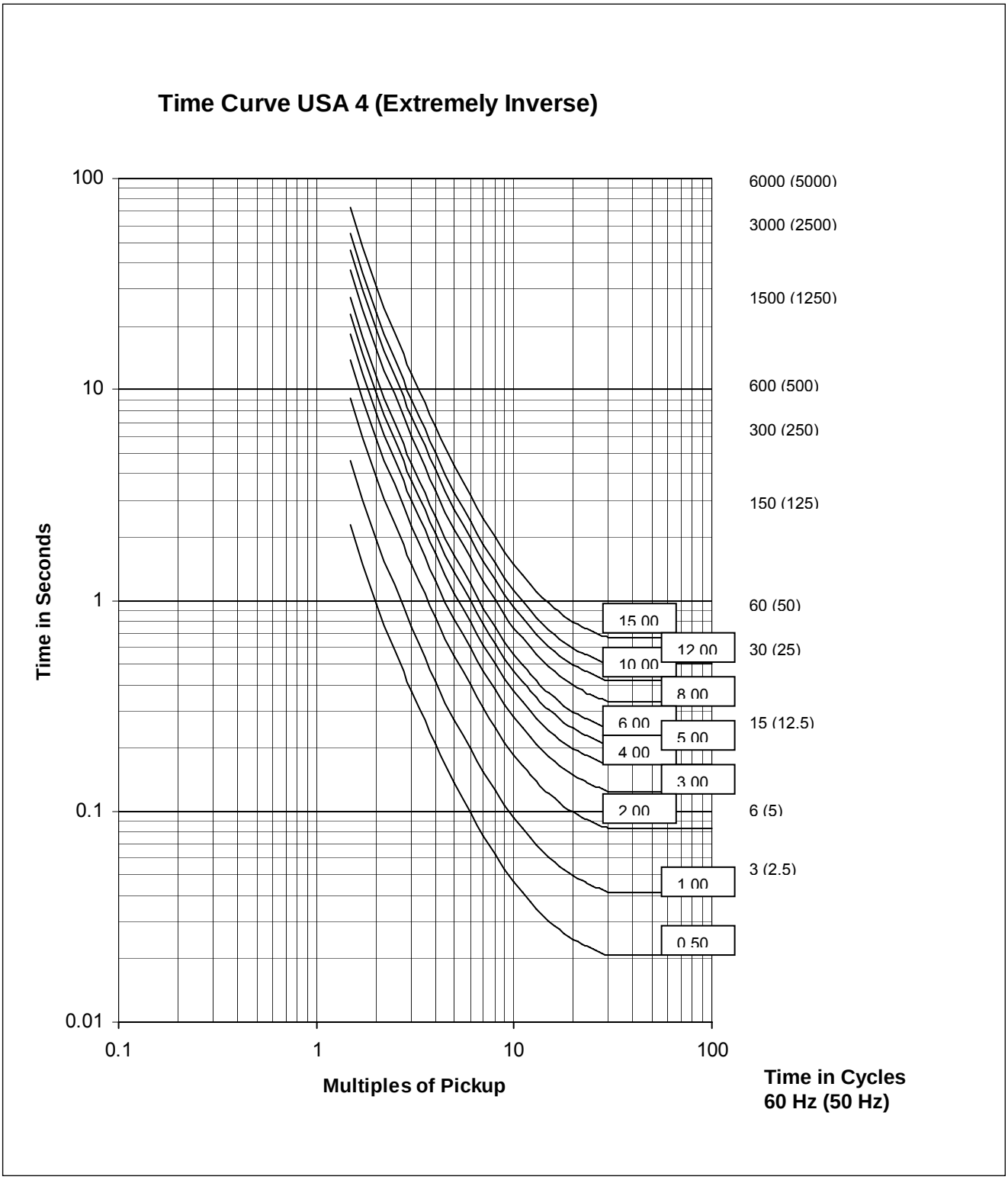


Figure 6-36. Time Curve USA 4

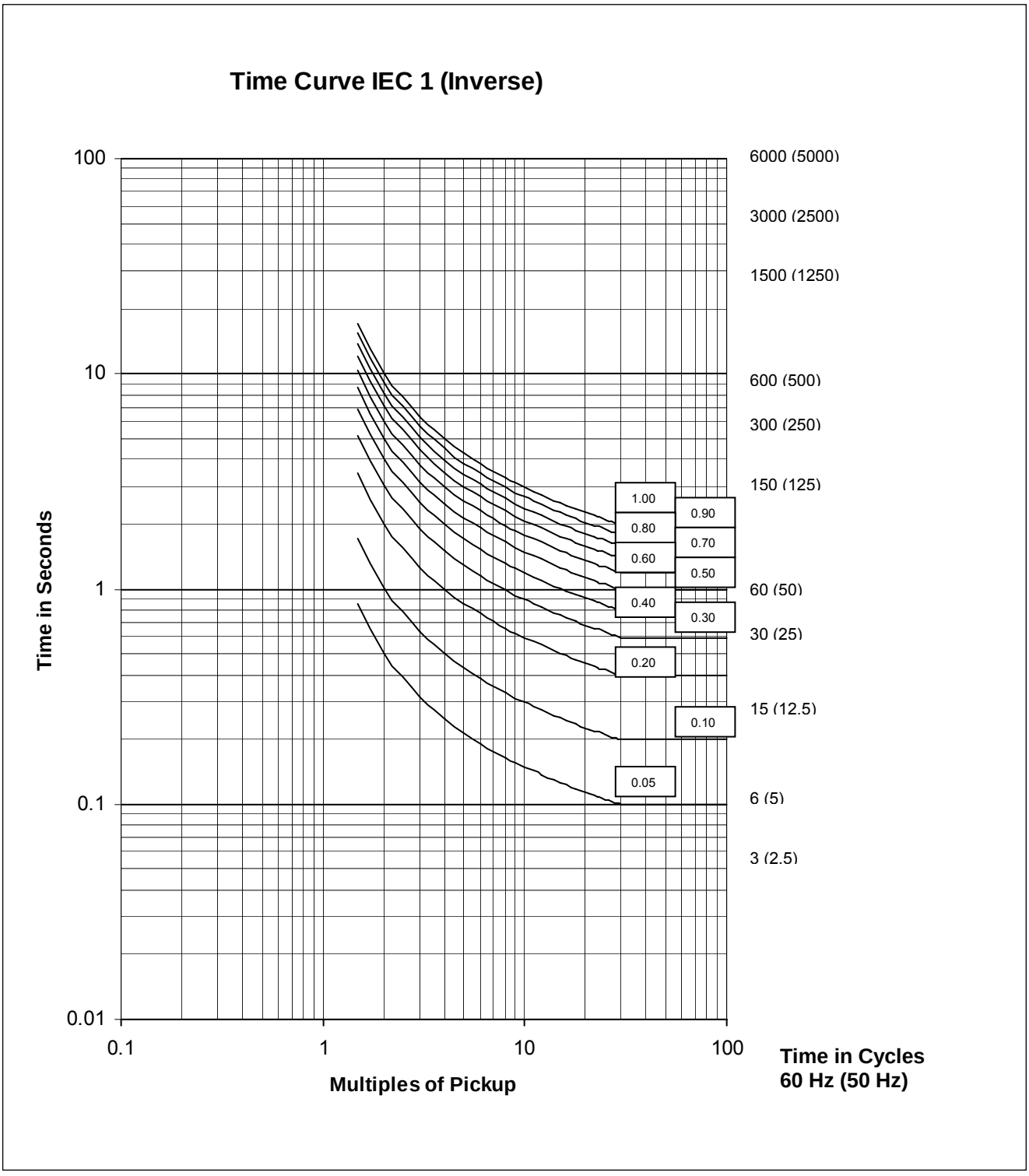


Figure 6-37. Time Curve IEC 1

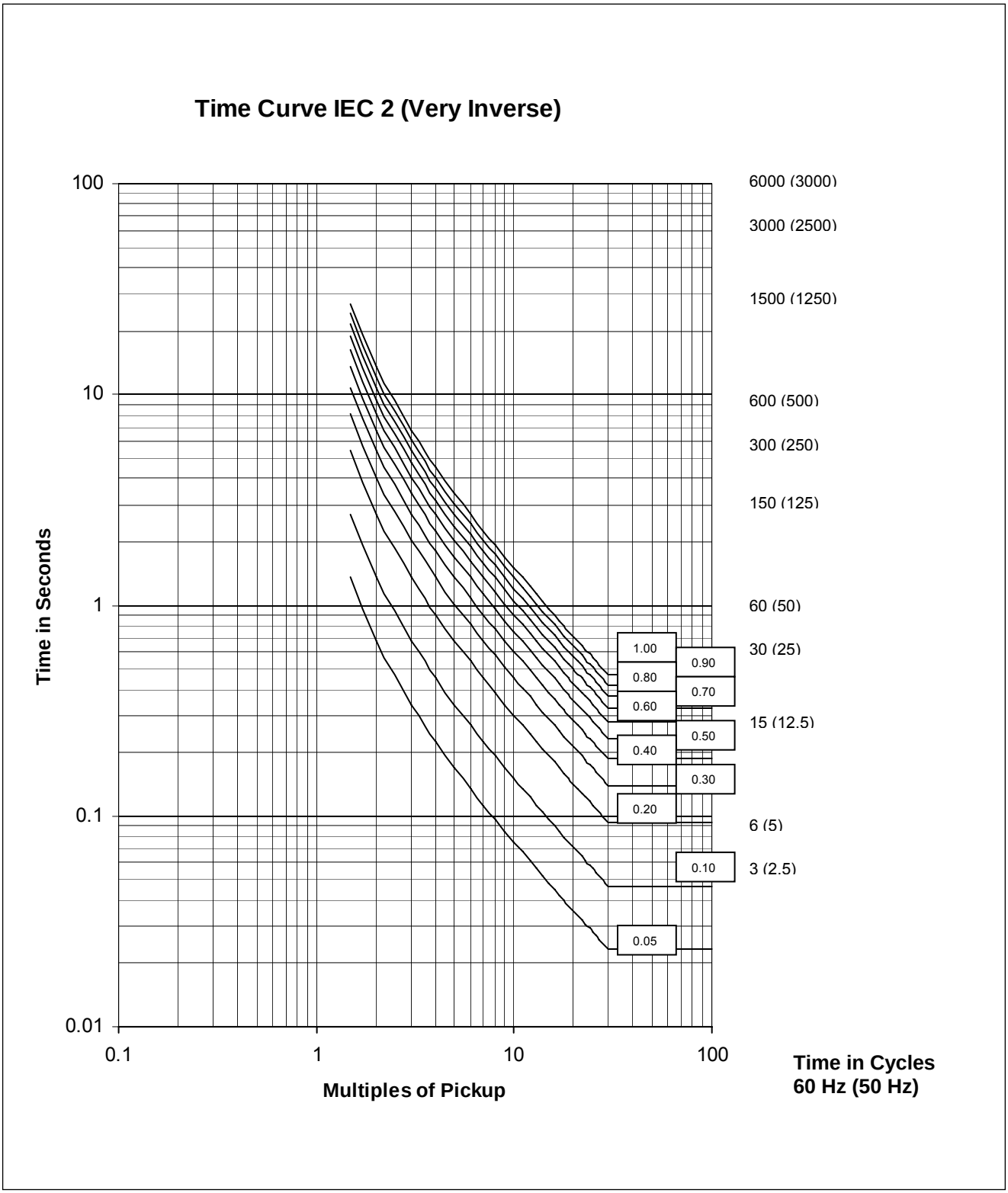


Figure 6-38. Time Curve IEC 2

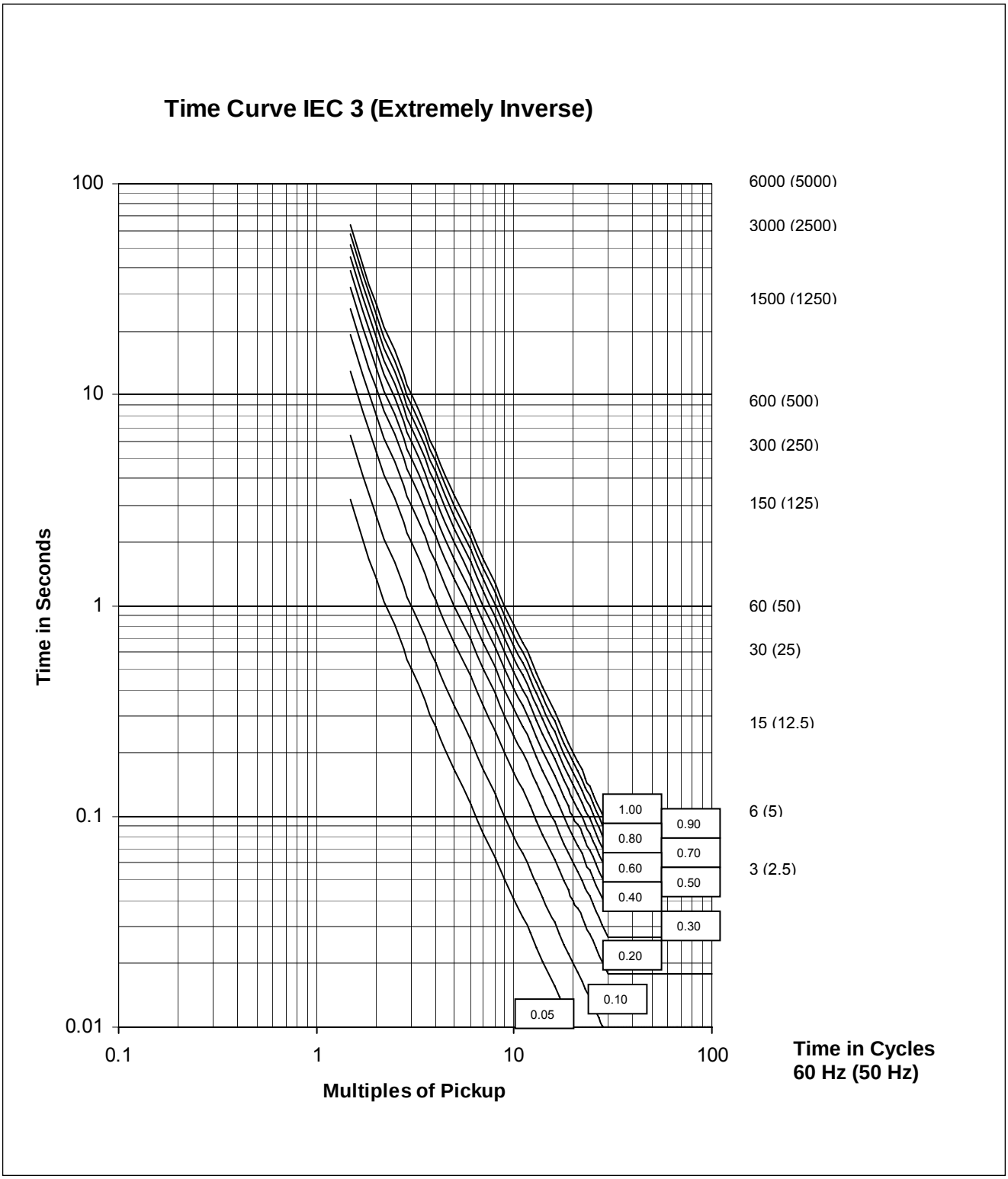


Figure 6-39. Time Curve IEC 3

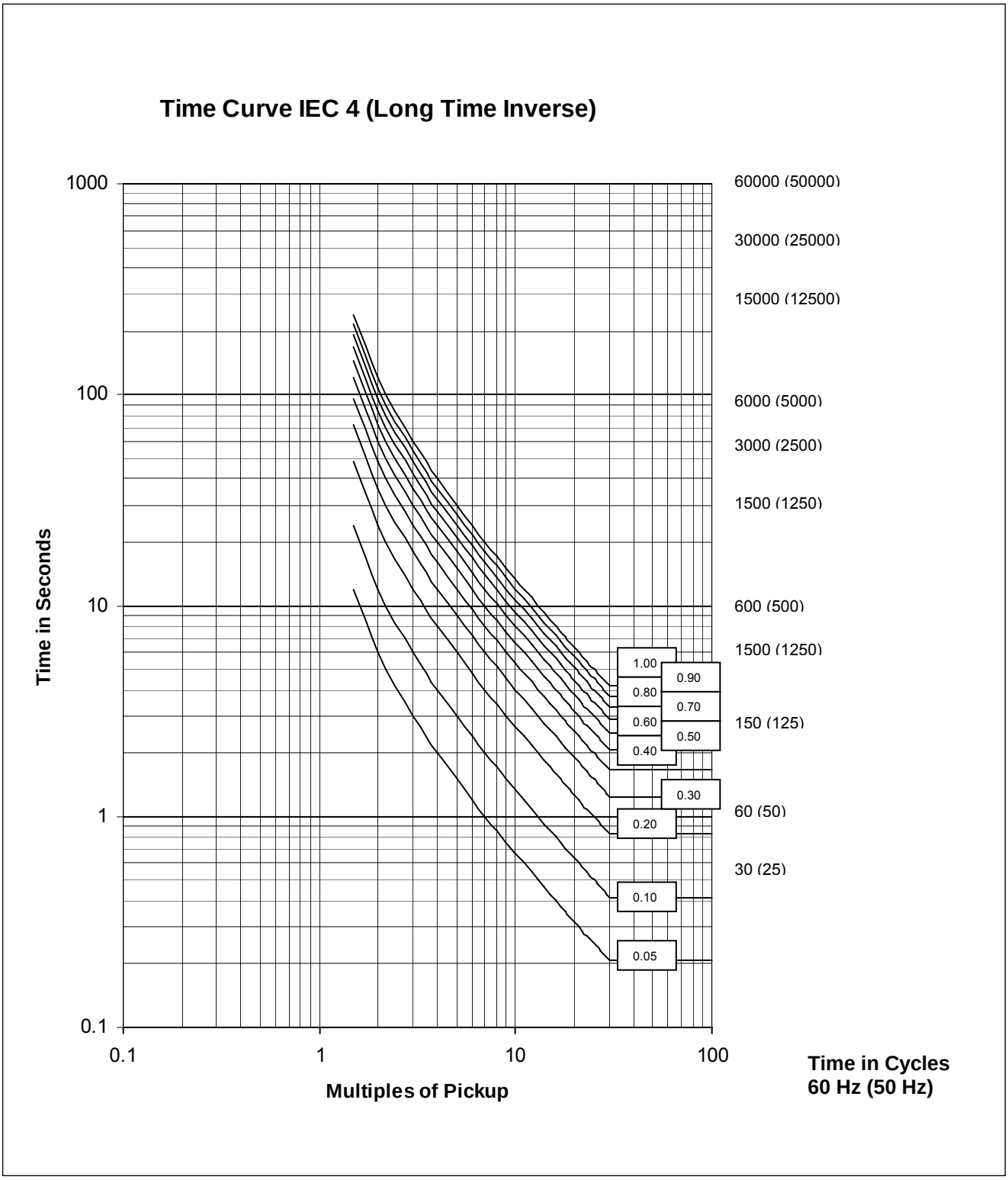


Figure 6-40. Time Curve IEC 4

SECTION 7: LABORATORY ACCEPTANCE TESTS

NOTE

Before performing any of the tests described in this section, be sure that you have read and understood the procedures in Section 6 of this manual. In particular, review the information on the READ mode and PROGRAM mode. These modes will be used many times during the procedures in this section

7.1 INTRODUCTION

This section contains procedures for testing two 9300 relays that are connected back-to-back. It is also possible to perform some tests on a single RFL 9300 that is communicating with itself (its transmitter connected to its receiver). These single-relay tests will be described in Section 8 of this manual.

NOTE

Three terminal units are to be converted to two terminal operation for Laboratory and Single Relay tests.

7.2 EQUIPMENT REQUIREMENTS

The following equipment is required to perform back-to-back testing:

1. A Volt-Ohm meter.
2. A dc voltage source capable of supplying either 48 Vdc or 125 Vdc, depending upon the power supplies installed in the RFL 9300.
3. A dc current source that can provide at least 0.4 amperes to drive two 0.2A dc sense circuits.
4. A 60-Hz, single-phase ac current source that can supply up to 15 amperes.
5. The following item is required for 9300 relays equipped with modem modules:
    a. Two twisted pairs of wire several feet long.
6. The following items are required for 9300 relays equipped with direct digital interface modules: (See Figure 7-1)
    a. An RFL DCE emulator (RFL part No. 105880).
    b. A +5Vdc power supply for the RFL DCE emulator.
    c. Two RS-449 cable assemblies used to connect the direct digital interface module to the RFL DCE emulator (RFL part No. 302196-X or equivalent).

7. The following items are required for 9300 relays equipped with fiber optic modules:

    a. Two fiber optic patchcords.

8. The following items are required for 9300 relays equipped with short haul fiber interface modules: (See Figure 7-1)

    a. Two Fiber Service Units. (RFL part No. 105075-X)

    b. Four fiber optic patchcords.

    c. An RFL DCE emulator (RFL part No. 105880).

    d. A +5Vdc power supply for the RFL DCE emulator.

    e. Two RS-449 cable assemblies used to connect the fiber service units to RFL DCE emulator (RFL part No. 302196-X or equivalent).

9. The following items are required for 9300 relays equipped with G.703 modules:

    a. Two twisted pairs of wire several feet long.

7.3 SYSTEM SETUP

Use the following procedure to prepare for the laboratory acceptance tests:

1. Verify that the Alarm I/O module is configured for your station battery voltage, or system damage may result. Refer to paragraph 21.2 for Alarm I/O module strapping instructions.

2. Connect the communications transmitters and receivers of the two RFL 9300s, in accordance with Figure 7-1.
    RFL 9300s with modems will require two twisted pairs.
    RFL 9300s with direct digital modules will require two RS-449 cables and a DCE emulator.
    RFL 9300s with fiber optic modules will require two fiber patchcords.
    RFL 9300s with short haul fiber interfaces will require a DCE emulator, two fiber service units, two RS-449 cables and four fiber optic patchcords.
    RFL 9300s with G.703 modules will require two twisted pairs.

3. Start up the two RFL 9300s, using the procedures given in Section 6 of this manual.
    Both RFL 9300s should be in the STANDBY mode, with two moving dots on the display and no alarm indications.

4. Using the READ display mode, verify that the delay in the communications link is normal.
    The PINGPONG value should read about 18 ms for modem versions, or 4 ms for direct digital or fiber versions.

>> text continues on page 7-4 <<

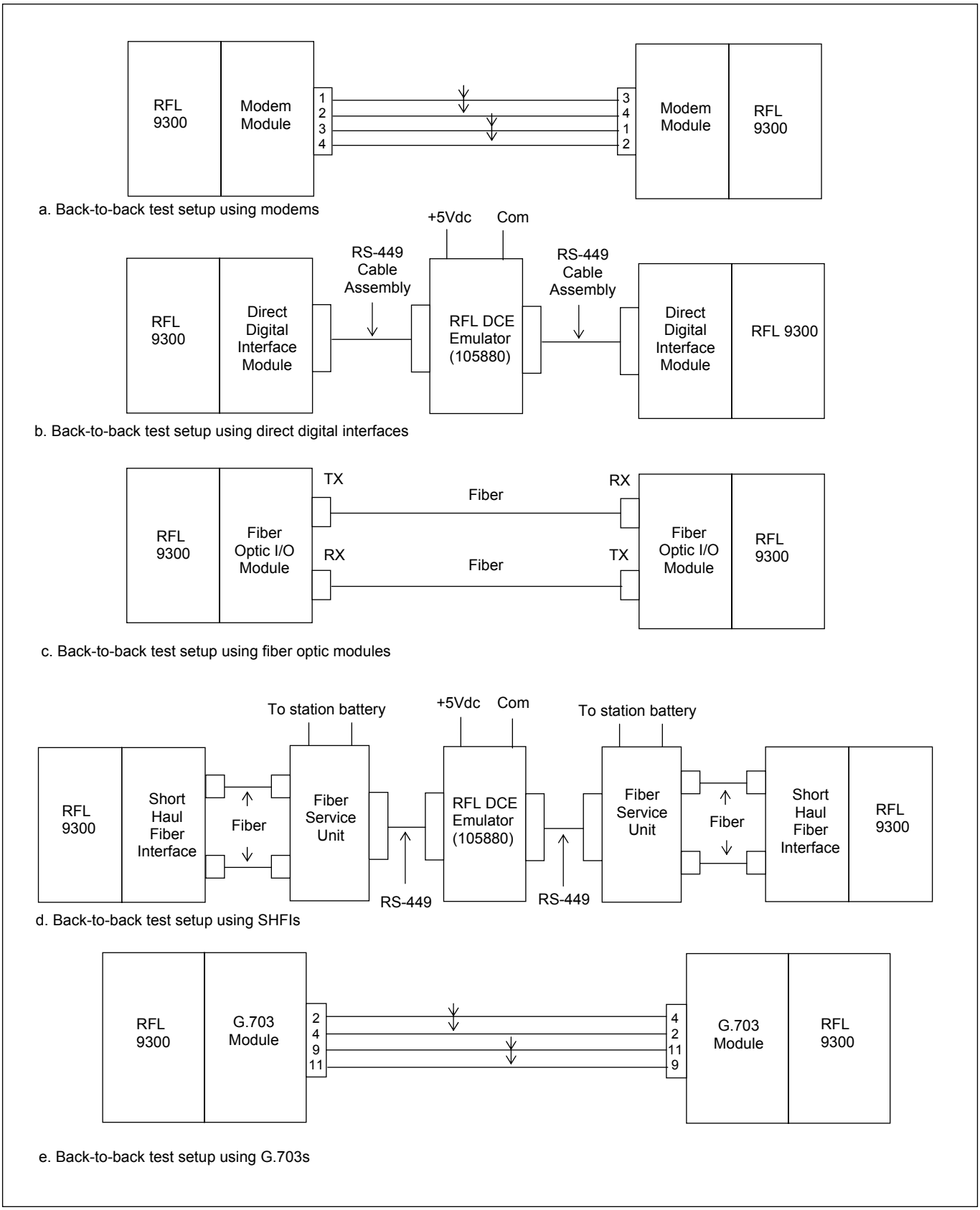


Figure 7-1. Back-to-back relay, test setups

5. Using the PROGRAM display mode, program both relays as follows:

Parameter	Display	Meaning	Value
20	PH BIAS	Phase Bias	3 A
21	GND BIAS	Ground Bias	1.5 A
23	GND DLY	Ground Delay	DISABLE
25	FD PHASE	Local Phase Fault Detector Current	6 A
26	FD GND	Local Ground Fault Detector Current	0.5 A
27	BACKUP	System Backup Functions	ENABLE

6. All other parameters should be set to the factory-default values listed in Tables 6-9 or 6-10 as applicable, in Section 6 of this manual. Using the READ mode, verify these settings. If they are not the default values, use the PROGRAM mode to change them.

NOTE

The RFL 9300 relay determines breaker open/closed status on the basis of AC line current measurements. If all four Phase Controller's measure peak AC line current <= 1/8A for 40ms the supervisor will issue the open breaker signal. If the breaker is open and any one of the four Phase Controllers measures peak AC line current > 1/8A the Supervisor will issue a breaker closed signal. The Phase Controllers are programmed to issue a fault detector signal when the breaker closes. Therefore, in all of the following tests, if the test current is initially zero, all four phase controllers will issue a fault detector signal of 75ms duration when the test current exceeds 1/8A peak, whether the increase is gradual or sudden.

7.4 TEST PROCEDURES

The procedures described in this section will test the conditions and functions listed below:

Condition or Function Tested	Paragraph
Alarm Conditions and Transmit Address Alarm	7.4.1
Direct Transfer Trip	7.4.2
External A-G Faults	7.4.3
Other External Fault Types *	7.4.4
Internal A-G Faults	7.4.5
Internal A-B Faults	7.4.6
Internal Three-Phase Faults	7.4.7
Other Internal Fault Types *	7.4.8
Weak-Feed Internal A-G Faults	7.4.9
Other Weak-Feed Internal Fault Types *	7.4.10
Internal A-G Faults With Remote Breaker Open	7.4.11
Other Internal Fault Types With Remote Breaker Open *	7.4.12
Backup Tripping With High-Set Overcurrent	7.4.13
Demonstration Of Rainbow Characteristic *	7.4.14
Internal A-G Faults With Outfeed *	7.4.15
Demonstration Of Channel Delay Compensation Derived from DML Value *	7.4.16
Oscillography	7.4.17

* Optional procedure.

Some other relay functions are less important, or more difficult to test; these functions are outside the scope of these Laboratory Test Procedures. These functions include the following:

Loss-of-load (backup).

Open conductor detection.

Switch-into-fault (backup).

Desensitizing overreach caused by dc offset.

Channel impairment testing (single-channel).

Dual channel switchover testing.

Bias control, including overhead/underground setting.

Ground delay.

7.4.1 ALARM CONDITIONS AND TRANSMIT ADDRESS ALARM

1. Verify the RFL 9300's local alarm output by removing the phase A controller module.
   The red SYS indicator on the 93B SV LED will light. The display will read "ALARM 60 34" and the beeper will sound. The contacts between rear-panel terminals TB8-1 and TB8-3 will close; this can be verified with an ohmmeter.

2. Push the phase A controller module back into the chassis.
   The relay will return to normal operation; the red SYS indicator will go out, the display will change back to the moving dots, and the beeper will stop.

3. Verify the RFL 9300's local alarm output by removing the phase B controller module.
   The red SYS indicator on the 93B SV LED will light. The display will read "ALARM 61 34" and the beeper will sound. The contacts between rear-panel terminals TB8-1 and TB8-3 will close; this can be verified with an ohmmeter.

4. Push the phase B controller module back into the chassis.
   The relay will return to normal operation; the red SYS indicator will go out, the display will change back to the moving dots, and the beeper will stop.

5. Verify the RFL 9300's local alarm output by removing the phase C controller module.
   The red SYS indicator on the 93B SV LED will light. The display will read "ALARM 62 34" and the beeper will sound. The contacts between rear-panel terminals TB8-1 and TB8-3 will close; this can be verified with an ohmmeter.

6. Push the phase C controller module back into the chassis.
   The relay will return to normal operation; the red SYS indicator will go out, the display will change back to the moving dots, and the beeper will stop.

7. Verify the RFL 9300's local alarm output by removing the G controller module.

   The red SYS indicator on the 93B SV LED will light. The display will read "ALARM 63 34" and the beeper will sound. The contacts between rear-panel terminals TB8-1 and TB8-3 will close; this can be verified with an ohmmeter.

8. Push the G controller module back into the chassis.

   The relay will return to normal operation; the red SYS indicator will go out, the display will change back to the moving dots, and the beeper will stop.

9. Verify the communications alarm functions by turning off the power at the remote relay or by disconnecting the incoming communications link.

   The red TX/RX indicator on the 93B SV module will light, the display will read "ALARM 46," and the beeper will sound. The BACKUP indicator on the 93B DISPLAY module will light, showing that the backup functions are active. The communications alarm output relay will operate, and the contacts between rear-panel terminals TB8-4 and TB8-6 will close; this can be verified with an ohmmeter.

   There will be a 5-second delay in the operation of the alarm output relay. This is because the communications alarm delay (Parameter #41) has been set to ENABLE.

   When testing an RFL 9300 equipped with a modem module, <u>both</u> wires in the twisted pair must be disconnected. If one wire is left connected, a longer recovery time may be required to restore communications. This is because disconnecting a single wire interrupts the communications path in both directions, but inter-wire coupling keeps a small signal present in both directions. This signal confuses the modem, and results in the longer recovery time.

10. Restore the incoming communications signal.

    The local relay will return to normal operation. The red TX/RX and BACKUP indicators will go out, the display will change back to the moving dots, and the beeper will stop.

11. At the present time the local RFL 9300 transmit address is set to “4000” and the remote RFL 9300 transmit address is set to “0095”. These addresses are compatible since their sum equals 4095.

    Verify the operation of the transmit address alarm by setting the transmit address of the local RFL 9300 to “4001”. This will make the transmit addresses of the local and remote RFL 9300s incompatible.

    The displays will read “ALARM 46” and “ALARM 16”, and the beeper will sound.

12. Restore the correct address by setting the local RFL 9300 transmit address back to “4000”.

    The local and remote RFL 9300s will return to normal operation; the alarms will go out, the displays will change back to the moving dots, and the beeper will stop.

7.4.2 DIRECT TRANSFER TRIP

1. At one RFL 9300, connect a dc circuit with 0.2-ampere loading in series with the DTT-1 trip circuit (rear-panel terminals TB2-1 and TB2-2).

   This will be the receiving RFL 9300 during this procedure.

2. At the other RFL 9300, connect a dc voltage across the DTT-IN terminals (rear-panel terminals TB9-3 and TB9-4) as follows:

   If the Alarm I/O is strapped for 48Vdc, connect a 38Vdc to 58Vdc voltage source.
   If the Alarm I/O is strapped for 125Vdc, connect an 88Vdc to 150Vdc voltage source.
   If the Alarm I/O is strapped for 250Vdc, connect a 200Vdc to 288Vdc voltage source.
   (Refer to paragraph 21.2 for Alarm I/O strapping instructions)

   This will be the transmitting RFL 9300 during this procedure.

   When the voltage is applied, the DTT TX indicator should light on the 93B DISPLAY module in the transmitting RFL 9300. The DTT RX and DTT 1 indicators should light on the 93B DISPLAY module at the receiving RFL 9300.

3. Disconnect the dc voltage source from the DTT-IN terminals at the transmitting RFL 9300.

   When the voltage is removed, the DTT TX indicator on the 93B DISPLAY module in the transmitting RFL 9300 will remain lit until its RESET switch is pressed.

   At the receiving RFL 9300, the output relay will remain latched until the initiating voltage is removed at the transmitting RFL 9300, and the DTT-1 trip current is externally interrupted. The indicators at the receiving RFL 9300 will remain lit until the relay is unlatched and the RESET switch is pressed.

4. Watch the display on the receiving RFL 9300.

   If the current through the trip contacts is not interrupted within 500 ms, the message "ALARM 24" will appear on the display. This means that the lockout relay (Device 86) is defective.

5. Repeat steps 2 through 4 with the trip contacts unloaded.

   The DTT 1 indicator at the receiving RFL 9300 will not light, because no trip current was sensed. The DTT tripping relay will remain energized as long as the initiating voltage is applied at the transmitting RFL 9300; this can be verified with an ohmmeter.

This test may be repeated in the other direction. The test also may be repeated with 0.2 Adc loading on the DTT-2 trip circuit (terminals TB2-3 and TB2-4).

7.4.3 EXTERNAL A-G FAULTS

This procedure will prove out the ac current measurement function, the fault detector response, and stability during external faults.

1. Connect a single-phase ac current source to both RFL 9300s. (See Figure 7-2).

   This simulates an external A-G fault. At the left RFL 9300, test current is injected into the Phase A polarity terminal and the $3I_0$ non-polarity terminal. At the right RFL 9300, the polarities are opposite.

   The system external connection diagrams in Section 5 of this manual show the $3I_0$ current connected to the non-polarity terminal of the ground ACT (rear-panel terminal TB4-2). This effectively inverts the polarity of the residual current relative to the phase currents. This technique provides tripping on each half-cycle for ground faults. By inverting the polarity of $3I_0$ relative to I_A, the test circuit of Figure 7-2 follows this technique.

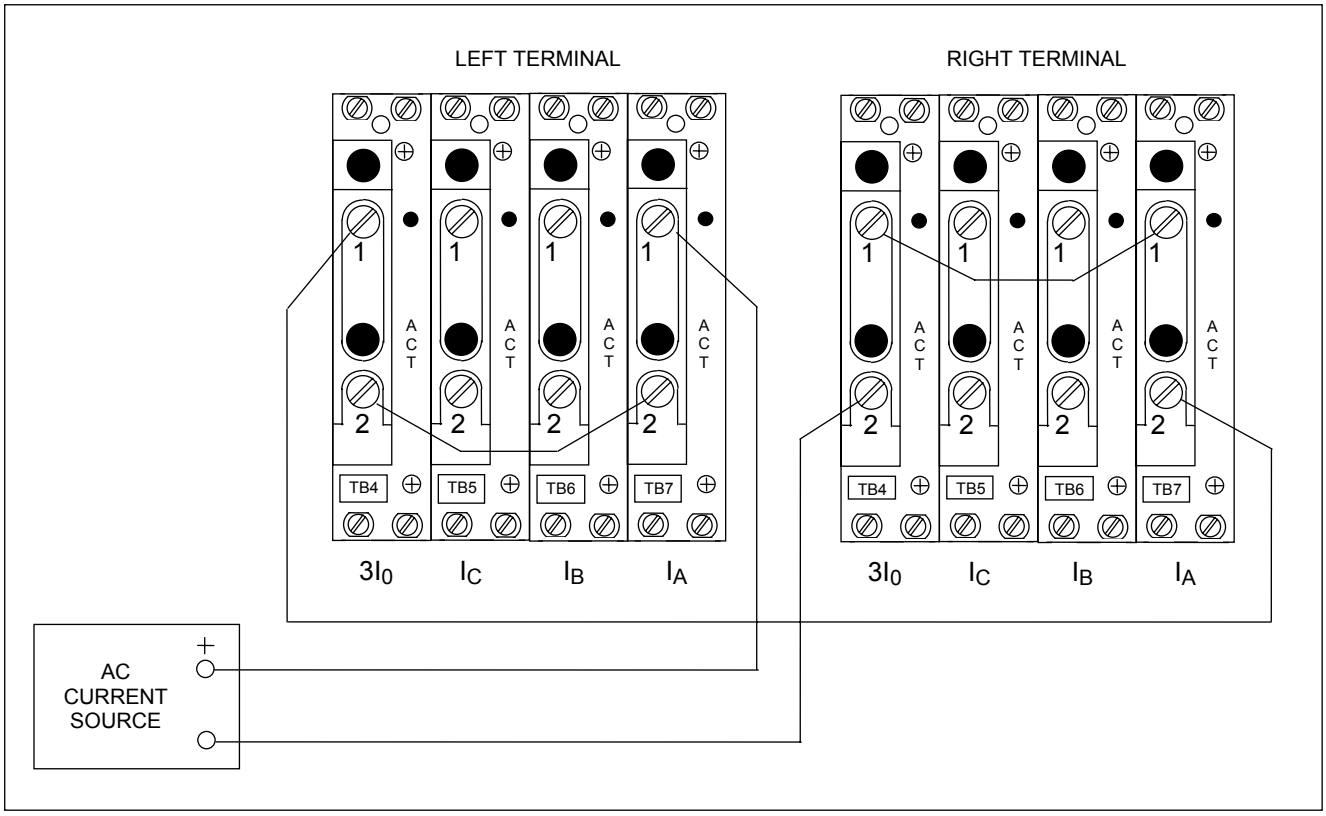


Figure 7-2. Test connections simulating an external A-G fault

2. Vary the magnitude of the ac test current. Place either RFL 9300 in the READ display mode, and verify that the Phase A and $3I_0$ currents are the same value as the test current.

   The currents can be checked by viewing the following parameters:

Local Phase A current	**Parameter #5 (LOC IA)**
Local $3I_0$ current	**Parameter #8 (LOC 3I0)**
Remote Phase A current	**Parameter #9 (REM1 IA)**
Remote $3I_0$ current	**Parameter #12 (REM1 3I0)**

The display has a resolution of 0.25 amperes, and is accurate to ±0.125 amperes. The minimum display reading is 0.5 amperes.

The display ac current readings and settings are in terms of rms amperes. However, the RFL 9300 does not measure current. Instead, it measures "charge," or the area under the half-cycle current wave. For display purposes, the RFL 9300 converts charge to ac rms current (assuming a perfect, symmetrical, 60-Hz sine wave). All references to "current" in this procedure are really "charge, as converted to current."

3. Gradually increase the ac test current.
   At 0.5 amperes, the fault detector in the 93B PC module monitoring $3I_0$ (ground) will pick up, and its FD indicator will light. At 6 amperes, the fault detector in the 93B PC module monitoring Phase A will pick up, and its FD indicator will light.

4. Gradually reduce the AC test current to zero. Suddenly change the test current by at least 1 ampere.
   The phase fault detectors will operate momentarily, and their FD indicators will flash. A pulse-stretching timer keeps these signals active for 75 ms.

5. Apply any test current, suddenly or gradually.
   The RFL 9300s will not trip. The test current may contain a dc offset or harmonics. These waveforms will not cause instability during external fault testing.

7.4.4 OTHER EXTERNAL FAULT TYPES (optional)

1. The other phase-to-ground external faults (B-G and C-G) may be tested by reconnecting the circuit shown in Figure 7-2 to energize Phase B or Phase C instead of Phase A.

2. Phase-to-phase external faults also may be simulated. For example, an A-B external fault may be simulated by connecting the current source as shown in Figure 7-3.

3. Three-phase external faults may be simulated by connecting the equipment as shown in Figure 7-4.
   The test setup in Figure 7-4 creates the phasor relationship shown in Figure 7-5. An external three-phase fault actually has the phasor relationship shown in Figure 7-6.

   Currents I_B and I_C are in-phase for the test simulation, while these currents are 120 degrees out of phase for a real three-phase fault. This difference does not affect the validity of the single-phase test method. The RFL 9300 is a per-phase (or "segregated phase") relay. Each phase current (and residual current) is compared end-to-end, without regard to what is happening on the other phases (or residual). This means that the simplified phasors shown in Figure 7-5 can be used to simulate the real-world phasors shown in Figure 7-6.

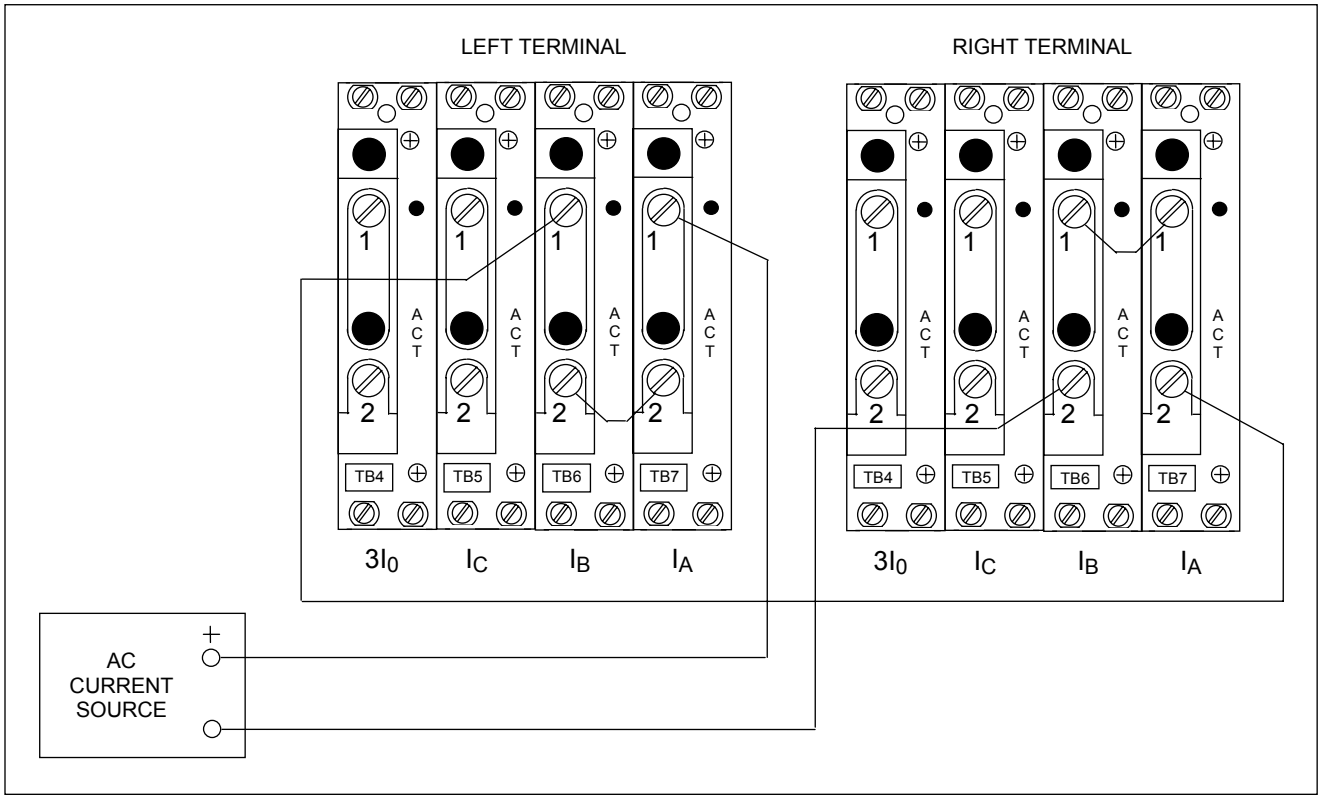


Figure 7-3. Test connections simulating an external A-B fault

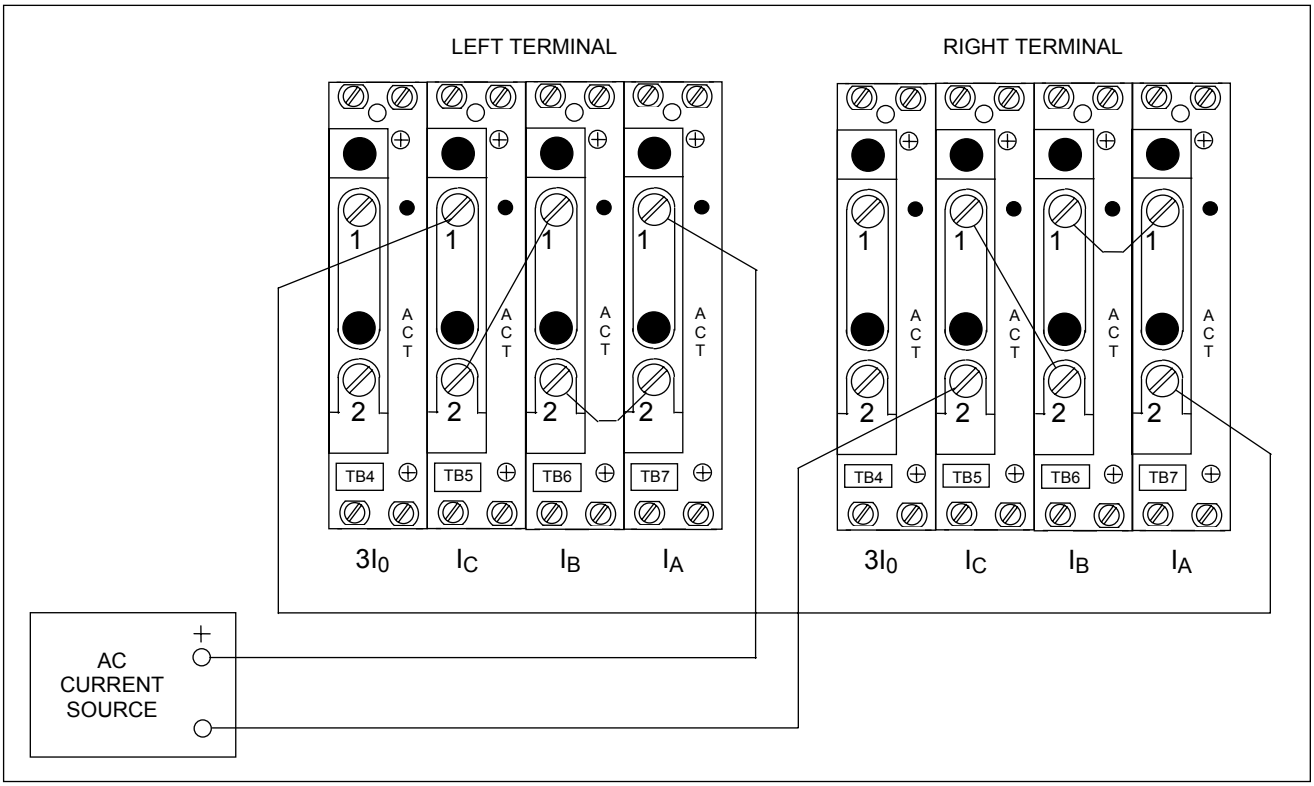


Figure 7-4. Test connections simulating an external three-phase fault

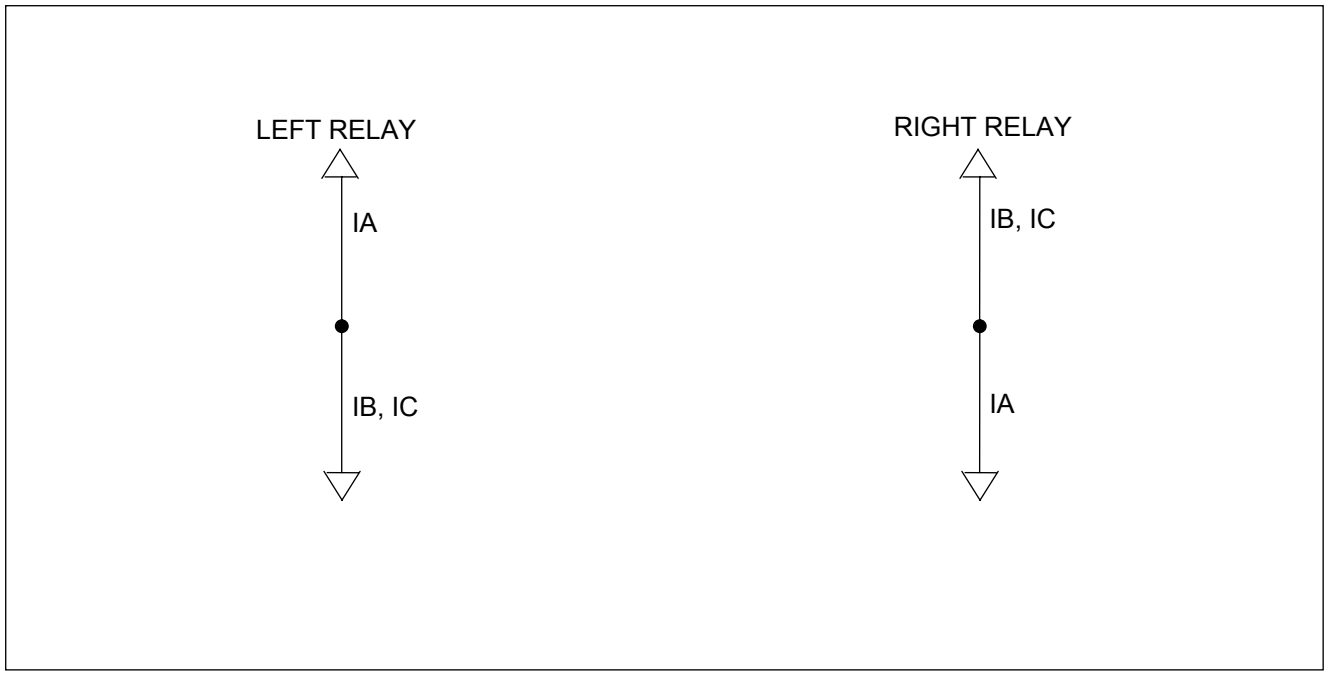


Figure 7-5. Phasor diagram, single-phase test simulation of an external three-phase fault

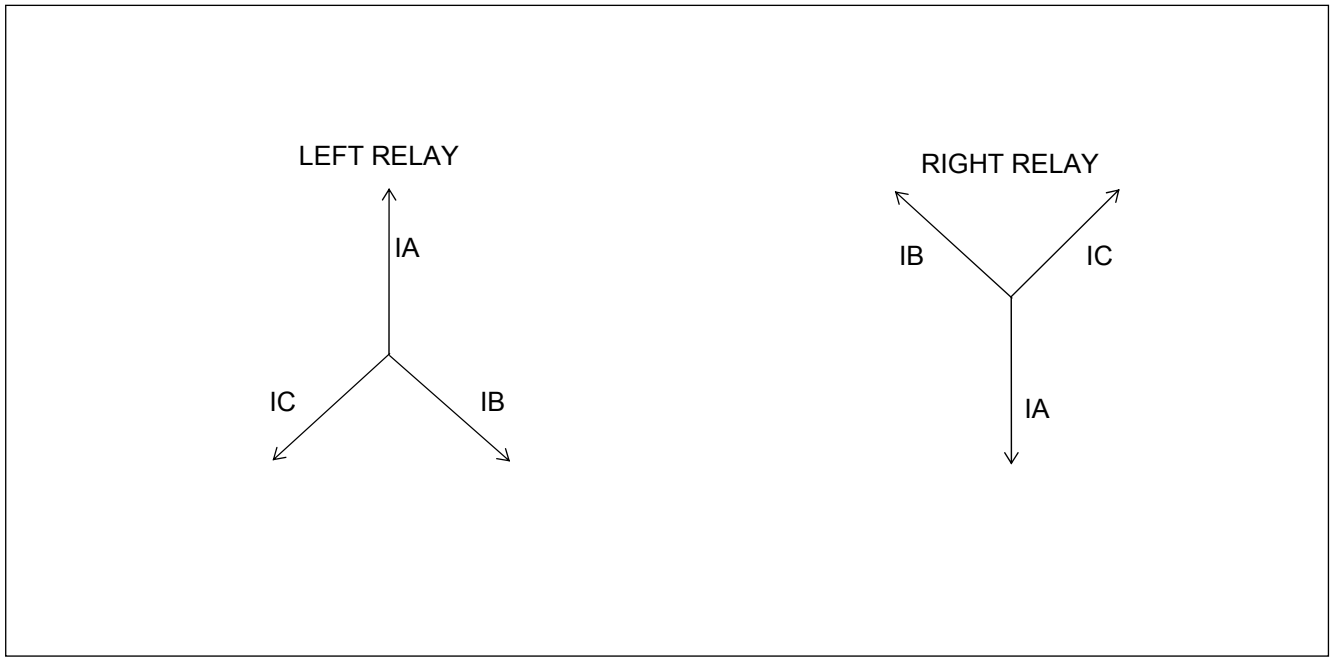


Figure 7-6. Phasor diagram, real external three-phase fault

7.4.5 INTERNAL A-G FAULTS

This procedure demonstrates "SFT" (Strong-Feed Trip) and "UHS" (Ultra-High Speed Trip). It is possible for a UHS to cause a weak-feed trip at the station receiving the UHS message if the current at the receiving station is less than 1.5A and there are no fault detections. Later in this section, weak-feed trip and remote breaker open trip will be tested.

SFT requires currents of at least 0.5 Arms at both terminals. UHS operates whenever the current at one terminal reaches +12 Apeak for 2 ms, and the other terminal does not have a peak reading that is more negative than the Blocking Level (BL). The BL peak value depends on the bias setting:

BL = – (11amperes – bias amperes) peak (minimum value is 7.5A peak)

Example: For a bias setting of 3 amperes rms (4.2 A peak):

BL = – (11 amperes – 4.2 amperes) = – 6.8 A peak

BL = – 7.5 amperes peak (minimum value)

UHS is usually about 5 ms faster than SFT.

1. Connect the equipment as shown in Figure 7-7.
   The current polarities at the left terminal and the right terminal are the same. This creates an "internal" current line-up for Phase A and ground.

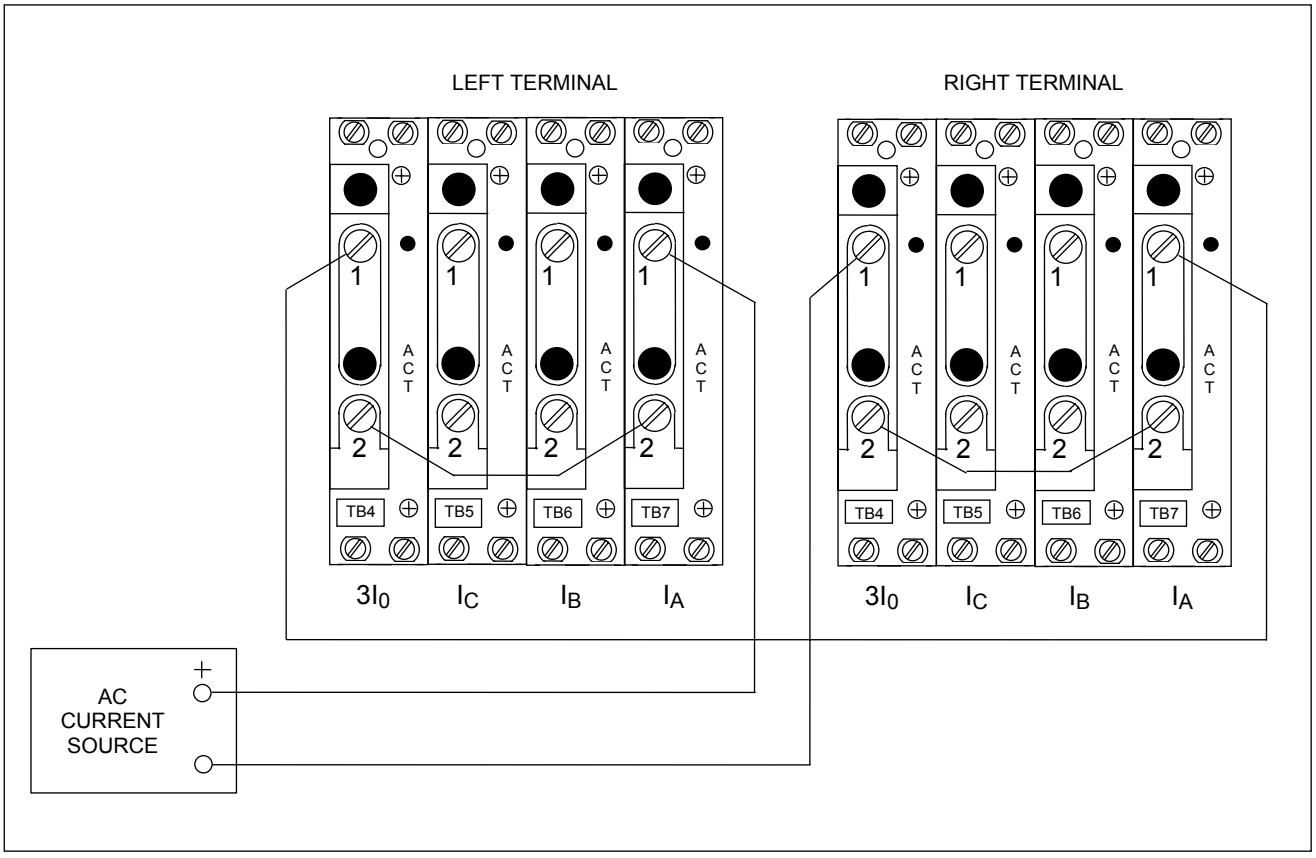


Figure 7-7. Test connections simulating an internal A-G fault

2. Connect a double-pole switch in the test current circuit.

   This will provide a "timer-start" contact for trip time measurements. Use any spare trip contact for "timer-stop," such as terminals 5-6 or 7-8 on TB-3.

3. Connect a dc circuit with 0.2-ampere loading in series with the TRIP 1 tripping contacts at each relay (TB3-1 and TB3-2).

4. Gradually increase the test current.

   At 0.5 ampere, the ground fault detectors will operate. At 0.75 ampere, the relays will trip, with targets on G and TRIP-1.

   At this point, the following conditions occur:

   1. With 0.75 amperes at each terminal, the "arithmetic sum" (or differential current) is 1.5 amperes. This satisfies the ground bias setting of 1.5 amperes.

   2. Both local and remote ground fault detectors operate. This satisfies the fault detector requirements for ground fault tripping.

   3. The 93B PC module monitoring Phase A does not trip for two reasons:

      a. There were no Phase A fault detector operations.

      b. The phase bias setting is 3 amperes, which is well above the arithmetic sum of 1.5 amperes.

5. Remove the test current. After externally interrupting the dc trip current, the relay targets may be reset by pressing the RESET switch on the 93B DISPLAY module.

   If the 0.2-Adc trip current remains for more than 500 ms, the message "ALARM 27" will appear on the display. This means a breaker or auxiliary trip device is defective.

6. Repeat steps 4 and 5 with the breaker trip circuit unloaded.

   The TRIP 1 indicator will not light because the dc trip current was never sensed.

7. Again starting from zero, gradually increase the current.

   At 0.75 ampere, the relays will trip, and the G indicator on the 93B DISPLAY module will light.

8. Continue to increase the current gradually.

   At 1.5 amperes, several actions will occur:

   a. The red SYS indicator on the 93B SV module will light.

   b. The red ALARM indicator on the 93B PC module monitoring Phase A will light.

c. The message "ALARM 34 31 60" will appear on the display.

d. The beeper will sound if it has been enabled.

This condition produces a "Local Charge Comparison Trip" (LCCT) alarm on Phase A (31) and a Phase A Controller general alarm (61). The LCCT alarm occurs because the arithmetic sum of 3 amperes exceeds the phase bias level, and the fault detectors have not energized. The RFL 9300 considers this to be an alarm condition for two reasons:

a. An LCCT alarm condition <u>cannot</u> occur during a real fault.

b. An LCCT alarm condition <u>can</u> occur for certain failure modes in the relay, such as an A/D converter failure.

If you leave this condition on, you will note that the alarm disappears approximately every five seconds and then comes back. This shows that the RFL 9300 is trying to clear the alarm.

9. Simulate an actual fault by applying the LCCT current level suddenly.

All red FD indicators on the 93B PC module will flash momentarily, and the A and G trip indicators on the 93B DISPLAY module will light.

If the fault current is allowed to persist, all fault detectors drop out. This happens because they are based on current change. However, there will be no LCCT alarm. Once a trip signal is issued this alarm is disabled until the fault is removed and a trip is no longer calculated.

10. Apply a test current of 6 amperes or more.

The Phase A fault detectors are now picked up continually, since the test current is above the phase fault detector setting.

If the test current has a full dc offset, tripping may occur at a current level that is significantly less than the steady-state value (for example, an arithmetic sum of 2 Arms instead of 3 Arms). This "overreach" effect is caused by dc offset, and is usually beneficial to the RFL 9300. For internal faults, it can only help improve speed and sensitivity. (Unfortunately, you cannot count on it, because the dc offset may not be present. Its presence depends upon fault inception angle and the L/R ratio of system impedance). On external faults, the dc offset has no effect at all. "Current In" is still equal to "Current Out"; for the RFL 9300, "Charge In" equals "Charge Out."

In tapped-load applications, the dc offset that may occur for low-side faults increases the tendency to over-trip. A higher bias level setting is required to assure security. The RFL 9300's software includes a "DC FILT" setting that allows the user to limit the overreach caused by dc offset.

11. Using the timer circuit described in step 2 above, measure trip times at various current levels. At UHS current levels, trip times will be about 5 ms faster than the times at lower currents. In general, trip times should be 11 to 25 ms for fiber or direct digital versions of the RFL 9300, and 25 to 40 ms for the modem version.

7.4.6 INTERNAL A-B FAULTS

1. Connect the equipment as shown in Figure 7-8.

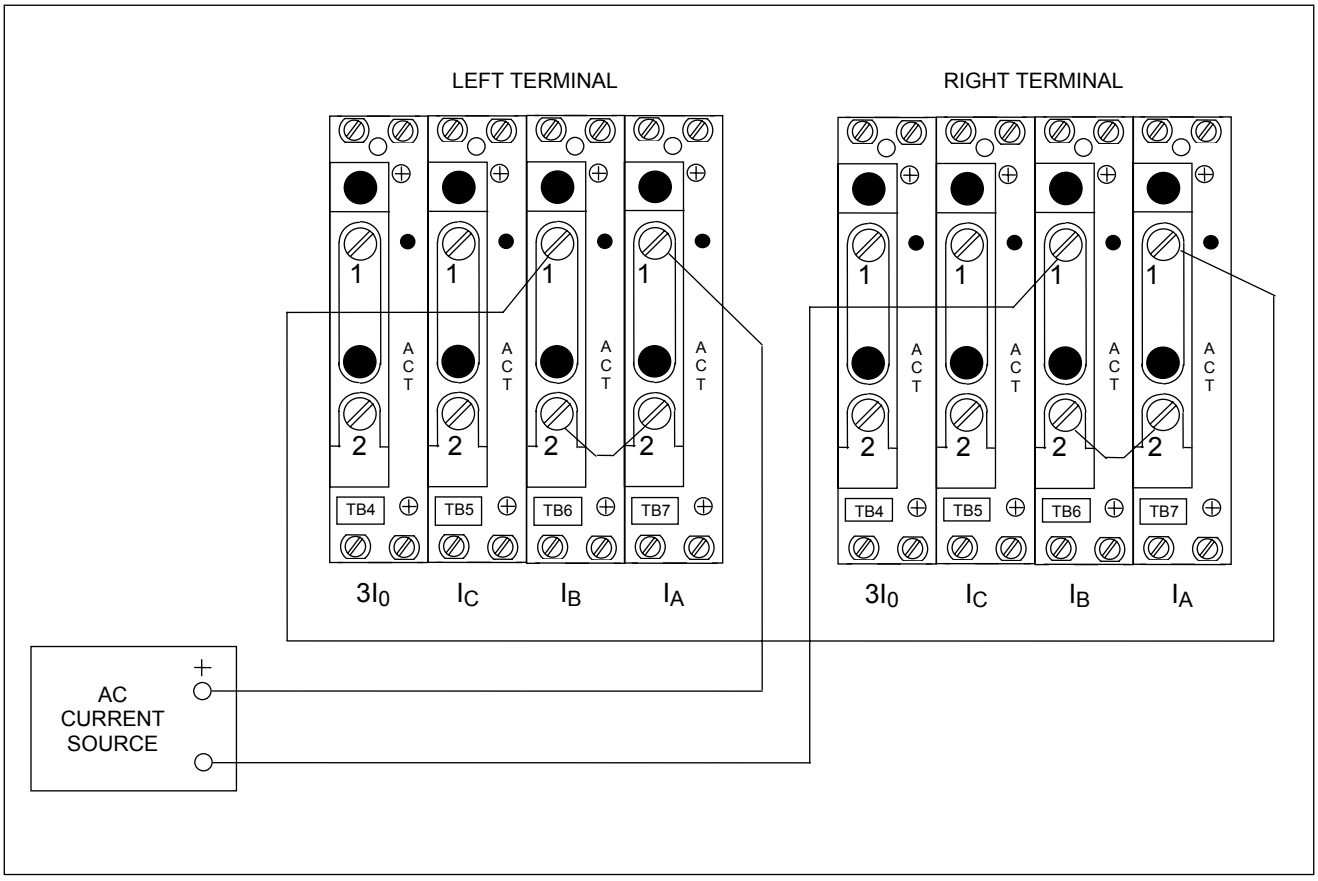


Figure 7-8. Test connections simulating an internal A-B fault

2. Starting from zero amperes, gradually increase the test current.
   At 1.5 amperes, the display will read "ALARM 34 32 31 61 62." This means an LCCT and general phase controller alarm condition exists on Phase A and Phase B.

   Note: All alarms may not be visible on the display controller. Four alarm codes can be displayed at one time. A partial list is considered normal for this test.

3. Apply 1.5 amperes suddenly.
   All red FD indicators on the 93B PC module will flash momentarily, and the A and B trip indicators on the 93B DISPLAY module will light.

4. Apply a test current of 6 amperes or more.
   The red FD indicators on the 93B PC modules monitoring Phase A and Phase B will light.

5 (optional).

   Measure trip times for various current levels.
   The results should be roughly the same as for A-G faults.

7.4.7 INTERNAL THREE-PHASE FAULTS

1. Connect the test circuit shown in Figure 7-9.

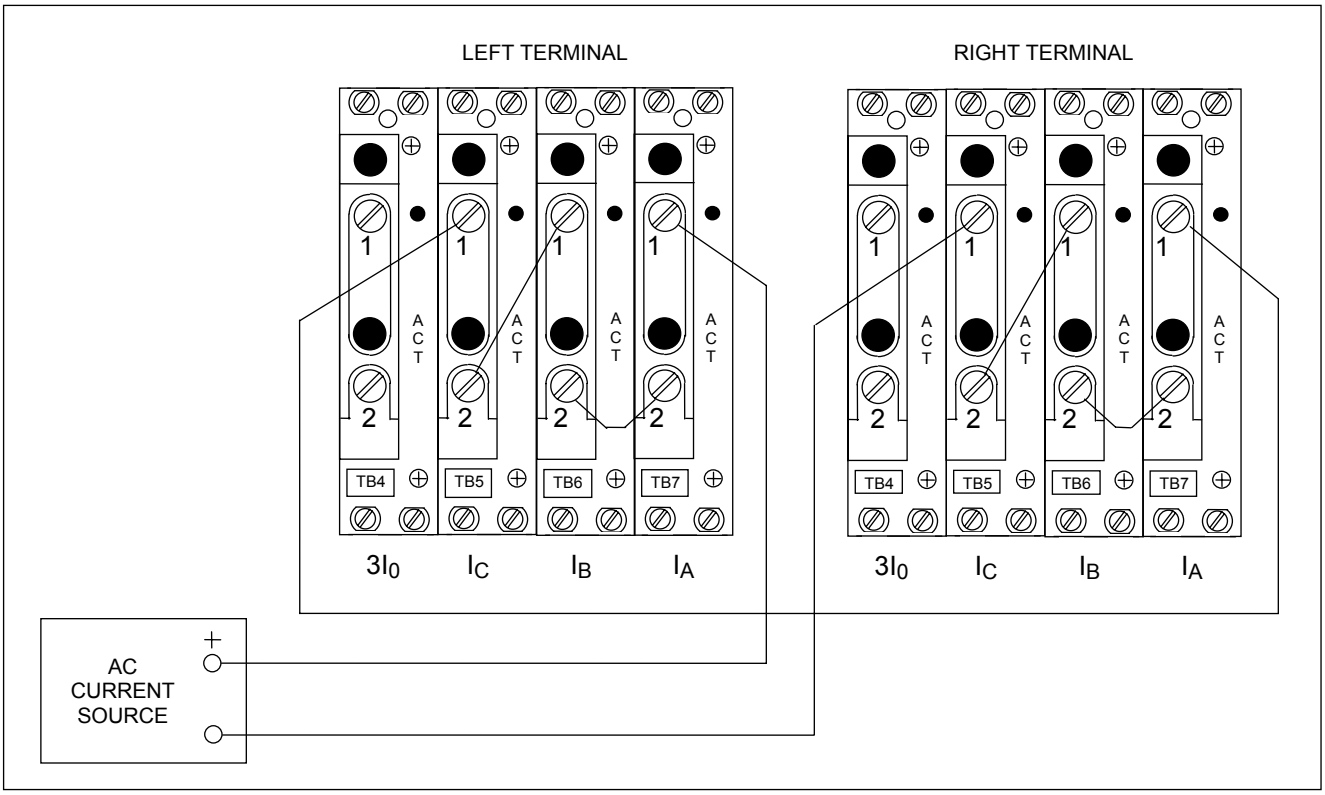


Figure 7-9. Test connections simulating an internal three-phase fault

2. Apply test currents of various levels.

   Results should be similar to the results obtained for the A-B fault simulation, except all three phase targets (A, B and C) should now operate. The reclose block output (terminals TB9-1 and TB9-2) also should operate.

7.4.8 OTHER INTERNAL FAULT TYPES (optional)

The other phase-to-ground (B-G and C-G) and phase-to-phase (B-C and C-A) internal faults may be simulated by modifying the test circuit connections shown in Figures 7-7 and 7-8 to energize the other phases.

7.4.9 WEAK-FEED INTERNAL A-G FAULTS

The RFL 9300's Weak-Feed Trip ("WFT") logic is activated when it senses a small current at one terminal and a large current at the other terminal. This condition is an internal fault with weak infeed at one terminal. The RFL 9300 defines "small" currents as less than 1.5 Arms. "Large" currents are defined as 1.5 amperes plus the bias setting.

1. Connect the test circuit shown in Figure 7-10.

   The test connections shown in Figure 7-10 simulate an internal A-G fault with weak infeed at the right terminal. The current infeed at the right terminal is set at ¼ Arms. Since the current is <0.5 Arms there will not be any current messages transmited from the right terminal to the left terminal. This means that the two current sources are not required to be synchronous. The fact that the phase controllers at the right terminal detect a peak current =>1/4 A will be interpreted to mean that the breaker is closed. If there is no current in the right terminal, the phase controller will interpret this to mean that the breaker is open and this test will generate strong-feed trips.

   The RFL 9300 trips whenever <u>both</u> of the following conditions are met:

   a. The current level at the left terminal is large enough to satisfy the "large" threshold defined above (1.5 amperes plus the bias setting).

   b. The fault detector requirement is satisfied.

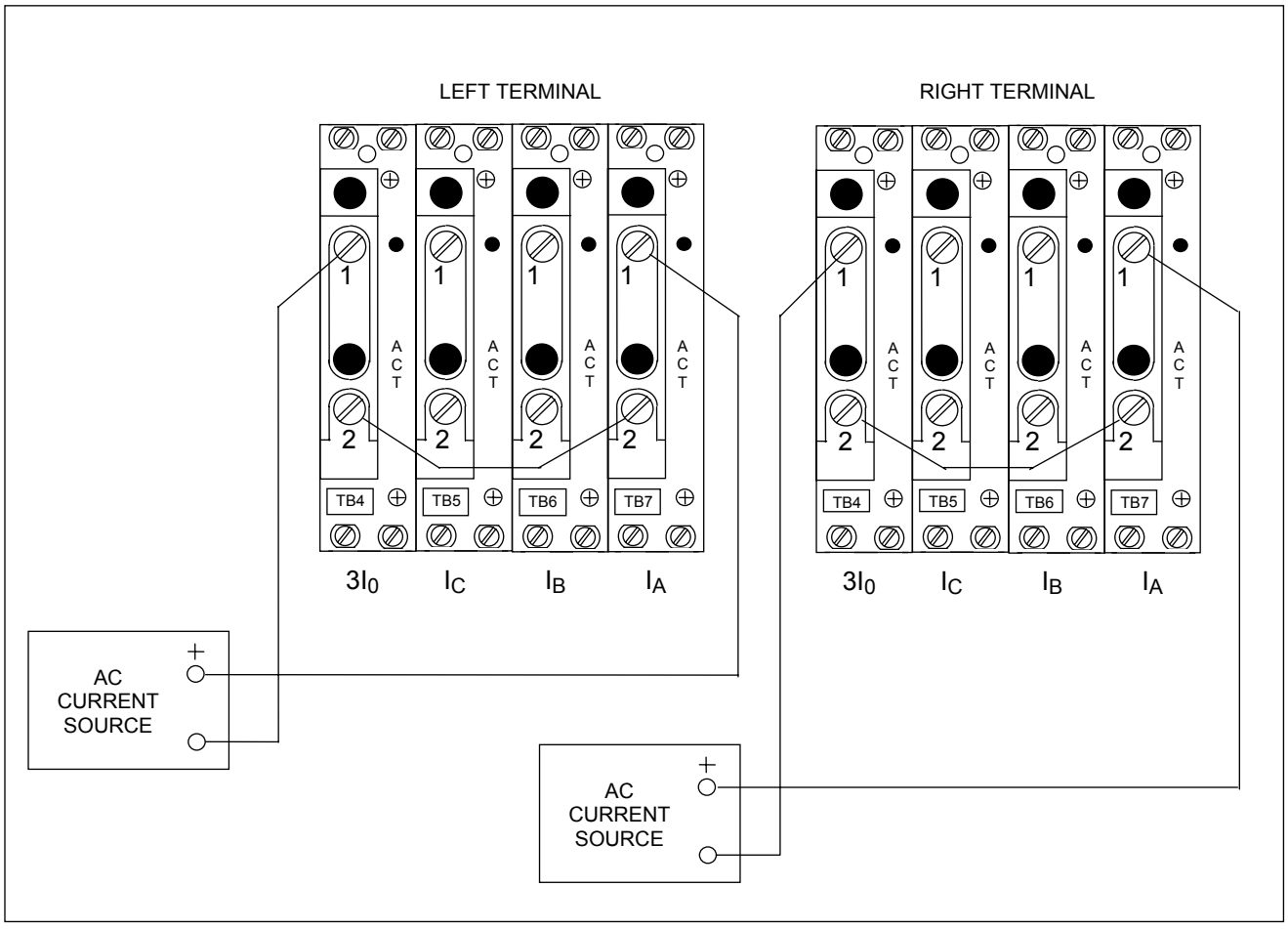


Figure 7-10. Test connections simulating an internal A-G fault with weak infeed at the right terminal

2. Gradually increase the test current at the left terminal.

   The 93B PC module monitoring $3I_0$ will pick up its overcurrent fault detector at 0.5amperes.

   At 3 amperes, the ground WFT logic is satisfied at the right terminal (less than 1.5 amperes local current and a received current of 1.5 amperes plus 1.5 amperes of bias). However, no tripping occurs because only one fault detector (G at the RFL 9300 at the left terminal) has operated.

   The LCCT alarm does <u>not</u> occur, since this alarm is operated only by Strong Feed Trip conditions.

3. Apply the 3-ampere test current suddenly at the left terminal.

   All red FD indicators on the 93B PC module will flash momentarily, allowing the RFL 9300 at the left terminal to trip on the received WFT message. The RFL 9300 at the left terminal then sends "Charge Comparison Trip - Ultimate" (CCT-U) signals to the right RFL 9300, causing it to trip. The TRIP 1 and G target indicators at both relays will light.

4. Return both test currents to zero, and reset the targets on both relays by pressing the RESET switches. Once the relays are reset, gradually increase the test current at the left terminal after returning the current at the right terminal to ¼ Arms.

   At 4.5 amperes, the Phase A WFT logic at the right RFL 9300 is satisfied (1.5 amperes plus 3 amperes phase bias). Once again, there is no tripping because the fault detector requirement has not been satisfied.

5. Return both test currents to zero, and apply the 4.5-ampere test current suddenly at the left terminal.

   All fault detectors in the 93B PC module will now flash momentarily, and both relays will trip. The TRIP 1, A, and G target indicators on both relays will light.

6. Return both test currents to zero, and reset the targets on both relays by pressing the RESET switches. Once the relays are reset, gradually increase the test current at the left terminal.

   At 6 amperes, the Phase A fault detector will pick up (continually), and both relays will trip. The TRIP 1, and A and G target indicators on both relays will light.

7.4.10 OTHER WEAK-FEED INTERNAL FAULT TYPES (optional)

The test circuit shown in Figure 7-10 may be modified to simulate the other types of weak-feed internal faults. Results for B-G and C-G faults should be similar to those described for A-G faults.

7.4.11 INTERNAL A-G FAULTS WITH REMOTE BREAKER OPEN

In 2-terminal mode the RFL 9300 will transmit a Weak Current Message (WCM) whenever the local breaker is open (no AC line current >1/8 A peak detected for 40 ms by all phase controllers). When an RFL 9300 receives a WCM, it will allow tripping if the local current is greater than the bias setting. A single fault detector, on the phase in question, satisfies the fault detector requirement for the 3I0 controller. This applies to 2-terminal mode only and only applies to the 3I0 controller. The phase A, B and C controllers still require 2 fault detectors.

1. Connect the test circuit shown in Figure 7-11.

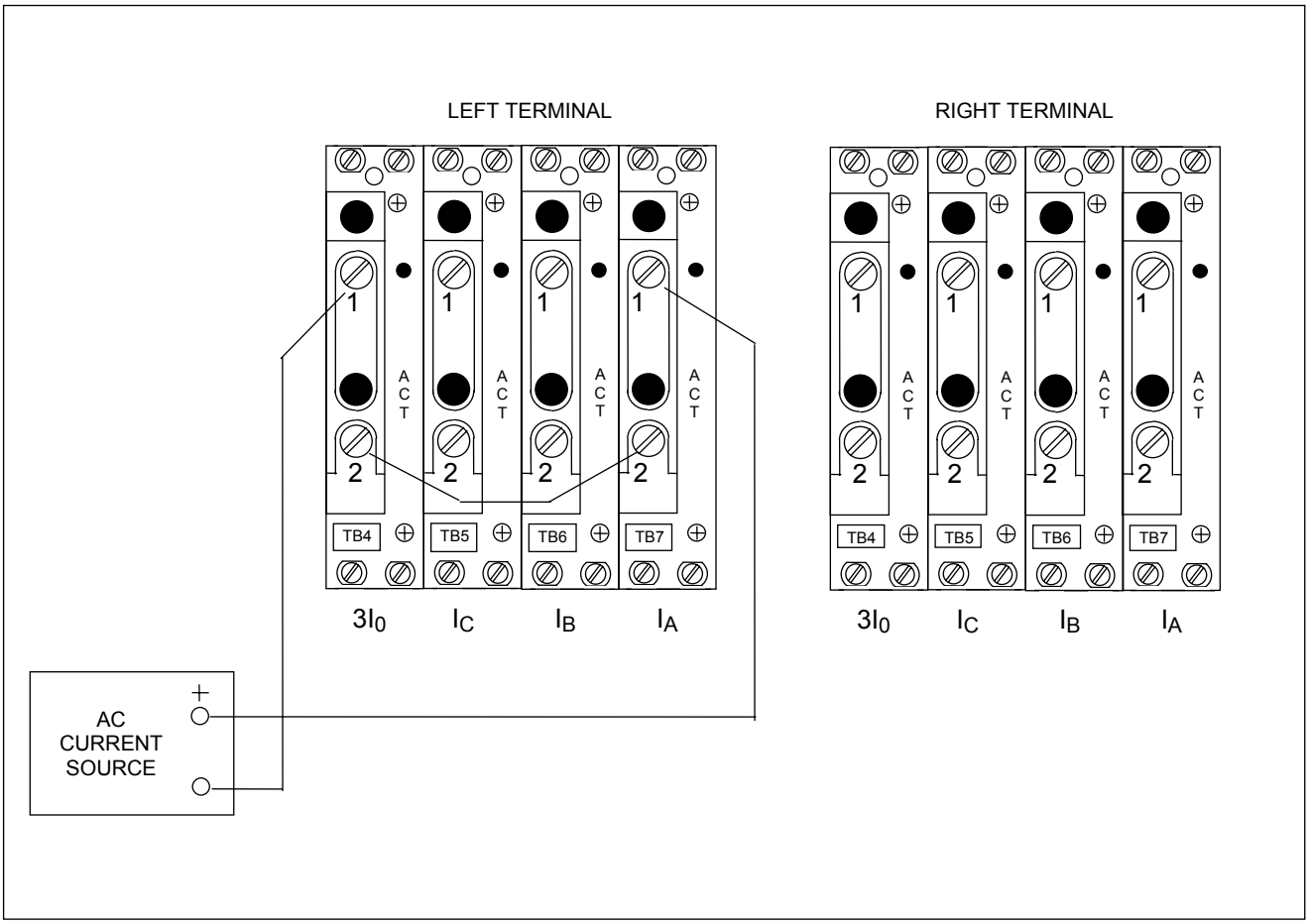


Figure 7-11. Test connections simulating an internal A-G fault with breaker open at the right terminal

2. Slowly increase the test current.

   At 0.5 amperes, the ground fault detector will operate. At 1.5 amperes, both relays will trip and their G target indicators will light. The RFL 9300 at the right terminal will trip on a received CCT-U message.

   It is useful to permit the RFL 9300 at the right terminal to attempt to trip the breaker, even though the lack of any ac line current indicates that the breaker is open. This trip attempt will close the tripping auxiliary relay contacts, and they can serve as breaker failure initiate inputs.

3. Continue to increase the test current.

   At 3 amperes, the LCCT alarm will occur on Phase A. This is because a received WCM activates the Strong Feed Trip (SFT) logic. The received WCM is treated as a received charge comparison data message with a current value of zero.

   At 3 amperes in Phase A at the left terminal, the arithmetic sum is 3 amperes. This satisfies the bias setting and creates an LCCT alarm condition, since the Phase A fault detector does not operate.

4. Return the test current to zero and suddenly apply a 3-ampere current.

   Tripping will occur at both relays, and the TRIP 1, and A and G target indicators on both relays will light.

7.4.12 OTHER INTERNAL FAULT TYPES WITH REMOTE BREAKER OPEN (optional)

The test circuit shown in Figure 7-11 may be modified to simulate the other fault types. The results obtained with B-G and C-G faults should be similar to those obtained with the A-G fault. For phase-to-phase and three-phase faults, the LCCT alarm will occur at 3 amperes if the current is increased gradually. If the 3-ampere test current is applied suddenly, tripping will occur, with appropriate phase targets.

7.4.13 BACKUP TRIPPING WITH HIGH-SET OVERCURRENT

The backup tripping modes (high-set overcurrent/loss-of-load/switch-into-fault) become operative if the received channel signal is lost and Parameter #27 (BACKUP) is enabled (See paragraph 3.13 for more information). The following procedure describes the testing of the high-set overcurrent function. The loss-of-load and switch-into-fault tripping modes are more difficult to test, and are beyond the scope of this procedure.

1. Temporarily lower the phase and ground backup settings to levels that are easy to test (such as 10 amperes phase and 7 amperes ground).

2. Connect the relays for an external A-G simulation. (See Figure 7-2)

3. Disable the channel in either direction.

   Both relays will go into a BACKUP ENABLE condition, and both red BACKUP indicators will light.

4. Increase the test current.

   At the ground overcurrent backup setting (7 amperes), both relays should trip on G and the TRIP 1 and G target indicators on both relays will light. At 10 amperes, both relays should trip on Phase A and the A target indicators on both relays should light.

5 (optional).

   Test the other phases to verify the backup high-set overcurrent tripping level.

6. Return the overcurrent backup settings to the default values (31.87 amperes phase and 31 amperes ground).

If two synchronized ac current sources are available, with the phase angle between test currents adjustable, tests may be done to demonstrate the "rainbow" characteristic, "Delay Measurement Based On Load" (DML) and "outfeed." These optional tests are described in the next three procedures.

7.4.14 OSCILLOGRAPHY TEST

1. Connect the test circuit as shown in Figure 7-19.

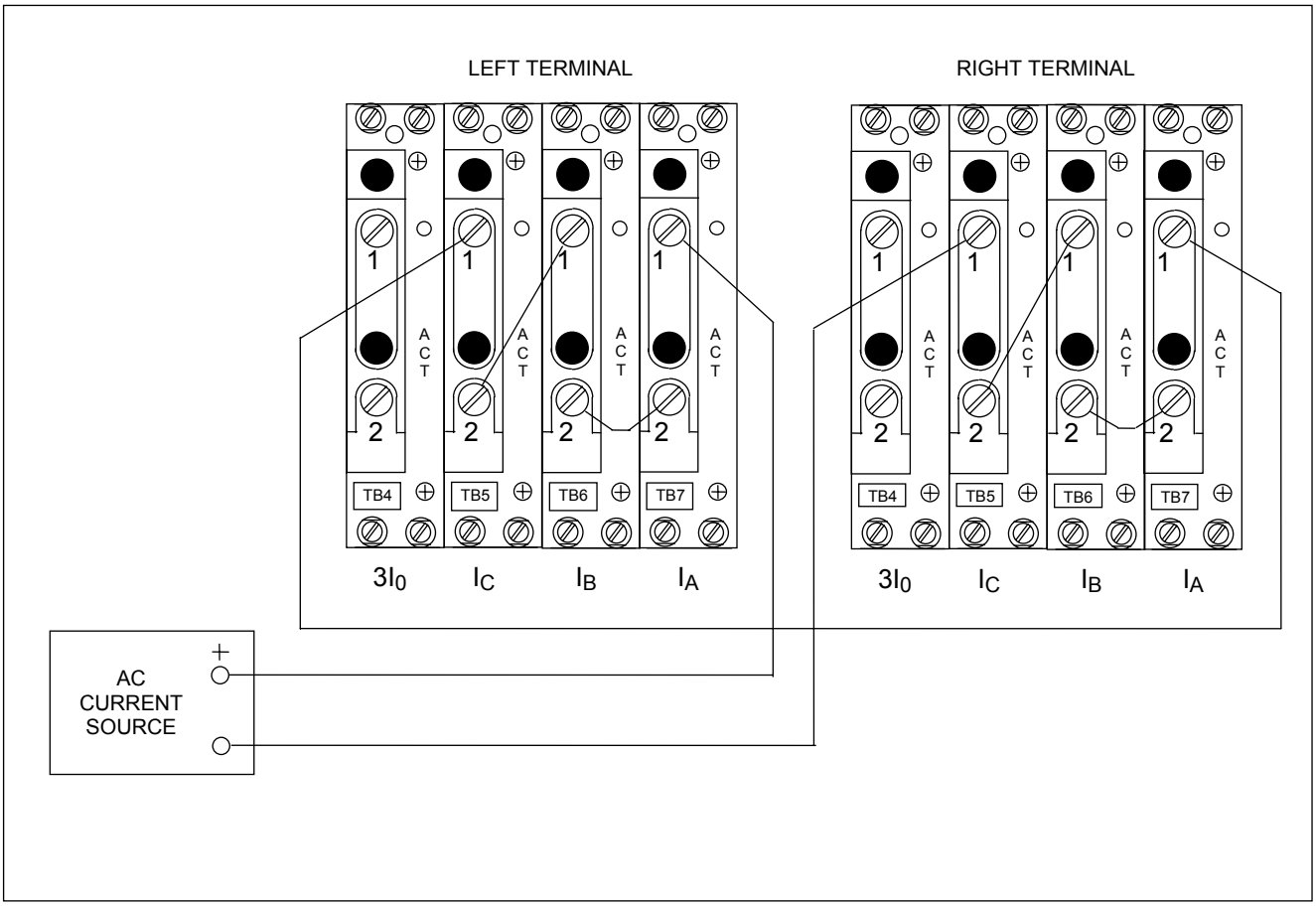


Figure 7-12. Test connections for oscillography test

2. Apply a 3.0 ampere test current.

3. Connect an RS-232 cable from the front or rear RS-232 connector to a PC equipped with Microsoft Windows HyperTerminal emulator. This procedure is described in Section 6 under the heading "ACCESSING THE RFL 9300 FROM A PC OR TERMINAL".

4. Establish communication between the RFL 9300 and your PC or laptop. When communication has been established the RFL 9300 will send the following prompt to your PC:

   9300>

5. Type "S" [ENTER] to enter the sequence of events menu as shown in Figure 6-11.

6. Type "F" [ENTER] to force an oscillography trip event.

7. Type “O” [ENTER] to download the oscillography record from the RFL 9300 oscillography board to the PC or laptop.

8. Click on “TRANSFERS”.

9. Click on “CAPTURE TEXT”.

10. Enter a new filename using the following format: XXXX.TXT. For example you can name the file OSC1.TXT. Then press the [ENTER] key.

11. You will be prompted to enter a record number. Enter record number 1, and then press the [ENTER] key. The oscillography data table will be displayed as shown in Figure 6-15.

12. Click on “TRANSFERS”.

13. Click on “CAPTURE TEXT”.

14. Click on “STOP” after the record is complete.

The oscillography record can be graphed using Microsoft Excel. A diskette containing a Microsoft Excel macro is provided by RFL to perform this task. The diskette also contains a file with instructions on how to use the Microsoft Excel macro under the filename README.TXT. The oscillography test data plot is shown below in Figure 7-20.

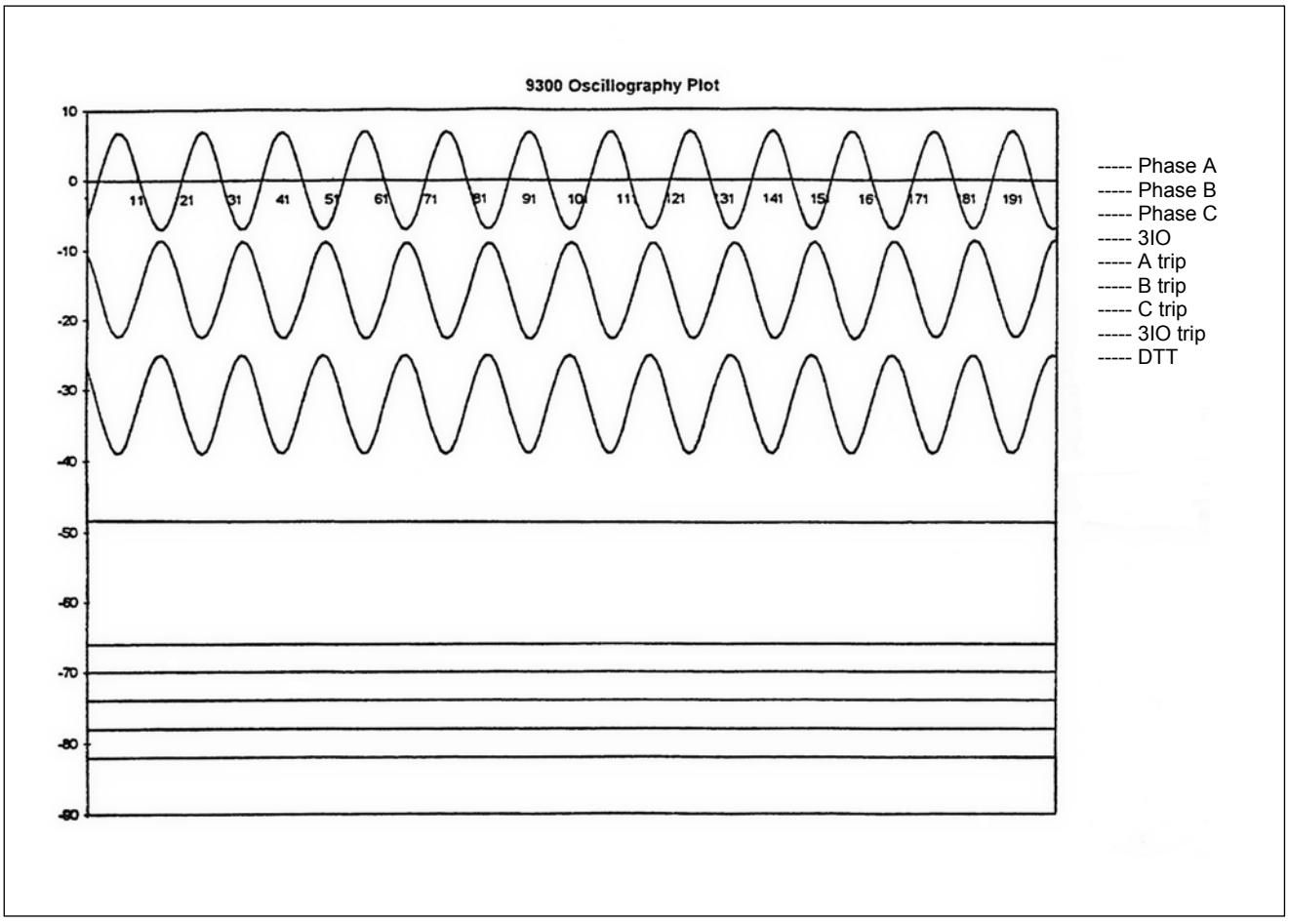


Figure 7-13. Oscillography Test data plot

The laboratory acceptance tests are now completed.

SECTION 8: FIELD COMMISSIONING

CAUTION

PROCEDURE TO PREVENT POTENTIAL RELAY MISOPERATION

Several test procedures in this section require the application of test currents to the 9300 relay. When the AC line current is above 1 amp, the 9300 relay is capable of compensating for unequal channel delay times between the transmit and receive communication paths. This DML (Delay Measurement Based on Load Current) technique is described in paragraph 2.7.8 of this manual. DML is only enabled in two-terminal line applications, and when the line current is above 1 amp. When the 9300 utilizes DML, the adjusted channel delay compensation time is maintained, even after the line current drops below 1 amp. This delay compensation value is maintained until the 9300 detects a loss of communications, excessive BER, or a change in the channel delay as measured by ping pong.

During the commissioning testing, as varying test currents are applied to relays, the relay may enable this DML feature. To insure the relay does not inadvertently maintain an incorrect value of channel delay compensation, it is recommended that when testing has been completed, the relay power supply be turned on and off. This will force the relay to reinitiate, and establish a new channel delay compensation value. It is also recommended at this time, that all relay settings be reconfirmed, and recorded as the "As Left Condition".

8.1 INTRODUCTION

This section contains the procedures required to put a two-terminal RFL 9300 system into service in the field. These include the following:

Description Of Tests	Paragraph
Single-Relay Tests (Optional procedure)	8.2
Verification Of End-To-End Communications	8.3
Startup Mode	8.4
Final Commissioning	8.5

It is assumed that the mounting and wiring procedures described in Section 5 of this manual have been performed, and the relays are in place.

8.2 SINGLE-RELAY TESTS (optional)

8.2.1 INTRODUCTION

NOTE

Three terminal units are to be converted to two terminal operation for Laboratory and Single Relay tests.

Single-relay testing is a convenient alternative to the back-to-back test procedures described in Sections 6 and 7 of this manual. During single-relay testing, the RFL 9300's communications are looped (transmit connected to receive). This means that all injected test currents will simulate internal faults with equal infeed. Other fault types (such as external faults and weak-feed faults) cannot be simulated during single-relay testing.

If the RFL 9300 relays were shipped directly to separate field sites, back-to-back connections cannot be made, and the procedures in Sections 6 and 7 cannot be performed. In this situation, single-relay testing should be performed to verify that each relay operates properly. (Even if you cannot perform the procedures in Sections 6 and 7, it is a good idea to read these sections. They contain information that will help you perform the procedures in this section.)

Single-relay tests in conjunction with startup mode commissioning tests should be sufficient to confirm proper operation and wiring of the relays. However, if End-to-End tests are desired, special test procedures are available from RFL customer service.

If you decide not to perform the single-relay tests, go to the next procedure, Verification Of End-To-End Communications, as shown in paragraph 8.3 of this manual.

NOTE

When performing single-relay tests, enter a Transmit Address of “0000” to disable the addressing feature of the unit. This will allow the unit to operate in looped mode.

8.2.2 EQUIPMENT REQUIREMENTS

The following equipment is required to perform single-relay testing:

1. A Volt-Ohm meter.

2. A dc voltage source capable of supplying either 48 Vdc or 125 Vdc, depending upon the power supplies installed in the RFL 9300.

3. A dc current source that can provide at least 0.4 amperes to drive two 0.2A dc sense circuits.

4. A 60-Hz, single-phase ac current source that can supply up to 15 amperes.

5. The following item is required for 9300 relays equipped with a modem module:

    a. A twisted pair of wires about 12 inches (30.5 cm) long.

6. The following items are required for 9300 relays equipped with a direct digital interface module: (See Figure 8-1)

    a. An RFL DCE emulator (RFL part No. 105880).

    b. A +5Vdc power supply for the RFL DCE emulator.

    c. An RS-449 cable assembly used to connect the direct digital interface module to P1 of the RFL DCE emulator (RFL part No. 302196-X or equivalent).

    d. A loopback connector consisting of a DB-37 male connector with pin 4 connected to pin 6, and with pin 22 connected to pin 24.

7. The following item is required for 9300 relays equipped with a fiber optic module:

    a. A fiber optic patchcord.

8. The following items are required for 9300 relays equipped with a short haul fiber interface module: (See Figure 8-1)

    a. A Fiber Service Unit. (RFL part No. 105075-X)

    b. Two fiber optic patchcords.

    c. An RFL DCE emulator (RFL part No. 105880).

    d. A +5Vdc power supply for the RFL DCE emulator.

    e. An RS-449 cable assembly used to connect the fiber service unit to P1 of the RFL DCE emulator (RFL part No. 302196-X or equivalent).

    f. A loopback connector consisting of a DB-37 male connector with pin 4 connected to pin 6, and with pin 22 connected to pin 24.

9. The following item is required for 9300 relays equipped with a G.703 module:

    a. A loopback connector consisting of a DB-15 male connector with pin 2 connected to pin 4, and with pin 9 connected to pin 11.

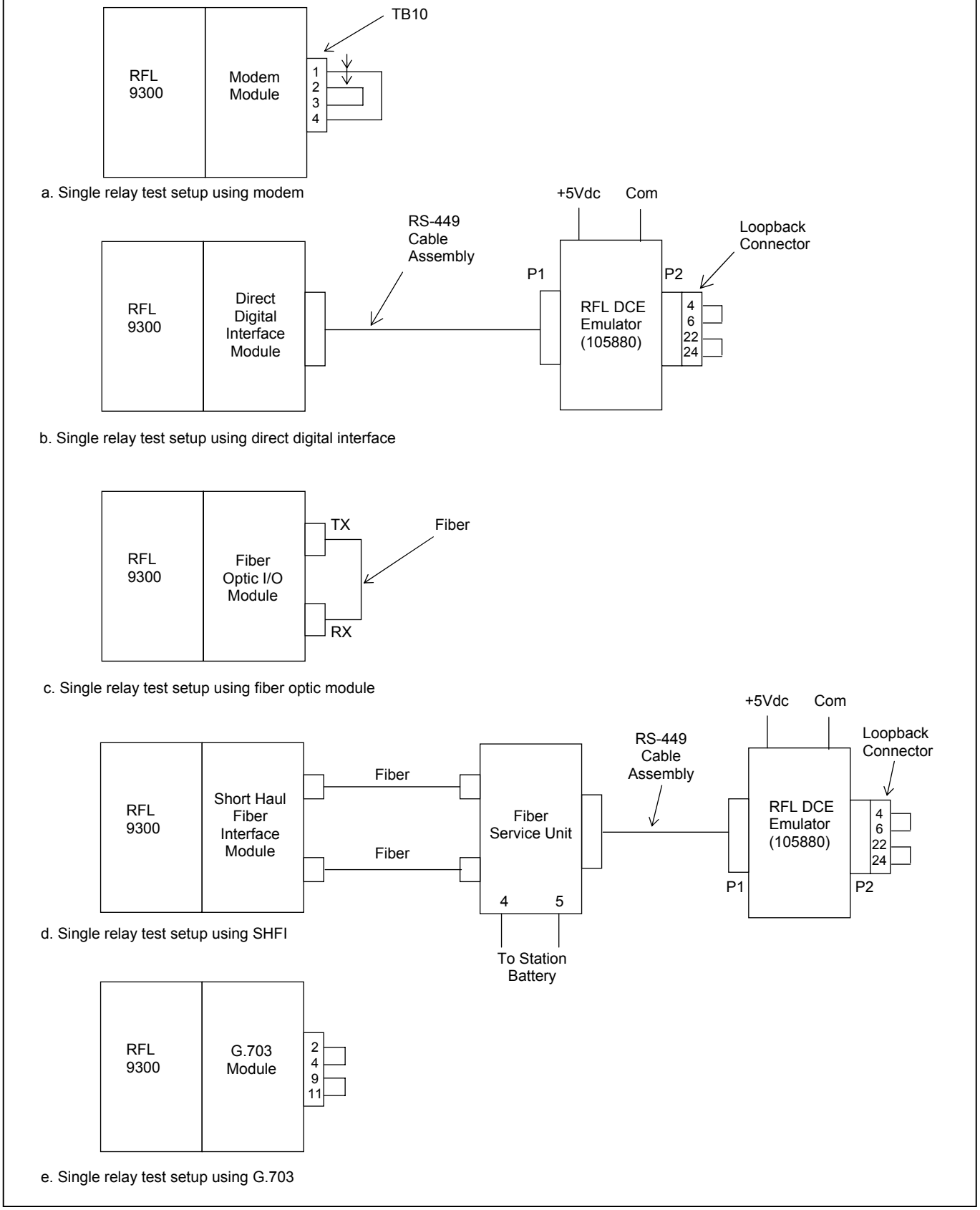


Figure 8-1. Single relay test setups

8.2.3 SINGLE-RELAY TEST PROCEDURES

There are five single-relay tests:

Description Of Test	Paragraph
Familiarization	8.2.3.1
Alarm Conditions	8.2.3.2
Direct Transfer Trip	8.2.3.3
Internal Faults	8.2.3.4
Backup Tripping, High-Set Overcurrent	8.2.3.5

Before performing any single-relay tests, carefully read the procedures in Section 6 of this manual. In particular, review the information on the READ mode and PROGRAM mode. These modes will be used many times during the procedures described in this section. Also, make sure that the modules are using the latest software versions as described in paragraph 6.1 of this manual. Set up the system relay parameters in accordance with paragraph 7.3.

Perform all steps in each test procedure in the order shown, unless otherwise directed. Expected results and/or comments are indented and appear in **boldface** type.

8.2.3.1 FAMILIARIZATION

The following procedure prepares the RFL 9300 for the single-relay tests, and familiarizes you with RFL 9300 operation.

1. Make sure the power switch on the RFL 9300's power supply is in the off ("0") position.

2. Disconnect the BREAKER TRIP and DTT TRIP output circuits by disconnecting the wires from rear-panel terminal blocks TB2 and TB3.

   If the wires are not tagged, tag them as you remove them. This will make it easier to reconnect them later.

3. Disconnect the communications link from the RFL 9300. On relays equipped with modems, remove all wires from the terminal block on the rear-panel of the line coupler I/O. On relays equipped with direct digital, fiber optic, short haul fiber, or G.703 modules, unplug the connectors.

   If the communications lines are not tagged, tag them as you remove them. This will make it easier to reconnect them later.

4. Connect the RFL 9300's transmit output to its receive input as follows:

   Modem Versions:

   Connect one end of a twisted pair to the terminal block on the rear panel of the line coupler I/O, terminals 1 and 2. Connect the other end of the twisted pair to terminals 3 and 4. These connections are not polarity sensitive.

   Direct Digital Versions:

   Connect an RFL DCE emulator, an RS-449 Cable assembly, and a loopback connector to the direct digital interface module as shown in figure 8-1.

   Fiber Optic Versions:

   Connect a fiber optic patchcord between the fiber optic TX and RX connectors on the rear panel.

   Short Haul Fiber Versions:

   Connect an RFL DCE emulator, a fiber service unit, an RS-449 Cable assembly, a loopback connector, and two fiber optic cables to the short haul fiber interface module as shown in figure 8-1.

   G.703 Versions:

   Remove the G.703 module from the 9300 and place the J5 jumper in the “loop” position. Reinsert the G.703 module into the chassis and connect a loopback connector to the G.703 module as described in paragraph 8.2.2, step 9. After the completion of single-relay testing, move the J5 jumper back to the “normal” position before placing the 9300 into service.

5. Place the power switch on the RFL 9300's power supply in the on ("1") position. Set the Transmit Address of the unit to “0000”.

   The three green indicators on the front of the power supply will light, and the RFL 9300 will start to initialize. After a few seconds, the green P-P and BER OK indicators on the 93B CC module will light, and the PROTECTION indicator on the 93B DISPLAY module will light green. A pair of dots will move across both lines of the display, from left to right.

   If the P-P and BER OK indicators fail to light, the RFL 9300's receiver may be overdriven (modem or fiber optic versions) or the clock polarity may be wrong (direct digital version). To correct, do the following:

Modem Versions:

Connect a dBm meter across the modem transmit terminals (line coupler rear panel terminal block, terminals 1 and 2). Lower the 9300 front panel and adjust potentiometer R30 on the modem module to –10dBm. Reset to 0dBm,or to the value required by your local network, after testing.

Direct Digital Versions:

Pull the 93 DD I/O module out of the RFL 9300. Place jumper J2 on the 93 D I/O in Position A, and re-insert the module into the chassis. If the P-P and BER OK indicators still don't light, pull the 93 DD I/O module out gain, place jumper J3 in Position A, and re-insert the module into the hassis.

If the P-P and BER OK indicators still don't light, pull the 93 DD I/O module out again, place J2 back in Position B, and re-insert the module into the chassis.

Fiber Optic Version:

Temporarily loosen one of the fiber optic patchcord connectors.

Short Haul Fiber Version:

Replace the loopback fiber. If the problem persists, replace the short haul fiber interface module.

G.703 Version:

Check the loopback jumper and repair or replace if necessary. Verify that the J5 jumper on the G.703 module is in the "loop" position. If the problem persists, replace the G.703 module.

6. Using Figure 6-1 and Table 6-1 in Section 6 of this manual, familiarize yourself with the RFL 9300's front-panel controls and indicators.

7. Familiarize yourself with the RFL 9300's different display modes by following the procedures starting on page 6-6 in Section 6 of this manual.

8. Using the RFL 9300's PROGRAM display mode, go through the RFL 9300's programmable parameters, and set them in accordance with Table 8-1 for a Two-Terminal system or Table 8-2 for a Three-Terminal system.

9. Place the RFL 9300 back in the STANDBY display mode.
   The display will return to the moving dot pattern.

10. If you plan on using a dumb terminal to access the RFL 9300 through its RS-232 port, refer to paragraph 6.5 in Section 6 of this manual.

11. Connect a dc circuit with 0.2 Ampere loading in series with the DTT-1 trip circuit (rear panel terminals TB2-1 and TB2-2).

Table 8-1. Programmable parameters, RFL 9300 Two-Terminal Charge Comparison System

No.	Display	Definition	Setting
20	PH BIAS	Phase bias	3.0 A
21	GND BIAS	Ground bias	1.5A
22	BIAS CTL	Bias control	ENABLE *
23	GND DLY	Ground delay	DISABLE
24	DLAY SEC	Bias control and ground delay time	1000 ms/30 s *
25	FD PHASE	Local phase fault detector current	6A
26	FD GND	Local ground fault detector current	0.5A
27	BACKUP	System backup functions	ENABLE
28	PH OC BU	Phase overcurrent backup	31.875 A *
29	G OC BU	Ground overcurrent backup	31 A *
30	PH TOC	Phase inverse time overcurrent enable/disable	ENABLE
31	P PICKUP	Phase inverse time overcurrent pickup value	31.875A
32	PH CURVE	Phase inverse time overcurrent curve select	USA1
33	PH DIAL	Phase inverse time overcurrent dial setting	SET 15.0
34	GND TOC	Ground inverse time overcurrent enable/disable	ENABLE
35	G PICKUP	Ground inverse time overcurrent pickup value	31.0A
36	G CURVE	Ground inverse time overcurrent curve select	USA1
37	GND DIAL	Ground inverse time overcurrent dial setting	SET 15.0
38	OVHD/UGD	Overhead or underground cable	UGD *
39	OPEN CON	Open conductor action	ALARM (6) *
41	CM ALM D	Communications alarm delay	ENABLE *
42	DC FILT	Dc filter for tapped load applications	ENABLE *
43	DEFAULT	Reset Parameter #'s 20 - 44 to default values	DISABLE (2) *
44	BEEPER	Enable/disable audible beeper	ENABLE (3) *
45	DISPLAY	Adjust display intensity	Brightest (4) *
46	XMIT ADD1	Select transmit address 1	0000
48	COM MODE	Selects hot standby communications mode.	AUTO *
49	ACT CHAN	Selects channel for hot standby communications.	CH1 or CH2 (5) *
50	G B4 TRP	Guard before trip	ENABLE
51	RS232 BD	Selects RS-232 baud rate	9600 *
52	RS232 PR	Selects RS-232 handshaking protocol	XON/XOFF *
141	SEL POLE	Selective pole relaying enable/disable	DISABLE (7)
145	TRIP RLS	Selects trip release algorithm	TRIP+100

<< Refer to page 8-9 for notes >>

Table 8-2. Programmable parameters, RFL 9300 Three-Terminal Charge Comparison System

No.	Display	Definition	Setting
20	PH BIAS	Phase bias	3.0 A
21	GND BIAS	Ground bias	1.5 A
22	BIAS CTL	Bias control	ENABLE *
23	GND DLY	Ground delay	DISABLE
24	DLAY SEC	Bias control and ground delay time	1000 ms/30 s *
25	FD PHASE	Local phase fault detector current	6 A
26	FD GND	Local ground fault detector current	0.5 A
27	BACKUP	System backup functions	ENABLE
28	PH OC BU	Phase overcurrent backup	31.875 A *
29	G OC BU	Ground overcurrent backup	31 A *
30	PH TOC	Phase inverse time-overcurrent enable/disable	ENABLE
31	P PICKUP	Phase inverse time-overcurrent pickup value	31.875A
32	PH CURVE	Phase inverse time-overcurrent curve select	USA1
33	PH DIAL	Phase inverse time-overcurrent dial setting	SET 15.0
34	GND TOC	Ground inverse time-overcurrent enable/disable	ENABLE
35	G PICKUP	Ground inverse time-overcurrent pickup value	31.0A
36	G CURVE	Ground inverse time-overcurrent curve select	USA1
37	GND DIAL	Ground inverse time-overcurrent dial setting	SET 15.0
38	OVHD/UGD	Overhead or underground cable	UGD *
39	OPEN CON	Open conductor action	ALARM (6) *
41	CM ALM D	Communications alarm delay	ENABLE *
43	DEFAULT	Reset Parameter #'s 20 - 44 to default values	DISABLE (2) *
44	BEEPER	Enable/disable audible beeper	ENABLE (3) *
45	DISPLAY	Adjust display intensity	Brightest (4) *
46	XMIT ADD1	Select transmit address 1	0000
47	XMIT ADD2	Select transmit address 2	0000
50	G B4 TRP	Guard before trip	ENABLE
51	RS232 BD	Selects RS-232 baud rate	9600 *
52	RS232 PR	Selects RS-232 handshaking protocol	XON/XOFF *
141	SEL POLE	Selective pole relaying enable/disable	DISABLE (7)
145	TRIP RLS	Selects trip release algorithm	TRIP+100

Notes for Tables 8-1 and 8-2:

1. The asterisk (*) indicates factory default values.

2. When this parameter is enabled and the **[ENT]** key is pressed, the Display Controller requests that the PROGRAM mode security code (.248) be entered. Once it is, all parameter values will be reset to the default values listed above. These are the values the parameters are set to before the RFL 9300 leaves the factory.

3. When this parameter is set to ENABLE, the audible beeper can be used to notify the operator if an alarm condition exists. During prolonged alarm conditions, the user may wish to disable the beeper until the condition is corrected. It is recommended that this parameter remain enabled. Alarms may not be noticed if the display is in the READ or PROGRAM mode, or if the RFL 9300 is not being manned and the user is depending on the beeper to indicate an alarm condition.

4. When this parameter is shown, the **[8]** and **[0]** keys can be used to increase or decrease the display intensity (or brightness). When the setting is changed, the bottom line of the display will change to the new intensity, while the top line unit remains constant as a reference. When the **[ENT]** key is pressed, both lines assume the new intensity setting.

5. In dual-channel systems, either channel number may be displayed if COMM MODE (Parameter #49) is set to AUTO.

6. This parameter applies to three-pole systems only.

7. This parameter applies to single-pole systems only.

8.2.3.2 ALARM CONDITIONS

The following procedure tests the RFL 9300's local alarm, and communications alarm functions.

1. Verify the RFL 9300's local alarm output by removing the phase A controller module.
   The red SYS indicator on the 93B SV LED will light. The display will read "ALARM 60 34" and the beeper will sound. The contacts between rear-panel terminals TB8-1 and TB8-3 will close; this can be verified with an ohmmeter.

2. Push the phase A controller module back into the chassis.
   The relay will return to normal operation; the red SYS indicator will go out, the display will change back to the moving dots, and the beeper will stop.

3. Verify the RFL 9300's local alarm output by removing the phase B controller module.
   The red SYS indicator on the 93B SV LED will light. The display will read "ALARM 61 34" and the beeper will sound. The contacts between rear-panel terminals TB8-1 and TB8-3 will close; this can be verified with an ohmmeter.

4. Push the phase B controller module back into the chassis.
   The relay will return to normal operation; the red SYS indicator will go out, the display will change back to the moving dots, and the beeper will stop.

5. Verify the RFL 9300's local alarm output by removing the phase C controller module.
   The red SYS indicator on the 93B SV LED will light. The display will read "ALARM 62 34" and the beeper will sound. The contacts between rear-panel terminals TB8-1 and TB8-3 will close; this can be verified with an ohmmeter.

6. Push the phase C controller module back into the chassis.
   The relay will return to normal operation; the red SYS indicator will go out, the display will change back to the moving dots, and the beeper will stop.

7. Verify the RFL 9300's local alarm output by removing the G controller module.
   The red SYS indicator on the 93B SV LED will light. The display will read "ALARM 63 34" and the beeper will sound. The contacts between rear-panel terminals TB8-1 and TB8-3 will close; this can be verified with an ohmmeter.

8. Push the G controller module back into the chassis.
   The relay will return to normal operation; the red SYS indicator will go out, the display will change back to the moving dots, and the beeper will stop.

9. Verify the communications alarm functions by disconnecting the incoming communications link.
   The red TX/RX indicator on the 93B SV module will light, the display will read "ALARM 46," and the beeper will sound. The BACKUP indicator on the 93B DISPLAY module will light, showing that the backup functions are active. The communications alarm output relay will operate, and the contacts between rear-panel terminals TB8-4 and TB8-6 will close; this can be verified with an ohmmeter.

   There will be a 5-second delay in the operation of the alarm output relay. This is because the communications alarm delay (Parameter #42) has been set to ENABLE.

When testing an RFL 9300 equipped with a modem module, both wires in the twisted pair must be disconnected. If one wire is left connected, a longer recovery time may be required to restore communications. This is because disconnecting a single wire interrupts the communications path in both directions, but inter-wire coupling keeps a small signal present in both directions. This signal confuses the modem, and results in the longer recovery time.

10. Restore the incoming communications signal.

    The local relay will return to normal operation. The red TX/RX and BACKUP indicators will go out, the display will change back to the moving dots, and the beeper will stop.

8.2.3.3 DIRECT TRANSFER TRIP

The following procedure tests the RFL 9300's Direct Transfer Trip (DTT) function.

1. Connect a dc circuit with 0.2-ampere loading in series with the DTT-1 trip circuit (rear-panel terminals TB2-1 and TB2-2).

2. Determine the voltage setting of the Alarm I/O module in your relay by referring to paragraph 21.2 before performing this test. It will be set to either 48V, 125V or 250V. Connect a dc voltage source (48 Vdc, 125 Vdc, or 250Vdc as applicable) across the DTT-IN terminals (rear-panel terminals TB9-3 and TB9-4).

   When the voltage is applied, the DTT TX, DTT RX, and DTT 1 indicators should light on the 93B DISPLAY module.

3. Disconnect the dc voltage source from the DTT-IN terminals.

   When the voltage is removed, the DTT TX indicator on the 93B DISPLAY module will remain lit until its RESET switch is pressed. The output relay will remain latched until the DTT-1 trip circuit current is interrupted and a DTT signal has not been received for 100 ms. The DTT RX and DTT 1 indicators will remain lit until the relay is unlatched and the RESET switch is pressed.

4. Watch the display on the 93A DISPLAY module.

   If the current through the trip contacts is not interrupted within 500 ms, the message "ALARM 24" will appear on the display. This means that the lockout relay (Device 86) is defective.

5. Repeat steps 2 through 4 with the trip contacts unloaded.

   The DTT 1 indicator will not light, because no trip current was sensed. The DTT tripping relay will remain energized until 100 ms has elapsed since the last DTT signal was received. This can be verified with an oscilloscope.

8.2.3.4 INTERNAL FAULTS

The following procedures simulate three types of internal faults: A-G, A-B, and three-phase.

8.2.3.4.1 Internal A-G Faults

This procedure demonstrates "SFT" (Strong-Feed Trip) and "UHS" (Ultra-High Speed Trip). SFT requires test currents of at least 0.5 Arms. UHS operates whenever the test current reaches +12 Apeak for 2 ms, and the terminal does not have a peak reading that is more negative than the peak Blocking Level (BL). The value of the local station CT control current required to block a UHS signal received from the remote station(s), referred to as the UHS bias value, is a function of the phase bias setting.

BL = – (11 amperes – bias amperes)peak (minimum value is 7.5A peak)

The equation applies over a limited range of phase bias settings. The range allowed is from 1-2.5 Arms. If the value was less than 1 amp it would already have failed the range test. If the phase bias setting >2.5 Arms the value used for the equivalent peak phase bias setting in the above equation is 3.5 A (peak). Any value greater than this would reduce the blocking current level below 7.5 A (peak) which approaches the level of normal load current (5 Arms max). It is not desirable to have normal load current levels block UHS since this would essentially disable the function.

Example: For a bias setting of 3 amperes rms (4.2A peak):

BL = – (11 amperes – 4.2 amperes) = – 6.8A peak

BL = – 7.5 amperes peak (minimum value)

UHS is usually about 5 ms faster than SFT.

1. Connect the equipment as shown in Figure 8-2.
   This creates an "internal" current line-up for Phase A and ground.

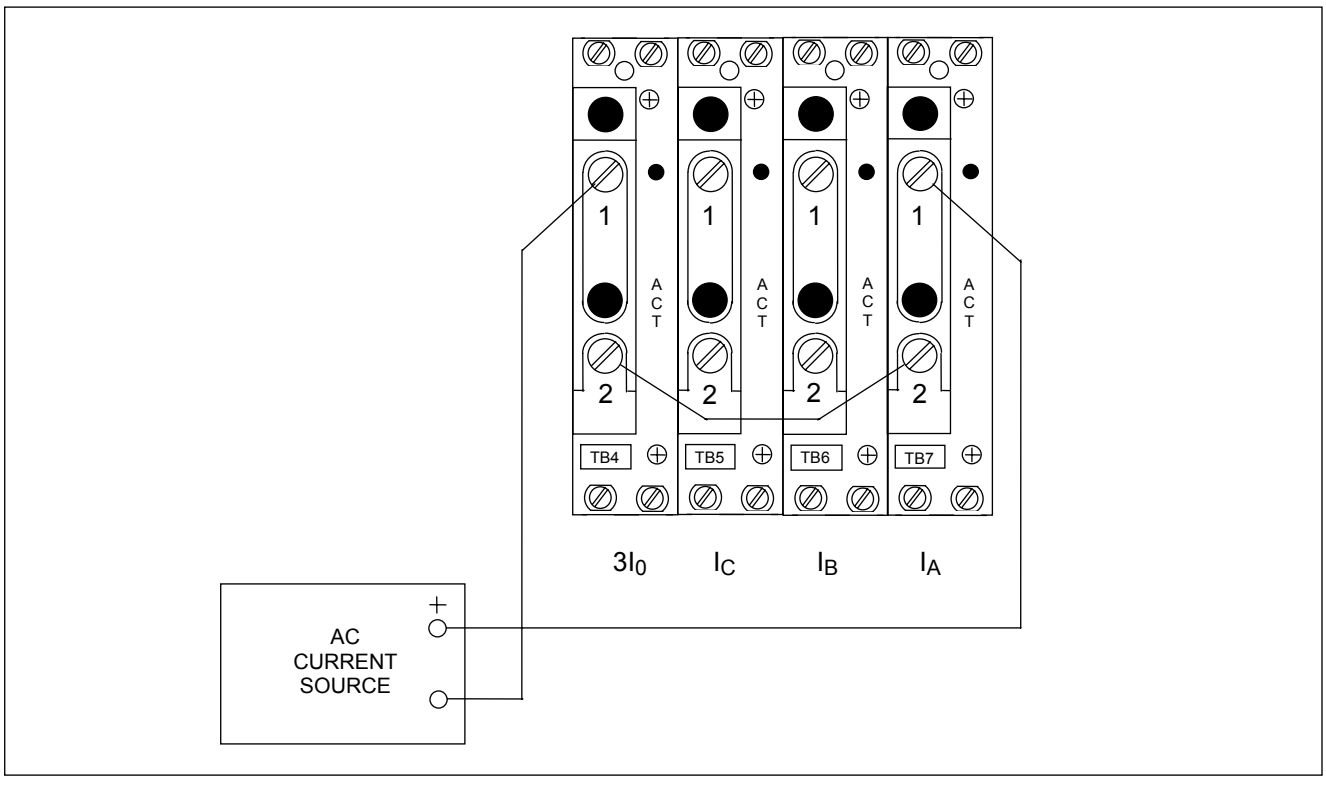


Figure 8-2. Test connections simulating an internal A-G fault

2. Connect a double-pole switch in the test current circuit.

   This will provide a "timer-start" contact for trip time measurements. Use any spare trip contact for "timer-stop," such as terminals 5-6 or 7-8 on TB-3.

3. Connect a dc circuit with 0.2-ampere loading in series with the TRIP 1 tripping contacts (TB3-1 and TB3-2).

4. Gradually increase the test current.

   At 0.5 ampere, the ground fault detector will operate. At 0.75 ampere, the relay will trip, and the G and TRIP-1 indicators on the 93B DISPLAY module will light.

   At this point, the following conditions occur:

   1. With a test current of 0.75 amperes to 1.0 amperes, the "arithmetic sum" (or differential current) exceeds the ground bias setting of 1.5 amperes.

   2. The ground fault detector will operate. This satisfies the fault detector requirements for ground fault tripping.

   3. The 93B PC module monitoring Phase A does not trip for two reasons:

      a. There was no Phase A fault detector operation.

      b. The phase bias setting is 3 amperes, which is well above the arithmetic sum of 1.5 amperes.

5. Remove the test current. The indicators may be reset by pressing the RESET switch on the 93B DISPLAY module.

   If the 0.2-Adc trip current remains for more than 500 ms, the message "ALARM 27" will appear on the display. This means a breaker or auxiliary trip device is defective.

6. Repeat steps 4 and 5 with the breaker trip circuit unloaded.

   The TRIP 1 indicator will not light because the 0.2-ampere dc trip current was never sensed. For this condition, the tripping relay remains operated for 100 ms after the fault is removed, and the phase controller rescinds its trip signal.

7. Again starting from zero, gradually increase the current.

   At 0.5 ampere, the ground fault detector will operate. At 0.75 ampere to 1.0 ampere, the relay will trip, and the G and TRIP-1 indicators on the 93B DISPLAY module will light.

8. Continue to increase the current gradually.

   At 1.5 amperes to 1.75 amperes, several alarms will appear:

   a. The red SYS indicator on the 93B SV module will light.

   b. The red alarm indicator on the 93B Phase A Controller module will light.

   c. The message "ALARM 34 31 61" will appear on the display.

d. The beeper will sound if it has been enabled.

This condition produces a "Local Charge Comparison Trip" (LCCT) alarm on Phase A (31) and a Phase A Controller general alarm (61). The LCCT alarm occurs because the arithmetic sum of 3 amperes exceeds the phase bias level, and the fault detectors have not energized. The RFL 9300 considers this to be an alarm condition for two reasons:

a. An LCCT alarm condition <u>cannot</u> occur during a real fault.

b. An LCCT alarm condition <u>can</u> occur for certain failure modes in the relay, such as an A/D converter failure.

If you leave this condition on, you will note that the alarm disappears every few seconds and then comes back. This shows that the RFL 9300 is trying to clear the alarm.

9. Simulate an actual fault by applying the LCCT current level suddenly.

The red FD indicator on the 93B PC module monitoring Phase A will flash momentarily, and the A and G trip indicators and the TRIP 1 indicator on the 93B DISPLAY module will light.

10. Apply a test current of 6 amperes or more.

The fault detector monitoring Phase A is now picked up continually, since the test current is above the phase fault detector setting.

If the test current has a full dc offset, tripping may occur at a current level that is significantly less than the steady-state value (for example, an arithmetic sum of 2 Arms instead of 3 Arms). This "overreach" effect is caused by dc offset, and is usually beneficial to the RFL 9300. For internal faults, it can only help improve speed and sensitivity. (Unfortunately, you cannot count on it, because the dc offset may not be present. Its presence depends upon fault inception angle and the L/R ratio of system impedance). On external faults, the dc offset has no effect at all. "Current In" is still equal to "Current Out"; for the RFL 9300, "Charge In" equals "Charge Out."

In tapped-load applications, the dc offset that may occur for low-side faults increases the tendency to over-trip. A higher bias level setting is required to assure security. The RFL 9300's software includes a "DC FILT" setting that allows the user to limit the overreach caused by dc offset. DC FILT is available only in 2-terminal mode.

11. Using the timer circuit described in step 2 above, measure trip times at various current levels. At UHS current levels, trip times will be about 5 ms faster than the times at lower currents. In general, trip times should be 11 to 25 ms for fiber, G.703, or direct digital, and 25 to 40 ms for the modem version.

8.2.3.4.2 Internal A-B Faults

1. Connect the equipment as shown in Figure 8-3.

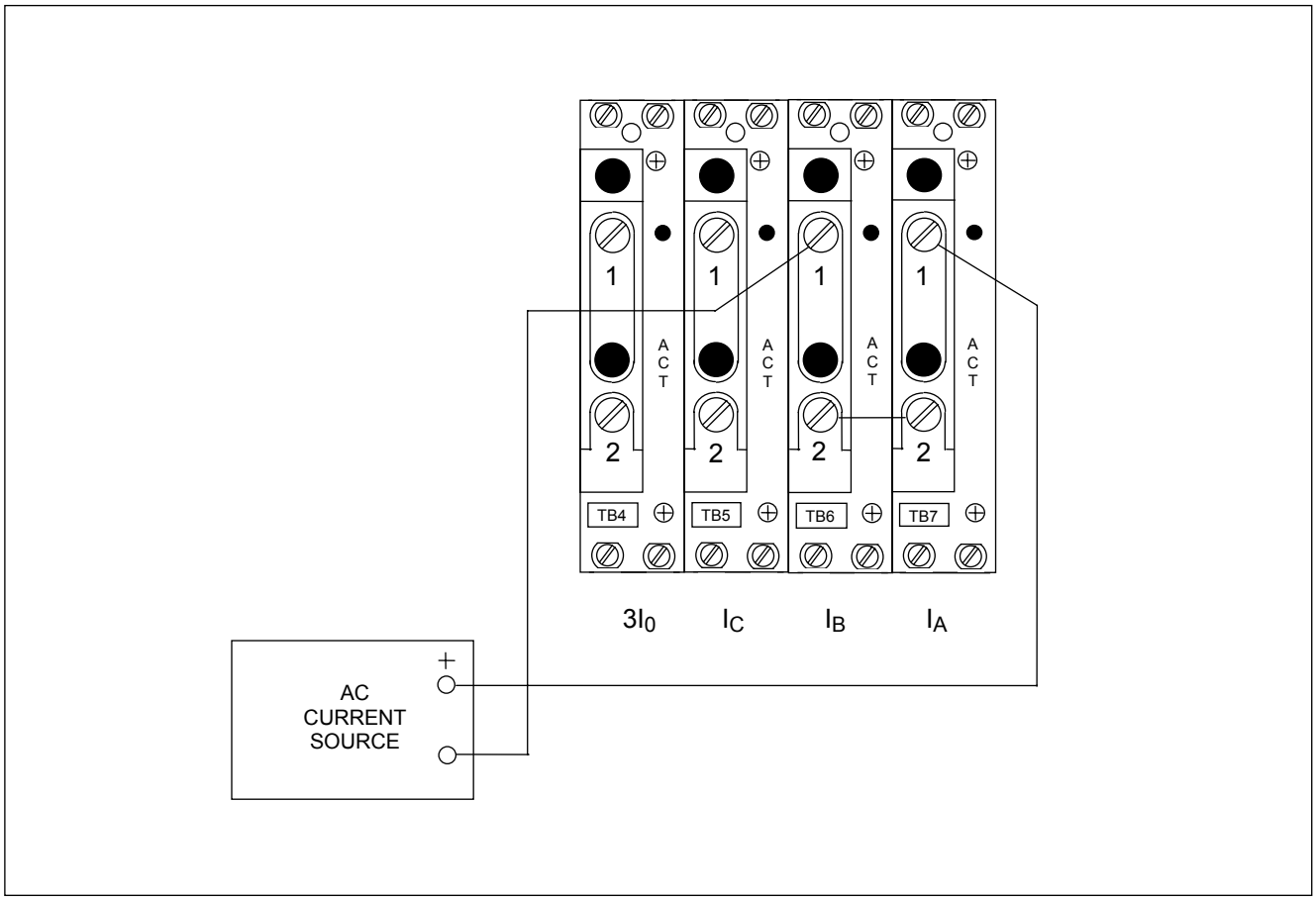


Figure 8-3. Test connections simulating an internal A-B fault

2. Starting from zero amperes, gradually increase the test current.
   Between 1.5 amperes and 1.75 amperes, the display will read "ALARM 34 32 31 61 62." This means an LCCT and general phase controller alarm condition exists on Phase A and Phase B.

   Note: All alarms may not be visible on the display controller. Four alarm codes can be displayed at one time. A partial list is considered normal for this test.

3. Starting from zero, apply 1.5 amperes suddenly.
   The red FD indicators on all 93B PC modules will flash momentarily, and tripping will occur. The A, B, and TRIP 1 indicators on the 93B DISPLAY module will light.

4. Continue to increase the test current to a level of 6 amperes or more.
   The red FD indicators on the 93B PC modules monitoring Phase A and Phase B will light.

5 (optional). Measure trip times for various current levels.
   The results should be roughly the same as for A-G faults.

8.2.3.4.3 Internal Three-Phase Faults

1. Connect the equipment as shown in Figure 8-4.

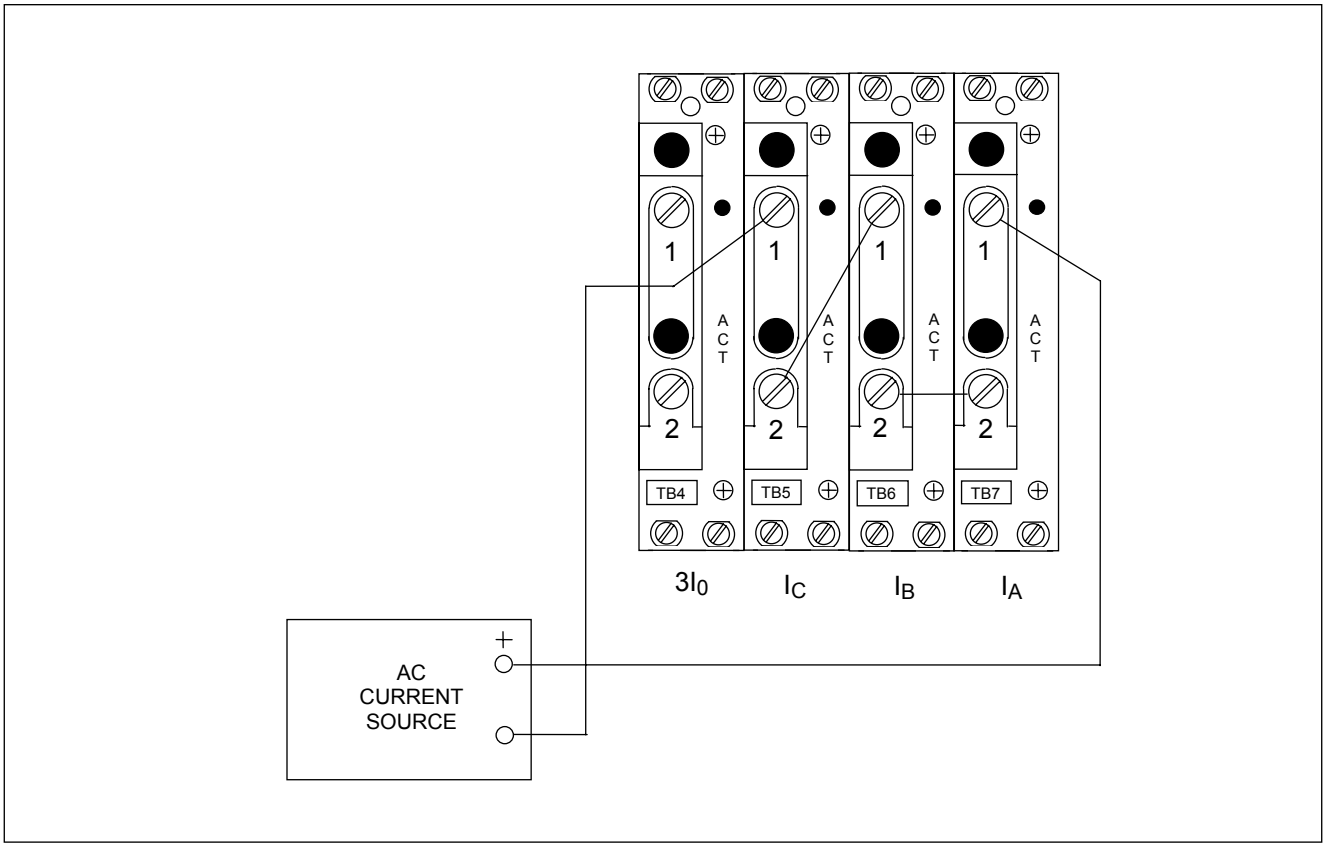


Figure 8-4. Test connections simulating an internal three-phase fault

2. Apply test currents of various levels.

   Results should be similar to the results obtained for the A-B fault simulation, except all three phase targets (A, B, and C) should now operate. The reclose block output (terminals TB9-1 and TB9-2) also should operate.

8.2.3.5 BACKUP TRIPPING, HIGH-SET OVERCURRENT

The RFL 9300's backup tripping modes (High-Set Overcurrent, Loss-Of-Load, and Switch-Into-Fault) become operative if the received channel signal is lost and Parameter #27 (BACKUP) is enabled. The following procedure verifies the high-set overcurrent function. The loss-of-load and switch-into-fault tripping modes are more difficult to test, and are beyond the scope of this procedure.

1. Temporarily lower the phase and ground backup settings to levels that are easy to test (such as 10 amperes phase and 7 amperes ground).

2. Disable the communications channel by disconnecting the incoming communications link.
   The RFL 9300 will go into a BACKUP ENABLE condition, and its red BACKUP indicator will light.

3. Inject test current into Phase A and ground, using the circuit shown in Figure 8-2.

4. Increase the test current.
   At the ground overcurrent backup setting (7 amperes), the RFL 9300 backup should trip on G and its G target indicator should light. At 10 amperes, the RFL 9300 also should trip on Phase A, and its A target indicator should light.

5. (optional) Test the other phases to verify the backup high-set overcurrent tripping level.

6. Return the overcurrent backup settings to the default values (31.87 amperes phase and 31 amperes ground).

The single-relay tests are now complete. To return the RFL 9300 to normal operation, proceed as follows:

1. Make sure the power switch on the RFL 9300's power supply is in the off ("0") position.

2. Reconnect the wires to the BREAKER TRIP and DTT TRIP terminals on rear-panel terminal blocks TB2 and TB3 that were disconnected during the familiarization procedure.
   Use the tags placed on the wires when they were disconnected as a guide when reconnecting them.

3. Disconnect the twisted pair, cable and DCE emulator, or fiber optic patchcord that was connected between the transmit output and the receive input during the familiarization procedure.

4. Reconnect the communication lines that were disconnected during the familiarization procedure.
   Use the tags placed on the wires when they were disconnected as a guide when reconnecting them.

5. Place the power switch on the RFL 9300's power supply in the on ("1") position.
   The three green indicators on the front of the power supply will light, and the RFL 9300 will start to initialize. After a few seconds, the green P-P and BER OK indicators on the 93B CC module will light, and the PROTECTION indicator on the 93B DISPLAY module will light green. A pair of dots will move across both lines of the display, from left to right.

8.3 VERIFICATION OF END-TO-END COMMUNICATIONS

Five different procedures are provided for verifying end-to-end communications: one for modem versions of the RFL 9300, one for direct digital versions, one for fiber optic versions, one for short haul fiber versions, and one for G.703 versions. Use the proper procedure for your RFL 9300:

Version	Paragraph
Modem	8.3.1
Direct Digital	8.3.2
Fiber Optic	8.3.3
Short Haul Fiber	8.3.4
G.703	8.3.5

8.3.1 MODEM COMMUNICATIONS

The following procedure verifies end-to-end communications for RFL 9300 relays equipped with modems. A multimeter or VOM will be required to perform this procedure.

1. Make sure the phone line being used (either dedicated metallic or multiplexed) is rated SPO Class A (Service Performance Objective – Class A).

   Using an SPO Class A line will guarantee communications before, during, and after a fault condition. For more information on SPO classifications, see Appendix B of this manual.

2. Make sure the connections to the phone line have been properly made.

   Connections should be as follows:

Transmit	**TB10-1 to TB10-2**
Receive	**TB10-3 to TB10-4**

3. Set the multimeter or VOM for ac voltage measurements.

4. Check the transmit output level by connecting the multimeter leads across rear-panel terminals TB10-1 and TB10-2.

   For telephone circuits, the meter indication should be about 0 dBm (0.8 volts for 600 ohm termination). For microwave or UHF radio, the desired level may be different, depending upon the communications equipment being used. Adjust the TX ADJ potentiometer on the front of the 93B MO module for the desired output level. The 93B MO module's output range is –20 dBm (TX ADJ fully counter clockwise) to +8 dBm (TX ADJ fully clockwise).

5. Check the receive input level by connecting the multimeter leads across rear-panel terminals TB10-3 and TB10-4.

   The 93B MO's AGC circuit enables it to receive signals from -39 dBm to 0 dBm; most telephone circuits have a nominal receive level of -16 dBm. If the meter indication is much high or lower than this, it must be re-adjusted. (Refer to the documentation supplied with the telephone or radio receiver equipment for the level adjustment procedure.)

   If desired, jumper J1 on the 93B MO module can be placed in Position B (TEST). This will attenuate the receive input signal by about 3 dB, which may be enough to bring the received signal into the range of the AGC circuit.

6. Using the RFL 9300's READ display mode, check the channel delay time by watching the ping-pong value displayed on the bottom line of the display.

   For short lines without long re-routes through alternative phone lines or microwave paths, the ping-pong value should be about 21 ms. For long lines with many repeaters, this delay can be 25 ms or more. (The RFL 9300 can tolerate channel delays as large as 31 ms.)

7. Place the RFL 9300 back in the STANDBY display mode.

   The display will return to the moving dot pattern.

Modem communications have now been verified. Go on to next procedure.

8.3.2 DIRECT DIGITAL COMMUNICATIONS

The following procedure verifies end-to-end communications for RFL 9300 relays equipped with direct digital interfaces. No additional equipment is required to perform this procedure.

1. Make sure the connections between the RFL 9300 and the DCE have been properly made.

   A shielded multi-pair cable should be used to connect the DCE to 37-pin D-subminiature connector J4 on the RFL 9300. This connector accepts RS-422 signals. The cable must be wired according to Table 5-1 in Section 5 of this manual.

2. Check the settings of polarity jumpers J2 and J3.

   J2 sets the polarity of the SEND timing signal, and J3 sets the polarity of the RECEIVE timing signal. Position A selects inverted polarity, and Position B selects normal polarity. The proper jumper settings will depend on the DCE being connected to the RFL 9300. Try to use the RFL 9300 with J2 and J3 in Position B. If the SEND timing is not working properly, move J2 to Position A. If the RECEIVE timing is not working properly, move J3 to Position A.

3. Using the RFL 9300's READ display mode, check the channel delay time by watching the ping-pong value displayed on the bottom line of the display.

   For short lines, the ping-pong value should be 4.0 or 4.5 ms. For very long lines or lines with many repeaters, this delay can be about 6 ms. (The RFL 9300 can tolerate channel delays as large as 31 ms.)

4. Place the RFL 9300 back in the STANDBY display mode.

   The display will return to the moving dot pattern.

Direct digital communications have now been verified. Go on to the next procedure.

8.3.3 FIBER OPTIC COMMUNICATIONS

The following procedure verifies end-to-end communications for RFL 9300 relays equipped with fiber-optic modules. A photometer (Photodyne XE Series or equivalent) will be required to perform this procedure.

1. Make sure the external fibers have been properly connected to the RFL 9300.
   The transmit fiber should be connected to the TX bulkhead connector on the 93 FT/FR I/O module at the rear of the RFL 9300. The receive fiber should be connected to the RX bulkhead connector on the 93 FT/FR I/O module.

2. Disconnect the receive fiber from the 93 FT/FR I/O module, and use a photometer to measure the incoming power level.
   The photometer reading should be within the ranges indicated in Table 8-3.

   If the measured average power is less than that shown in the Receiver Sensitivity column (lower limit with 3-dB margin), there is not enough margin for proper operation. This could be caused by excessive splicing losses in the fibers, excessive coupling losses, or a line length that exceeds the limits shown in Table 8-3.

Table 8-3. Acceptable received fiber optic power levels, RFL 9300 Charge Comparison System

Wavelength And Emitter Type	Mode	Receiver Sensitivity (Lower Limit)	Receiver Sensitivity (Lower Limit With 3-dB Margin)	Typical Line Length
850 nm LED	Multimode	-50 dBm	-47 dBm	5 mi (8 km)
1300 nm LED	Multimode	-40 dBm	-37 dBm	11 mi (18 km)
1300 nm LED	Singlemode	-40 dBm	-37 dBm	18 mi (29 km)
1300 nm Laser	Singlemode	-40 dBm	-37 dBm	36.5 mi (59 km)
1550 nm Laser	Singlemode	-40 dBm	-37 dBm	63 mi (102 km)

3. Using the RFL 9300's READ display mode, check the channel delay time by watching the ping-pong value displayed on the bottom line of the display.
   The ping-pong value should be 4.0 or 4.5 ms.

4. Place the RFL 9300 back in the STANDBY display mode.
   The display will return to the moving dot pattern.

Fiber optic communications have now been verified. Go on to the next procedure.

8.3.4 SHORT HAUL FIBER COMMUNICATIONS

The following procedure verifies end-to-end communications for RFL 9300 relays equipped with short haul fiber modules. No additional equipment is required to perform this procedure.

1. Make sure the connections between the RFL 9300 and the (FSU) fiber service unit have been properly made.
   The transmit fiber should be connected from the TX connector on the short haul fiber interface module to the RCV connector on the fiber service unit. The receive fiber should be connected from the RX connector on the short haul fiber interface module to the TX connector on the fiber service unit. The RS-449 cable should be connected from the fiber service unit to the external equipment.

2. Using the RFL 9300's READ display mode, check the channel delay time by watching the ping-pong value displayed on the bottom line of the display.
   For short lines, the ping-pong value should be 4.0 or 4.5 ms. For very long lines or lines with many repeaters, this delay can be about 6 ms. (The RFL 9300 can tolerate channel delays as large as 31 ms.)

3. Place the RFL 9300 back in the STANDBY display mode.
   The display will return to the moving dot pattern.

Short haul fiber communications have now been verified. Go on to the next procedure.

8.3.5 G.703 COMMUNICATIONS

The following procedure verifies end-to-end communications for RFL 9300 relays equipped with G.703 modules.
No additional equipment is required to perform this procedure.

1. Make sure the connections between the RFL 9300 and the external equipment have been properly made.
   A shielded, two-pair, four conductor cable with a 15-pin D-subminiature connector should be connected from the G.703 module on the rear panel of the RFL 9300 to the external equipment. This cable must be wired according to the G.703 signal list in Section 23 of this manual.

2. Check the settings of jumpers J2, J3 and J5.
   J2 should be in position A for normal operation.
   J3 should be set for a 56kbps or 64kbps data rate.
   J5 should be in the NORM position for normal operation.

3. Using the RFL 9300's READ display mode, check the channel delay time by watching the ping-pong value displayed on the bottom line of the display.
   For short lines, the ping-pong value should be 4.0 or 4.5 ms. For very long lines or lines with many repeaters, this delay can be about 6 ms. (The RFL 9300 can tolerate channel delays as large as 31 ms.)

4. Place the RFL 9300 back in the STANDBY display mode.
   The display will return to the moving dot pattern.

G.703 communications have now been verified. Go on to the next procedure.

8.4 STARTUP MODE

8.4.1 STARTUP MODE OVERVIEW

NOTE

THIS PROCEDURE IS FOR TWO-TERMINAL AND THREE-TERMINAL SYSTEMS.

IT IS ASSUMED THAT WE HAVE A QUIESCENT SYSTEM, THERE ARE NO ALARMS AND THERE ARE NO TAPPED LOADS IN THE SYSTEM. CURRENT FLOWING INTO ANY TAPS ON THE LINE WILL AFFECT THE ACCURACY OF THE “DIFF CURR” TEST.

Two tests are performed in Startup Mode to insure that the relay is correctly connected. These are the Phase Sequence test and the Differential Current test. These tests when used together will insure that PHASE A, PHASE B, and PHASE C CT connections are correct and that the 3I0 controller connections are properly phased. Either condition would prevent the unit from operating correctly.

Programming the relay using any remote RS232 connection to the display via APRIL is not recommended while Startup Mode is active at any of the stations in the system.

8.4.2 PHASE SEQUENCE TEST OVERVIEW

The phase sequence test checks for positive sequence phase rotation by determining if Phase A Current Leads Phase B current by 120 degrees and Phase B Current Leads Phase C current by 120 degrees and finally that Phase C current leads Phase A current by 120 degrees. The possibility that the phases are connected in sequence but are rotated in some way is addressed by the Differential Current test.

8.4.3 DIFFERENTIAL CURRENT TEST OVERVIEW

The differential current test determines if Phase A Current inputs at all stations are phased correctly relative to each other. It does this by calculating the arithmetic sum of the Phase A currents at each station. Since the relay operates on the assumption that current going into the protected zone equals current going out, the difference must always be zero in a balanced system with no faults and all wires connected to the proper inputs. The possibility that the phases are rotated in some way is addressed by the Differential Current test as well as the possibility that one station is phase inverted with respect to the other(s).

8.4.4 STARTUP MODE

NOTE

All relays should be placed in standby mode prior to starting this test using the step by step instructions in Section 6.

The RFL 9300 has four display modes:

1. STANDBY This is the RFL 9300's normal operating mode. The STANDBY mode is active whenever the RFL 9300 is not in any of the other modes.

2. READ The READ mode allows you to display all present parameter settings and readings. You move between parameters by pressing the **[ENT]** key and then the **[9]** key. This mode can be entered without a password.

3. STARTUP The STARTUP mode allows you to display parameters required during Final Commissioning of the Relays. You move between parameters by pressing the **[ENT]** key and then the **[9]** key. This mode requires a password for entry and exit.

4. PROGRAM The PROGRAM mode allows you to change parameter settings. Once a programmable parameter is displayed, you can scroll through a list of its allowable settings by using the **[8]** and **[0]** keys. This mode requires a password for entry and exit. New parameter values are not accepted unless the **[ENT]** key is pressed when the selected value is displayed on the bottom line of the display.

For more information on the RFL 9300's display modes, refer to the following paragraphs in this manual:

STANDBY	-	para. 6.4.1
READ	-	para. 6.4.2
STARTUP	-	para. 6.4.3
PROGRAM	-	para. 6.4.4

If program mode or read mode is active on any of the units, it is recommended that the user return the units to Standby Mode before Startup Mode is entered by any of the units in the system. Once Startup mode is active all operators including the ones at the remote stations may inspect parameters.

The relays should be programmed to the extent that the communications channels should already be verified and functioning correctly with no alarms present at any station before beginning the Startup Mode commissioning procedure.

For reliable accuracy, at least 1 amp of current should be flowing on all 3 phases through each station before entering startup mode. If Phase A current is less than 0.5 A RMS, the relay will reject the command to enter startup mode and return to standby mode.

8.4.4.1 ENTERING THE STARTUP MODE

NOTES

Before entering the STARTUP Mode, be sure to isolate the trip output circuit.

As soon as either station in a two terminal system or any of the three stations in a three terminal system is placed in STARTUP MODE, all the units will respond by entering Startup Mode. This will occur whether or not there is an operator using the display at the remote station(s). If the remote station has an operator displaying values in Read Mode or Program Mode, it may not be apparent that the system has entered Startup Mode and the remote relay will not display the Phase Sequence Test.

Tables 8-4 and 8-5 list the parameters that are available in STARTUP Mode. To enter the STARTUP Mode from the STANDBY mode, proceed as follows:

1. Press the **[ENT]** key two times.
   The word "STARTUP" will appear on the top line of the display, and the word "DISABLE" will appear on the bottom line.

2. Press the **[8]** key once.
   The word "ENABLE" will appear on the bottom line of the display.

3. Press the **[ENT]** key.
   The message "SEC CODE" will appear on the display. This means that you must enter a security code before the RFL 9300 will enter the STARTUP Mode. Press the [.], [1], [3],[5] and [ENT] keys as the required security code.

The relay should now be in startup mode and the display will show that the Phase Sequence Test has begun.

NOTE

As soon as the relays enter the startup mode, trip will be disabled at all substations. The RFL 93B SV at each substation will activate the system alarm as a constant reminder that the relay is not operating in a normal mode

Table 8-4. STARTUP mode parameters for RFL 9300 Two-Terminal Charge Comparison Systems

No.	Display	Definition
...	Moving dots	RFL 9300 is in STANDBY mode. Display controller parameter; not user-selectable.
0	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE.
1	PngPng 1	Value of ping-pong (round-trip delay) for remote 1.
3	SEQ TEST	Phase Sequence Test.
4	DIFF CURR	Differential Current Test
5	LOC IA	Local Phase A current.
6	LOC IB	Local Phase B current.
7	LOC IC	Local Phase C current.
8	LOC 3I0	Local 3I0 current.
9	REM1 IA	Remote 1 Phase A current.
111	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE.

Table 8-5. STARTUP mode parameters for RFL 300 Three-Terminal Charge Comparison Systems

No.	Display	Definition
...	Moving dots	RFL 9300 is in STANDBY mode. Display controller parameter; not user-selectable.
0	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE.
1	PngPng 1	Value of ping-pong (round-trip delay) for remote 1.
2	PngPng 2	Value of ping-pong (round-trip delay) for remote 2.
3	SEQ TEST	Phase Sequence Test.
4	DIFF CURR	Differential Current Test
5	LOC IA	Local Phase A current.
6	LOC IB	Local Phase B current.
7	LOC IC	Local Phase C current.
8	LOC 3I0	Local 3I0 current.
9	REM1 IA	Remote 1 Phase A current.
13	REM2 IA	Remote 2 Phase A current.
111	EXIT	Exit to STANDBY mode. Display function; can be set to either ENABLE or DISABLE.

8.4.4.2 PHASE SEQUENCE TEST ("SEQ TEST")

The phase sequence test determines if Phase A Current Leads Phase B current by 120 degrees and Phase B Current Leads Phase C current by 120 degrees and finally that Phase C current leads Phase A current by 120 degrees. The possibility that the phases are connected in sequence but are rotated in some way is addressed by the Differential Current test.

One amp of current should be present on each phase for the relays to enter startup mode. If not already in Startup Mode, enter Startup Mode following the detailed step by step instructions above, or see Section 6.

STEP 1.
The first test that is run in STARTUP MODE is the Phase Sequence test. As soon as either station in a two terminal system or any of the three stations in a three terminal system is placed in STARTUP MODE, all the units will respond by entering Startup Mode. This will occur whether or not there is an operator using the display at the remote station(s). If the remote station has an operator displaying values in Read Mode or Program Mode, it may not be apparent that the system has entered Startup Mode and the unit will not display the Phase Sequence Test.

All the units will immediately begin running the phase sequence test and display the following:

----------	----------
SEQ TEST	SEQ TEST
LI 1I 2I	LI 1I
----------	----------
(Three terminal)	(Two terminal)

The letter 'L' indicates the local station, "1" indicates remote station one, and " 2" indicates remote station two. Each station identification is followed by either and 'I" for invalid, a "P" for pass or a "F" for fail.
Each relay runs the phase sequence test and transmits the results to the other stations.

The display will show a valid result after about ten seconds. The unit should show all units passing this test for at least ten seconds, before continuing to the next step of the Startup Mode procedure.

STEP 2.
At this point the user should shunt phase A current as shown in Figure 8-5. Even though the 3I0 phase controller senses the change in current, the Phase Sequence Test will continue to show pass on all stations if the 3I0 controller is phased properly. Note that the 3I0 fault detector LED may light at this time and that this is not a problem.

STEP 3.
The user should now remove the shunt from PHASE A current.

NOTE

ALL THREE UNITS IN A THREE TERMINAL SYSTEM SHOULD PASS THE PHASE SEQUENCE TEST BEFORE CONTINUING TO THE NEXT STEP IN THE COMMISSIONING PROCEDURE

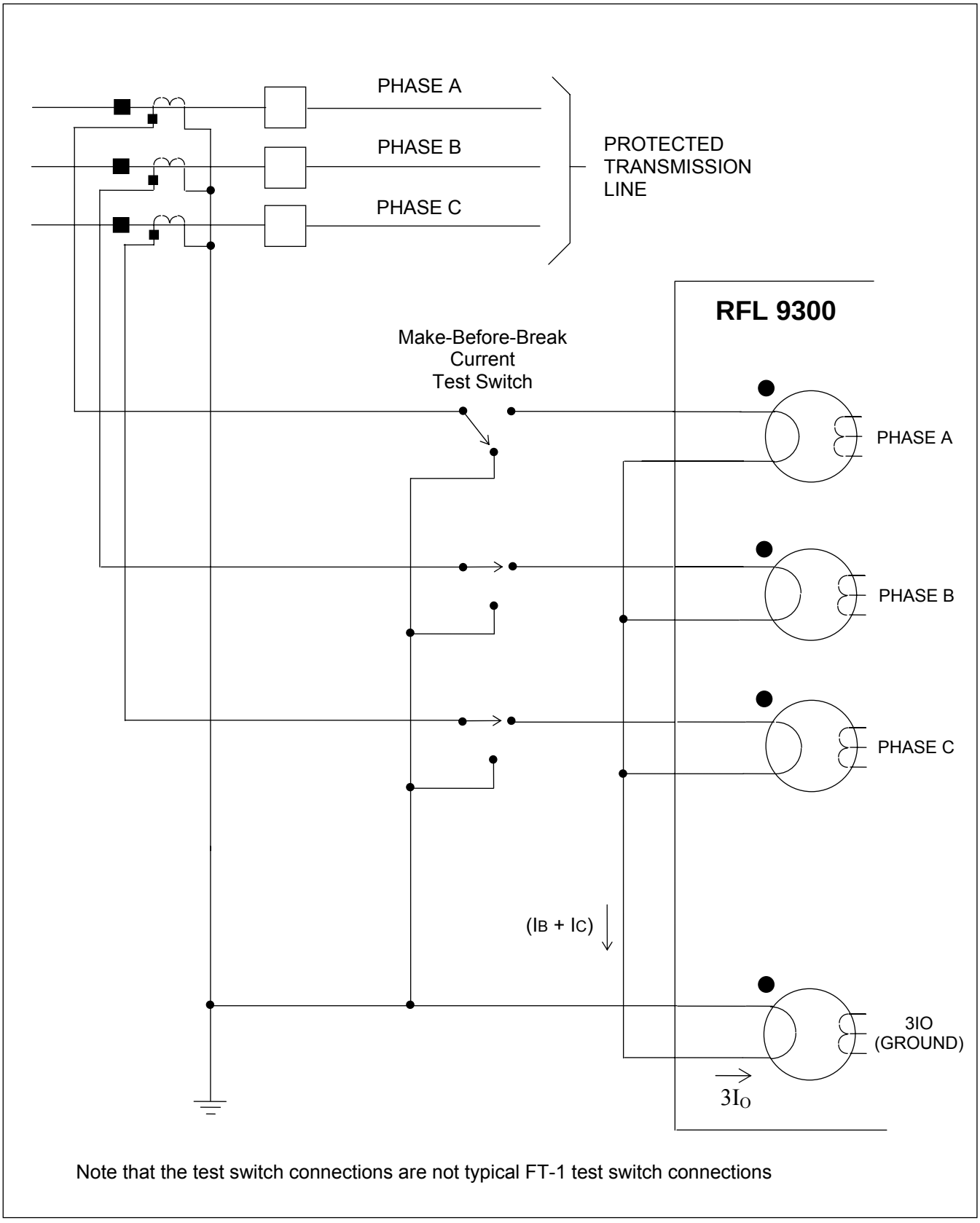


Figure 8-5. Electrical connections between RFL 9300 and current transformers on protected line (shows current test switches)

8.4.4.3 TROUBLE SHOOTING THE PHASE SEQUENCE TEST

In the process of commissioning the relay the first test that should be run and should pass is the Phase Sequence Test. This is parameter number 3 and the display will show SEQ TEST as the top line message. Essentially, the relay will measure the current flowing on Phase A Phase B Phase C and 3I0. This corresponds to the parameter numbers 5, 6, 7, and 8 “LOC IA”, “LOC IB”, “LOC IC”, and LOC3I0.

The current present should be at least 1 amp per phase and there should be no current on 3I0. (unbalances which cause currents on 3I0 of more than 0.5 amps RMS will cause the phase sequence test to fail).

The Phase sequence test determines if the phases are in the proper sequence and balanced. If the phases are in sequence and 120 degrees out of phase then the display will show LP for local unit passed the test, 1P for remote 1 unit passed the test (and 2P for remote 2 unit passed the test in a 3 terminal system). If any of the tests fail, the phases are improperly sequenced or unbalanced. This means that one or more of the Phases are connected to the wrong inputs, the wires may be inverted (i.e. backwards) or there is current on 3I0.

If the phase sequence test fails check the 3I0 current to determine if the system is unbalanced.

To check if current is present on ground, press [**ENT**] repeatedly until the display shows “LOC 3I0” on the first line. The second line should measure 0.00 amps.

To check if current is present on the other phase inputs, press [**ENT**] repeatedly until the message “LOC IA”, “LOC IB”, or “LOC IA” appears. Each should display at least 1.00 amp.

Remote stations can also be inspected using the display, however it is recommended that the Phase Sequence test be run locally at each station since shunting PHASE A current is not possible from a remote relay. Remote station(s) can be inspected for Phase A current, however this is intended to help trouble shoot the differential current test and not the Phase Sequence test.

If all the stations show at least 1.00 amps current flowing on A, B, and C and no current on 3I0, then there is a problem with the connection of phases to the relay.

Verify that the phases are connected to the correct inputs and are not inverted, and check for current on 3I0.

NOTE

ALL OF THESE PROBLEMS SHOULD BE CORRECTED BEFORE CONTINUING TO THE NEXT STEP OF THE PHASE SEQUENCE TEST.

By pressing the [ENT] key you can step through the values of the different currents to verify that phase current is still flowing and that no current is in 3I0. Measuring the phase angle between phases is done internal to the unit and can not be displayed in a meaningful way, however minor fluctuations in the difference in phase between adjacent phases will not result in a failed test.

One reason that the phase sequence test would fail at this point in the procedure is that a pair of inputs has been swapped.

8.4.4.4 DIFFERENTIAL CURRENT TEST ("DIFF CUR")

This test is for two-terminal and three-terminal systems. In a three terminal system Startup Mode is working with true currents and is not performing pre-fault load subtraction. The values that are used are true CT currents as is the case in two terminal systems.

NOTE

IT IS ASSUMED THAT WE HAVE A QUIESCENT SYSTEM, THERE ARE NO ALARMS OR ACTIVE FAULTS AND THERE ARE NO TAPPED LOADS IN THE SYSTEM. CURRENT FLOWING INTO ANY TAPS ON THE LINE WILL AFFECT THE ACCURACY OF THE "DIFF CURR" TEST.

For this test to be accurate all stations must have successfully passed the Phase Sequence Test.

The local, remote 1 and remote 2 relays should be in Startup Mode and the Phase Sequence Test should show each of the stations passing the test before proceeding.

If the user has not already done so, the shunt should be removed from the PHASE A current.

After "SEQ TEST" message is displayed, begin the Differential Current test by pressing the display keypad button [ENT] once. Alternatively, pressing keys [.] ,[4] and [ENT] consecutively at any time while in STARTUP MODE will display the Differential Current test screen.

The display will indicate "DIFF CUR" on line one and " NO DATA" on line two of the display, for up to ten seconds, or until valid data has been computed and received by the relay. The message " NO DATA" indicates that the test has begun but no valid data is yet available to display.

Once valid data has been received from all units, the display will show the largest value computed in the system. This value is the arithmetic sum or differential current between PHASE A currents at all units. Note that in a three terminal system that is properly phased, only one station will compute an arithmetic sum or differential current. This value will be displayed at all terminals. In a 2 terminal system, both stations will compute a differential current and both should be the same.

The display should show no current if all units are wired correctly. The DIFF CURR at each station will approach 0.00 amps. If the phases are connected incorrectly the display will show a value above 1 amp. Typically, this will indicate that the CT connections at the local or remote stations are phased improperly with respect to each other.

NOTE

IT IS POSSIBLE FOR A NON-ZERO VALUE OF DIFFERENTIAL CURRENT TO BE VALID IF THERE IS A TAPPED LOAD IN THE SYSTEM AND THE DIFFERENTIAL CURRENT IS EQUAL TO THE CURRENT IN THE TAP.

8.4.4.5 TROUBLESHOOTING THE DIFFERENTIAL CURRENT TEST

Under what conditions will the differential current test fail by indicating a non-zero current?

A failure in the differential current test can occur if there is a Phase rotation at one of the stations or if the phase relationship between stations shows a 180 degree inversion. If there is a phase rotation the value will be non-zero and above 1 amp. Phase rotation occurs when the 3 phases are 120 degrees apart and in sequence, but instead of having phases A, B, and C connected in the correct order, the unit is wired (B, C and A) or (C, A, and B) or some other phase rotated combination.

Another condition which will fail the differential current test is when PHASE A on one relay is connected to a different phase on one of the other relays.

If the relay displays a value much greater than 0 amps, then there is a problem that needs to be corrected before the relays may be put into service.

Verify the Addressing and communications between stations,
Verify that the phases are connected to the correct inputs,
Verify that the phase relationship between stations is correct,
Check for current on 3I0.
Be sure that there are no tapped loads in the system affecting the test.

NOTE

BRINGING A RELAY ON LINE WITHOUT CORRECTING A FAILED DIFFERENTIAL CURRENT TEST WILL CAUSE THE RELAY TO MISOPERATE.

8.4.4.5.1 Two Terminal Systems

If the terminals are wired correctly, then the current going into the local relay will be the same as the current going out of the remote 1 relay, and the differential current on Phase A will be zero. This can be seen in Figure 8-6.

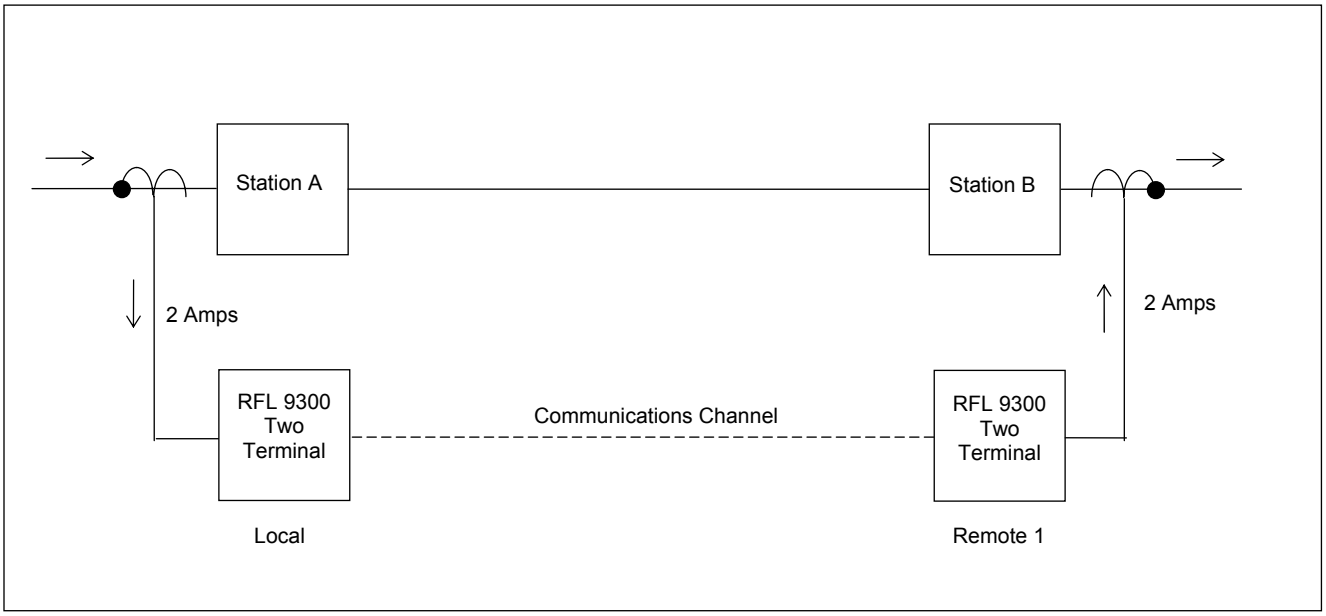


Figure 8-6. Correctly wired two-terminal system

If there is a phase inversion at the remote 1 relay, the resulting differential current indicated at both stations will be approximately double the current, or about four amps. This can be seen in Figure 8-7.

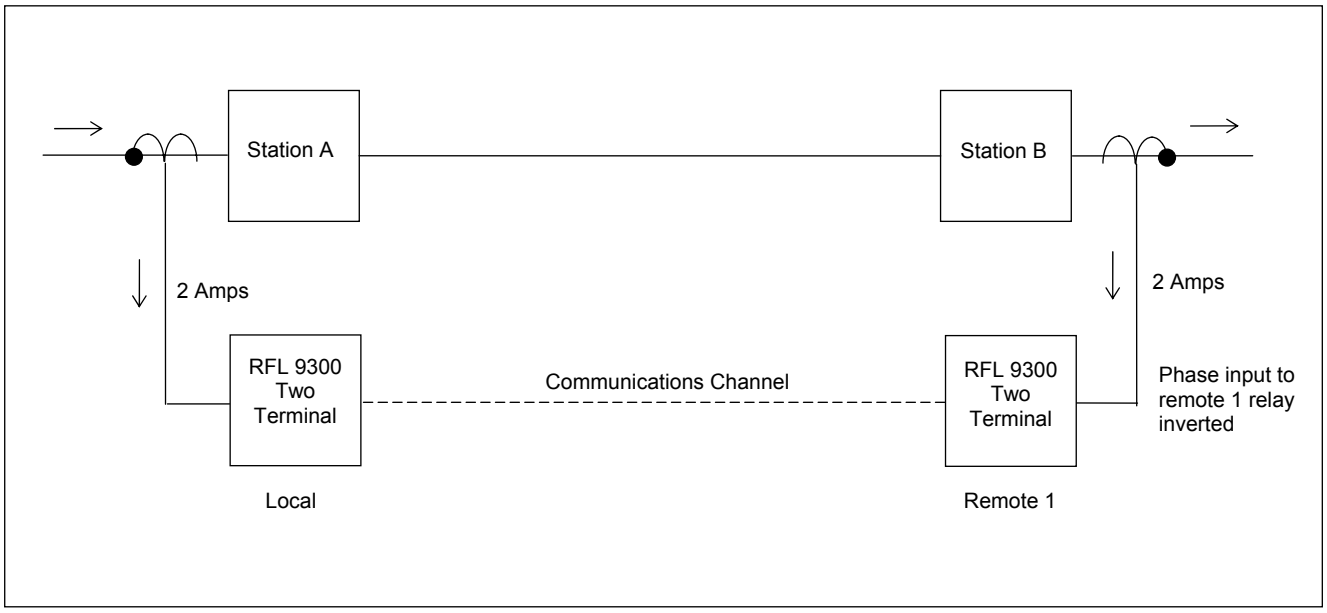


Figure 8-7. Phase inversion at remote 1 relay

If there is a phase inversion at the local relay, the resulting differential current indicated at both stations will be approximately double the current, or about four amps. This can be seen in Figure 8-8.

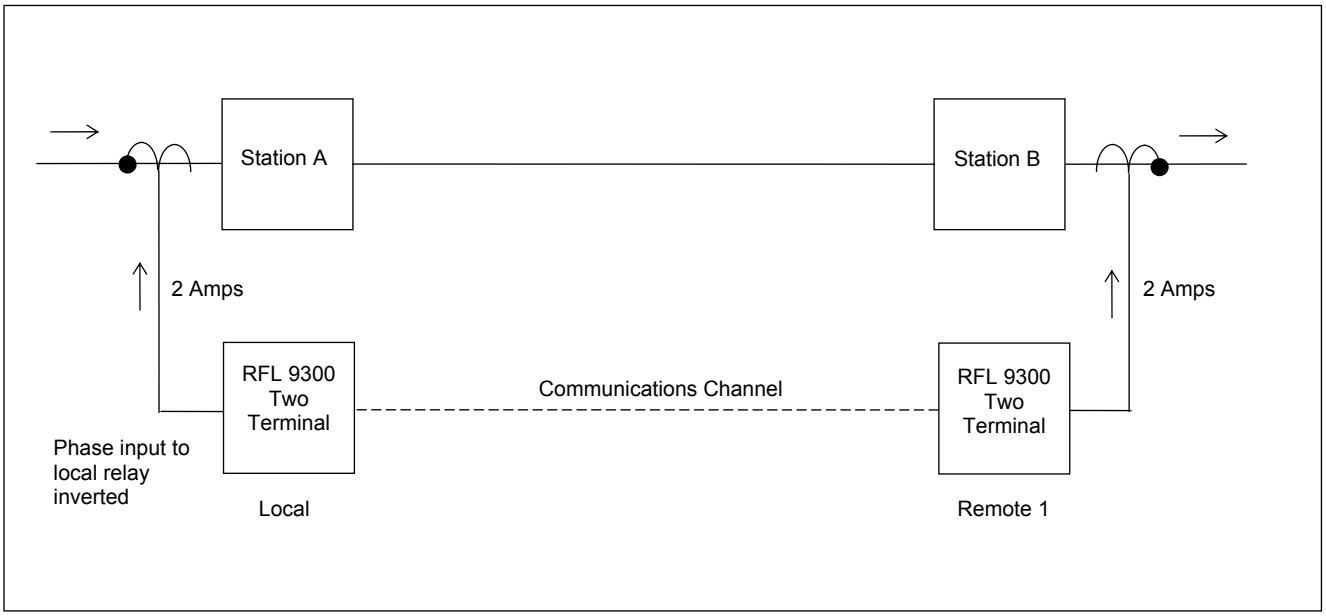


Figure 8-8. Phase inversion at local relay

8.4.4.5.2 Three Terminal Systems

If the differential current is greater that 1 AMP, the resulting differential current value may indicate which relay is incorrectly wired.

If all three relays are wired correctly then the sum of the currents going into the local and remote 2 relays will be the same as the current going out of the remote 1 relay as shown in Figure 8-9, and the differential current on Phase A will be zero.

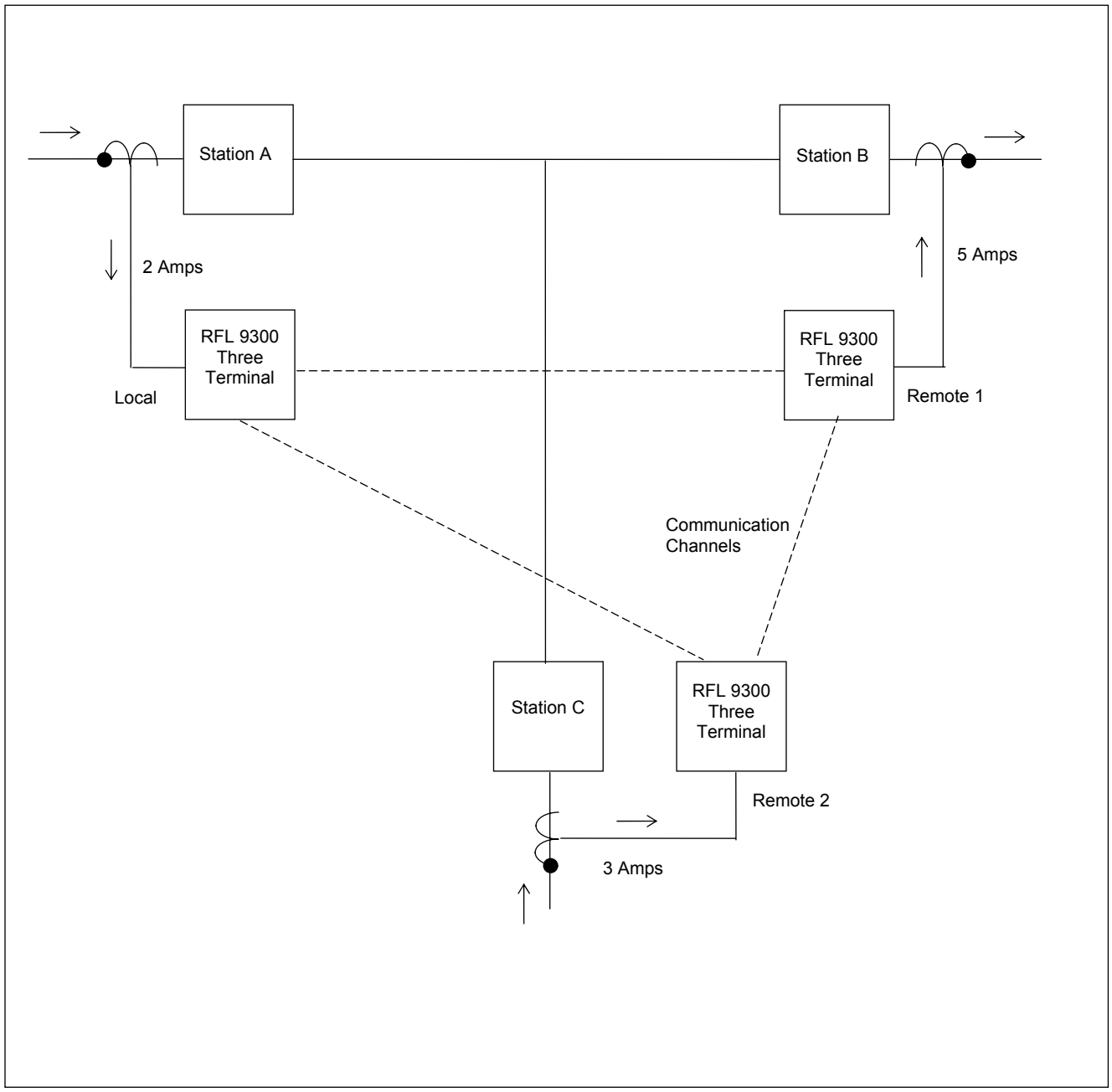


Figure 8-9. Correctly wired three-terminal system

If there is phase inversion or phase rotation at the remote 2 station as shown in Figure 8-10, the resulting Differential Current that will be displayed at all stations will be approximately double the current at remote 2, or about 6 amps.

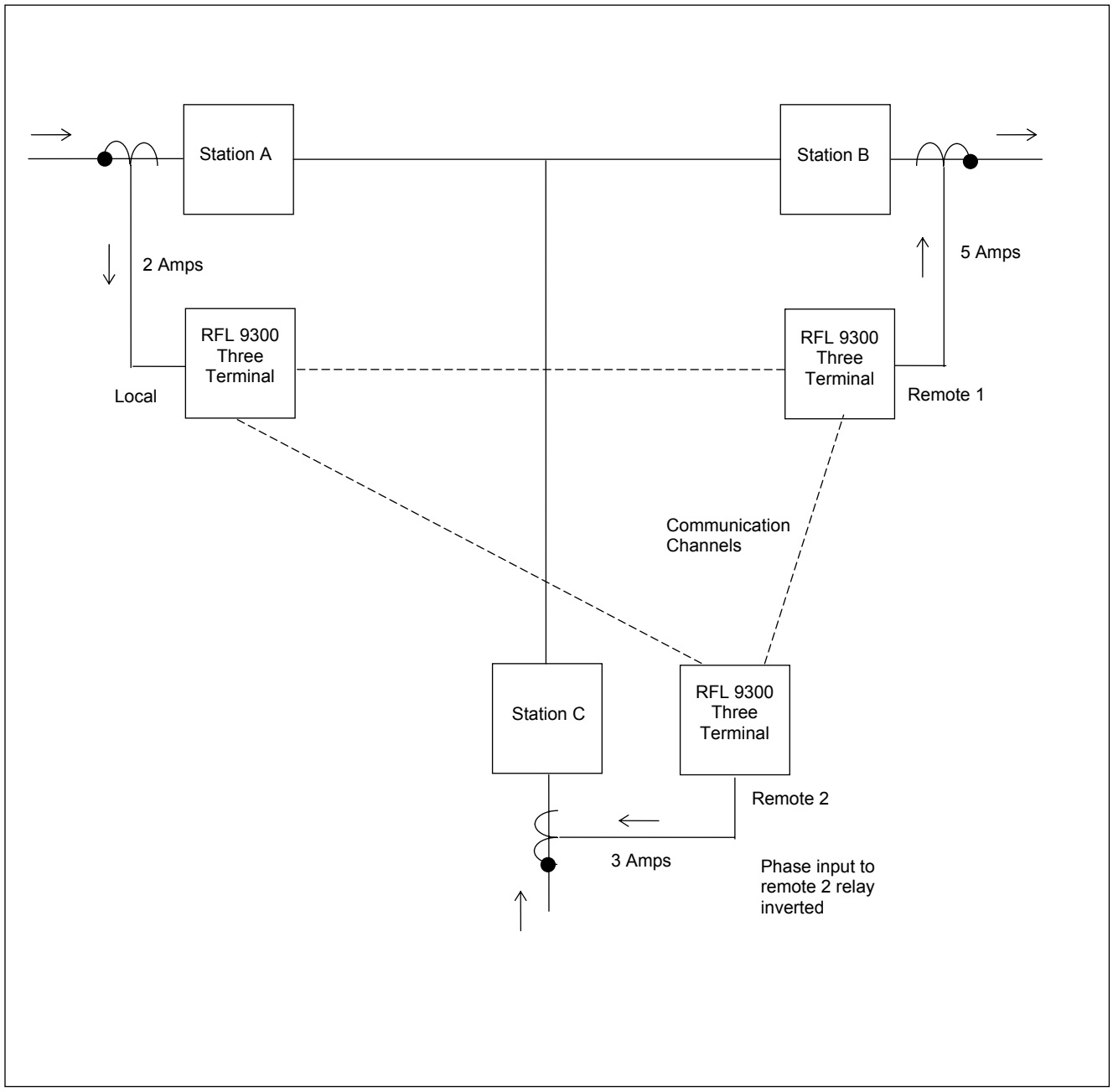


Figure 8-10. Phase inversion at remote 2

If there is phase inversion or phase rotation at the remote 1 station as shown in Figure 8-11, the resulting Differential Current that will be displayed at all stations will be approximately double the current at remote 1 or about 10 amps.

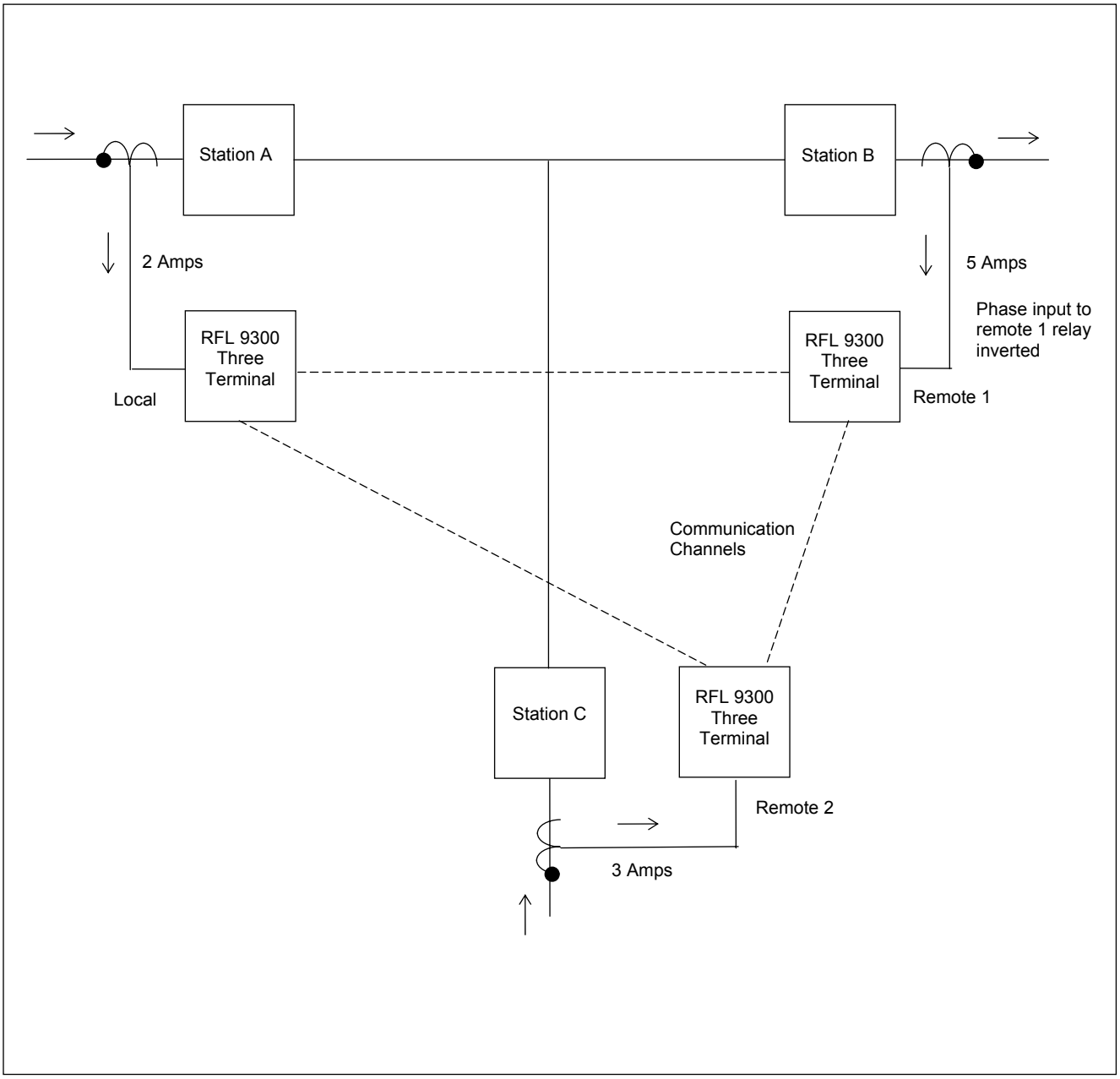


Figure 8-11. Phase inversion at remote 1

If there is phase inversion or phase rotation at the local station as shown in Figure 8-12, the resulting Differential Current that will be displayed at all stations will be approximately double the current at the local station or about 4 amps.

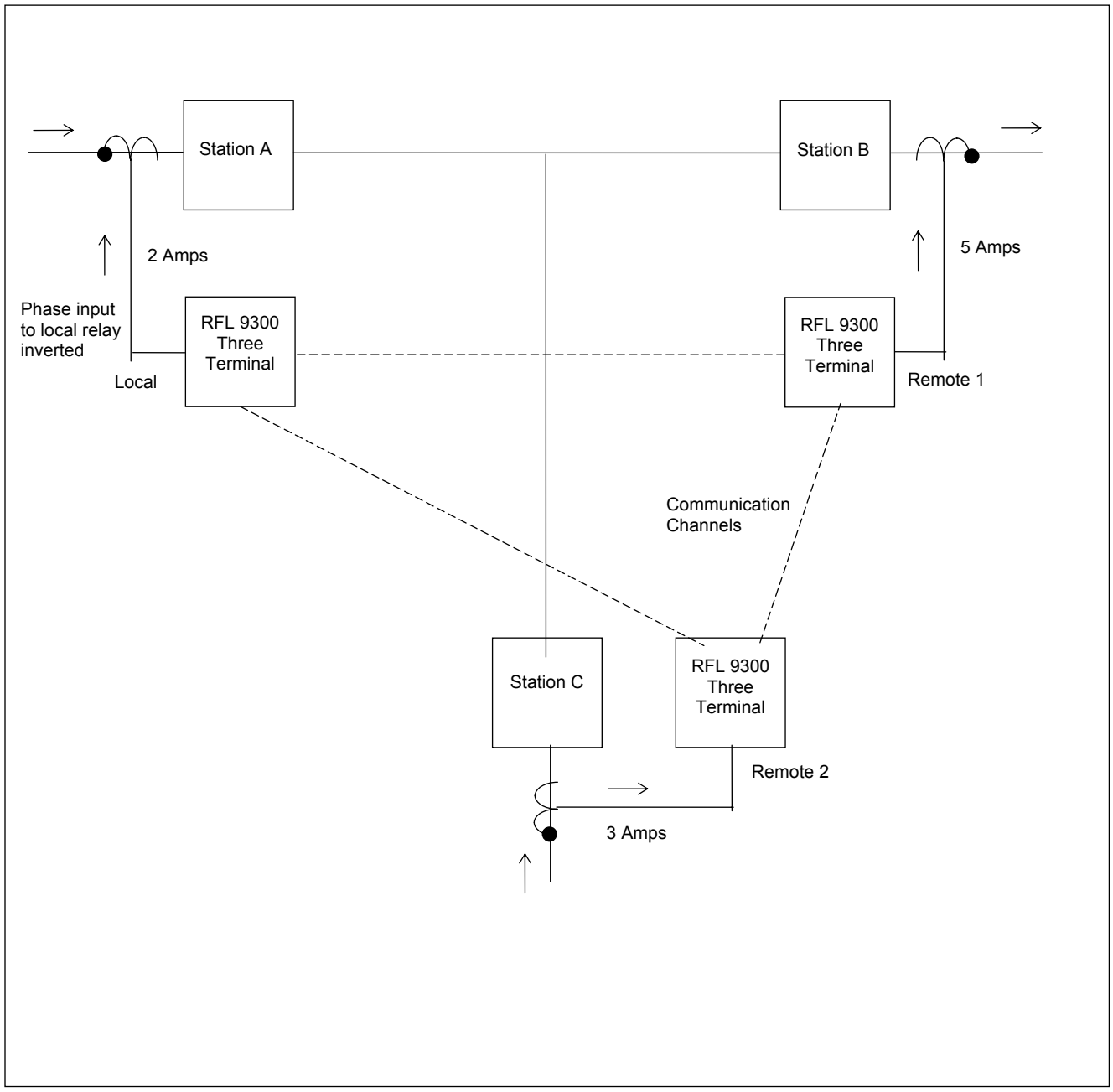


Figure 8-12. Phase inversion at local station

NOTE

THIS STARTUP MODE PROCEDURE SHOULD BE RUN AT EACH STATION TO INSURE PROPER INSTALLATION. PASSING THE PROCEDURE AT ONE STATION ONLY WILL NOT VERIFY THE WIRING ADEQUATELY. THE PHASE A SHUNT TEST PORTION OF THE PHASE SEQUENCE TEST SHOULD BE RUN AT EACH STATION.

To assist in trouble shooting any wiring problem without exiting the STARTUP Mode, the following parameters are active and may be displayed.

The display shows the parameter number for each measured value and a brief description of its meaning.

001 - Ping Pong R1 Ping-pong delay for remote 1. Equal to one-half the round-trip delay.

002 - Ping Pong R2 Ping-pong delay for remote 2. Equal to 1/2 the round-trip delay. (3 terminal only)

003 - Sequence Test Phase Sequence Test.

004 - Diff Cur Test Differential Current Test.

005 - Local I A Local Phase A current.

006 - Local I B Local Phase B current.

007 - Local I C Local Phase C current.

008 - Local 3I0 Local $3I_0$ current.

009 - Remote #1 I A Remote #1 Phase A current.

013 - Remote #2 I A Remote #2 Phase A current. (3 terminal only)

8.4.4.6 EXITING THE STARTUP MODE

To exit the STARTUP Mode, proceed as follows:

1. Press the **[.]** key, followed by the **[0]** and **[ENT]** keys.
   The word "EXIT" will appear on the top line of the display, with the word "ENABLE" on the bottom line.

2. Press the **[ENT]** key.
   The message "SEC CODE" will appear on the display. This means that you must enter a security code before the RFL 9300 will exit the STARTUP Mode. Press the [.], [1], [3], [5] and [ENT] keys to enter the required security code.

The RFL 9300 will go through a sequence similar to a front panel button reset that will last for about six seconds. All the lamps will illuminate for a few seconds. Then the RFL 9300 will return to the STANDBY mode and the display will return to the moving dot pattern. The security code in step 2 is required because exiting the STARTUP Mode re-enables the system trip functions, and should not be done casually.

8.5 FINAL COMMISSIONING

After all other procedures in this section have been performed, use the following procedure to place the RFL 9300 relays in service.

1. Place one RFL 9300 in the PROGRAM display mode, and set all of its programmable parameters to the required settings for your application. (Refer to Section 4 of this manual for further information.)

2. Place the RFL 9300 back in the STANDBY display mode.
   The display will return to the moving dot pattern.

3. Repeat steps 1 and 2 at the other RFL 9300 unit(s).

4. Reconnect all the trip output wires that were disconnected during system testing.

The RFL 9300 relay system is now in service.

SECTION 9: DISPLAY MODULE

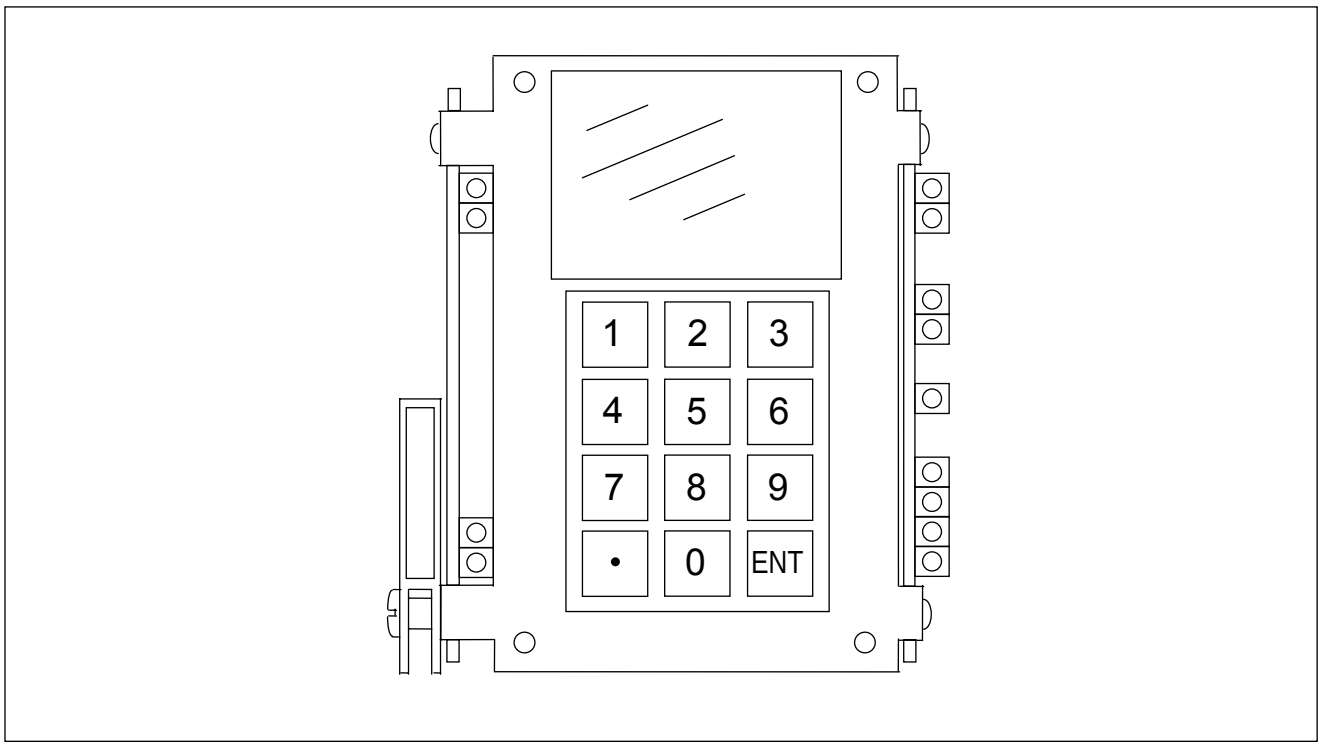


Figure 9-1. RFL 9300 display module for horizontal chassis

9.1 INTRODUCTION

The RFL 9300 display module (93B DISPLAY), shown in Figure 9-1, serves as the user interface to the RFL 9300. Entries on its keyboard place the RFL 9300 into one of its four operating modes. Programmable parameters can be set by keyboard entries while the RFL 9300 is in the PROGRAM mode.

Each display module contains three main assemblies (See Table 9-1). The display controller board is described below, the oscillography board is described in paragraph 9.3 of this section, and the front panel assembly is described in paragraph 9.4 of this section.

9.2 DISPLAY CONTROLLER BOARD

9.2.1 DESCRIPTION

The display controller board performs the following functions:

1. Accepts inputs from the keyboard on the front panel.

2. Operates the display on the front panel.

3. Controls its LED indicators, and the indicators on the oscillography board.

Table 9-1. RFL 93B Display Module, general information

Model Designator	Assembly Number
Display Module (93B DISPLAY) horizontal	106320-2
Display Module (93B DISPLAY) vertical	106320-3
Display Controller Board	106325-2
Oscillography Board	106330
Front Panel Assembly	106335

4. Reads the TRIP/DTT inputs and the current sense inputs on the oscillography board.

5. Retrieves IRIG-B values from the oscillography board for time tagging events.

6. Supplies trip commands to the oscillography board to trigger oscillography storage.

7. Retrieves oscillography values for downloading.

8. Operates the audible sounder on the oscillography board.

9. Stores information on the programmable variables and the state of all sealed-in LED indicators in non-volatile RAM.

10. Communicates with the RFL 93B SV Supervisor Module over an RS-485 interface bus.

11. Communicates with the outside world through a front or rear RS-232 port.

12. Controls the TRIP DISABLE/ENABLE line.

13. Uses the Trip Release algorithm programmed by the operator to unlatch output trip signals.

9.2.2 CONTROLS AND INDICATORS

Figure 9-2 shows the location of all controls and indicators on the display controller. These controls and indicators are described below. Those described as front-panel controls are accessible with the display module installed in the chassis; all others are accessible when the display module is removed from the chassis, or is placed on card extenders.

LED INDICATORS

DS301 PROTECTION - Front-panel indicator; lights red when protection is disabled; the color changes to green when protection is enabled.

DS302 TRIP - Front-panel indicator; four individual LEDs that light red to show which phase(s) are faulted; Phase A (A), Phase B (B), Phase C (C), or ground (G).

DS303 DTT TX - Front-panel indicator; lights red when a DTT signal is sent to the remote terminal.

DS304 DTT RX - Front-panel indicator; lights red when a DTT signal is received from the remote terminal.

DS305 BACKUP - Front-panel indicator; lights red when the RFL 9300 goes into the back-up mode. This will happen when Parameter 20 (BACKUP) has been enabled, and a communications failure occurs. (The RFL 9300's alarm relay will also change states.)

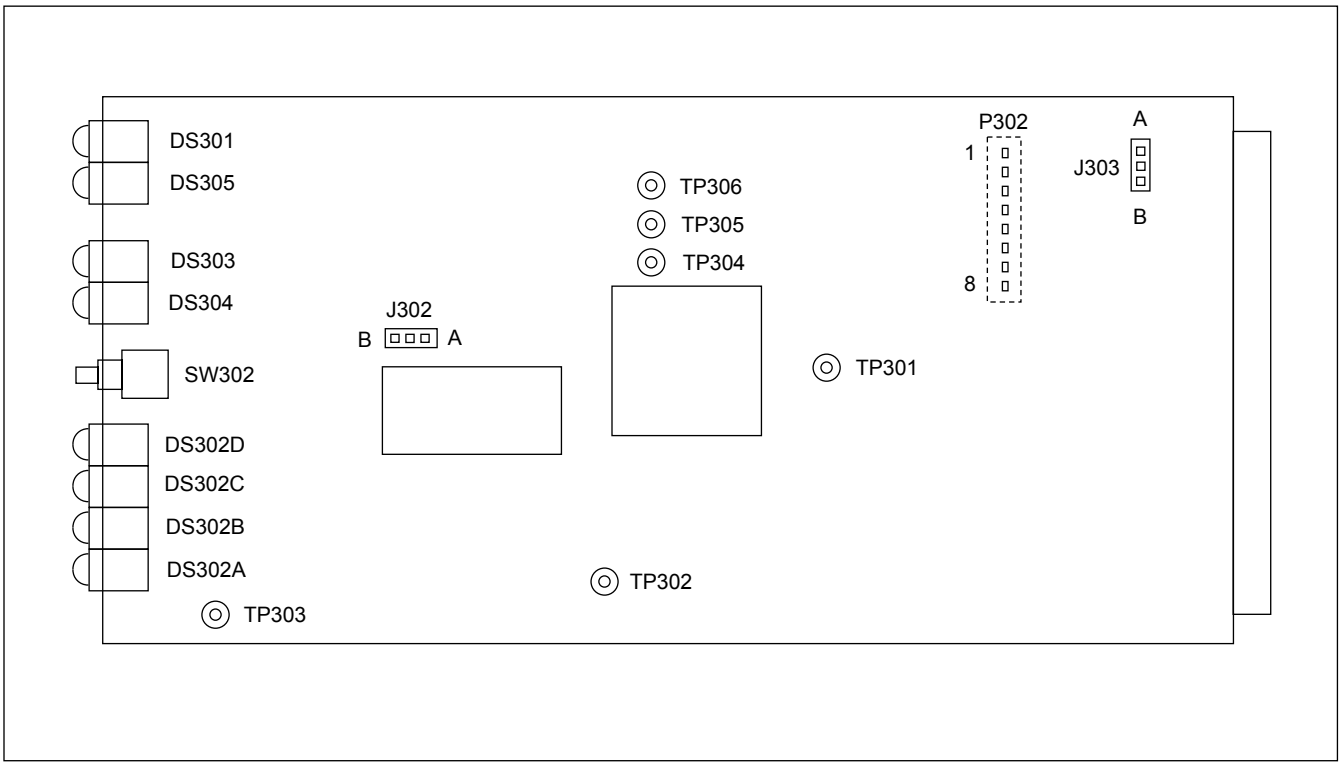


Figure 9-2. Controls and indicators for display controller board, used in RFL 9300 display module

CONNECTORS

P302 When the RS-232 front panel interface board (106755) is installed, a cable from the board plugs into P302 of the display controller board. When the RS-232 front panel interface board (106755) is not installed, programmable jumpers (P/N 98306) are used to jump pins 4 & 5 and 6 & 7 of P302.

JUMPERS

J302 Set at the factory according to the type of device installed for U314 and U315. Position A is used for 27C256 devices, and Position B is used for 27C512 devices. **Do not change the setting of this jumper, unless U314 and U315 are being replaced with another device type.**

J303 Install Jumper in position A when front panel interface board (106755) is installed.
Install Jumper in position B when front panel interface board (106755) is not installed.

SWITCHES

SW302 RESET - Front-panel control; manually resets all latched LED indicators.

TEST TURRETS

TP301 Monitoring point for watchdog timer pulses.

TP302 Monitoring point for 8-MHz microcontroller clock.

TP303 Ground

TP304 Monitoring point for local 2-kHz or 1.667-kHz clock.

TP305 Monitoring point for RX DATA line.

TP306 Monitoring point for TX DATA line.

9.2.3 THEORY OF OPERATION

For the following discussion refer to Figure 9-7, sheets 4 and 5.

MICROCONTROLLER

The heart of the display controller is 16-bit microcontroller U309. The 80C196KD microcontroller U309 has 1024 bytes of internal RAM, and operates with a 16-MHz crystal. It also contains a serial port, 48 I/O lines and two 16-bit timer/counters. The program and data for U309 are stored in EPROM's U314 and U315. Jumper J302 is set according to the type of devices installed for U314 and U315. J302 is placed in Position A for 27C256 devices, and in position B for 27C512 devices. When 27C512 devices are used, the most significant address line is controlled by microcontroller U309, allowing it to bank switch the program memory. U312 and 313 are used to latch the address bus using the ALE signal from the microcontroller. External data is stored in a 2Kx8 RAM chip (U311). Address decoding for the peripheral devices is accomplished in programmable logic chip U305. Data to and from these devices is buffered by U316 and U317, respectively.

MICROCONTROLLER SUPERVISOR

Microcontroller supervisor U308 contains a watchdog timer. Its output (U308-7) is normally high. About once every 2 ms, microcontroller U309 pulses its I/O port 1.0 output (U309-19) several times. This keeps the watchdog timer from timing out and causing U308-5 to go low. If, for some reason, the watchdog timer does time out, U309 is reset and begins its program again. During the reset, the communications control buffer U304 and two gates of quad buffer/line driver U301 are disabled by U318-6. This prevents any false signals during startup.

RS-232 COMMUNICATIONS

The /BACK UP EN, /CTS, /DCE, and /SC_RDY signals from the RFL 93A SV Supervisor Module and the RS-232 bus are entered through octal buffer U304, and are fed to U309's I/O port 0. The RS-232 TX is only enabled when U309-10 drives the /CTS signal low. /AUX LATCH DIS, /LOR LATCH DIS, /RTS, and /DC_RDY are output signals. They are derived from U309's I/O port 1, and are transmitted to the Relay I/O or the RFL 93B SV through U304.

RS-485 COMMUNICATIONS

RS-485 communications is provided through RS-485 transceiver U303. U303 has a separate enable for its transmitter and receiver sections. Before U303's transmitter can be active, the /RTS line must be high, driving U302-10 low. In addition, the /SC_RDY line must be low, making U302-4 high. U303's receiver is enabled whenever /DC_RDY is made low; this means the display controller is able to receive communications from the RFL 93B SV.

Incoming RS-232 signals (/RX DATA) are buffered by U301 and fed to U309's serial input. The /DC_RDY signal must be high in order to enable the U301 buffer. The 60/50 HZ signal is brought in through NAND gate U318 and fed to the microcontroller I/O port 2.3 (U309-44). An audible sounder is activated by I/O port 2.6 (U309-33); its drive signal is buffered by U318.

OSCILLOGRAPHY BOARD COMMUNICATIONS

Communications between the two boards is accomplished over a bi-directional eight-bit data bus (DOSC_0 through DOSC_7). The display controller board is the master, and therefore controls the data direction. The inverted direction control signal to the oscillography card appears on pin C24. Communications is initiated by the display controller, which sets the bus direction to transmit and then writes the command data into data latch U324. The transmit flag register U306 is also set by the write signal, and is output on C26 to tell the oscillography card that data has been written to the bus. The transmit flag is reset by the oscillography card when the data has been read. The display controller will then set the bus direction to receive and wait for data from the oscillography card, which will be indicated by a receive flag signal appearing on pin A25. When this occurs, the microcontroller will read the data through U323, which will also reset the receive flag signal from the oscillography card by placing a reset signal on pin A26. The receive process will continue if more than one byte of data was requested.

LED INDICATORS

The /TRIP DIS LED signal comes from the Relay I/O through edge connector terminal P1-C14; however, U309 originates the signal through the TRIP DIS output at edge connector terminal P1-A14. When TRIP DIS is high, U309 will also make U322-13 high. This causes PROTECTION indicator DS301 to light red when the /TRIP DIS LED signal goes low. When the /TRIP DISABLE LED signal is high, U309 will make U322-13 low thereby causing DS1 to light green. Data latch U322 also drives LED indicators DS302A through DS304.

FRONT PANEL INTERFACING

The WRDISPL signal latches the lower eight address lines onto octal flip-flop U320; the data bus data is latched onto octal flip-flop U321. This information is used to write to the displays on the RFL 93B DISPLAY's front panel, and read the keypad. The keypad readings are brought in from the front panel through hex inverting Schmitt trigger U319 and fed to the microcontroller's I/O port 0.

SINGLE-POLE CHASSIS INTERFACING

Initialization

The Display Controller works hand-in-hand with the Supervisor Controller to both initialize and monitor the interface between the RFL 9300 relay and the Single-Pole chassis.

The Supervisor will test SP_DETECT. If this line is low it indicates that the single-pole chassis is present in the system. In that case, the generic Single-Pole chassis alarm (Alarm #54) will become active and the alarm message will be transmitted to the Display Controller. Meanwhile the Display Controller, on power-up, will always transmit at least one 16-bit initialization message to the Single-Pole chassis whether the chassis is present in the system or not. This message will contain trip targets, current sense targets, and the trip release code all previously stored in non-volatile ram. The message will also contain a bit signifying whether the system is configured single-pole or 3-pole and a bit signifying whether or not the targets should be loaded or ignored. The Display Controller will send the initialization message to the Single-Pole chassis at 750ms intervals until it receives a message from the 93B SV rescinding the Single-Pole chassis alarm. If the Single-Pole chassis is not in the system the Supervisor will not have transmitted the alarm message in the first place and only one initialization message will be sent.

Once the Single-Pole logic has been initialized, it will begin transmitting a 16-bit status word to the Supervisor at 264ms intervals. The transmission will be asynchronous with a start bit (active low), 16 data bits and one stop bit (active high) The message bits will be synchronized to the system clock and will be in the mark, or logic 1 condition when no messages are being transmitted. SV_DAT will be utilized to transmit the message. The first time that the Supervisor detects one of these messages and determines that it is valid it will transmit a message to the Display Controller rescinding the single-pole alarm. When the Display Controller receives this message it will cease sending the initialization message to the Single-Pole chassis.

Normal Operation after Initialization is Complete

The single-pole logic will continue to transmit its 16-bit status message to the Supervisor at 264ms intervals. The Supervisor will not accept any status changes as valid until it receives two identical messages in succession. If a status single-pole logic Logic to the Display Controller. As long as there are no changes in single-pole logic status detected by the Supervisor, byte 2 of every 10th status message (2.64 second interval) will be transmitted to the Display Controller. This is to insure that the Display Controller will not miss a change in single-pole logic status.

When the Display Controller receives this message it will be saved in NV RAM. If the trip release code received from the Supervisor differs from the latest code known to the Display Controller, or if a new trip release code is programmed by the operator, the initialization message will be transmitted to the Single-Pole chassis with bit 7 = logic 1. This will signal the single-pole logic to ignore the target and mode bits but to accept the Trip Release code.

If the Supervisor has gone 600 ms without receiving a status message, or if it detects that the single-pole jumper position on the Supervisor card has changed, it will declare a SINGLE-POLE CHASSIS ALARM locally and transmit the alarm message to the Display Controller. As long as this alarm remains active the Display Controller will transmit the initialization message with bit 7 = logic 0, at 750ms intervals.

Display Controller Reset

If there are no SINGLE-POLE CHASSIS ALARMS once the Power-Up interval is completed, the only time that the interface message will be transmitted with bit 7 set equal to a logic 0, is when the Display Controller transmits a reset signal. In that case the message will be transmitted to the single-pole logic with all target bits set at logic 0.

Single Pole Logic Reset

Note that when the single-pole logic is configured for three-pole trip, the reset signal is ignored if there is an active trip on any phase. This differs from the single-pole case where the reset signal is processed on a phase-by-phase basis.

9.3 OSCILLOGRAPHY BOARD

9.3.1 DESCRIPTION

The oscillography board in the RFL 9300 display module performs the following functions:

1. Drives an audible sounder that alerts the operator of an alarm condition.
2. Reads the TRIP and DTT inputs.
3. Reads the Auxiliary Current Transformer (ACT) outputs.
4. Controls the LED indicators along its front edge.
5. Constantly reads and stores current values from all four ACT's.
6. Stores oscillography records of 200 ms of current values.
7. Outputs the stored oscillography record upon request from the display controller.
8. Demodulates the IRIG-B signal for use in the oscillography board and the display controller board.

9.3.2 CONTROLS AND INDICATORS

Figure 9-3 shows the location of all controls and indicators on the oscillography board. These controls and indicators are described below. Those described as front-panel controls are accessible with the RFL 93B DISPLAY installed in the RFL 9300 chassis; all others are only accessible when the RFL 93B DISPLAY is removed from the chassis, or is placed on card extenders.

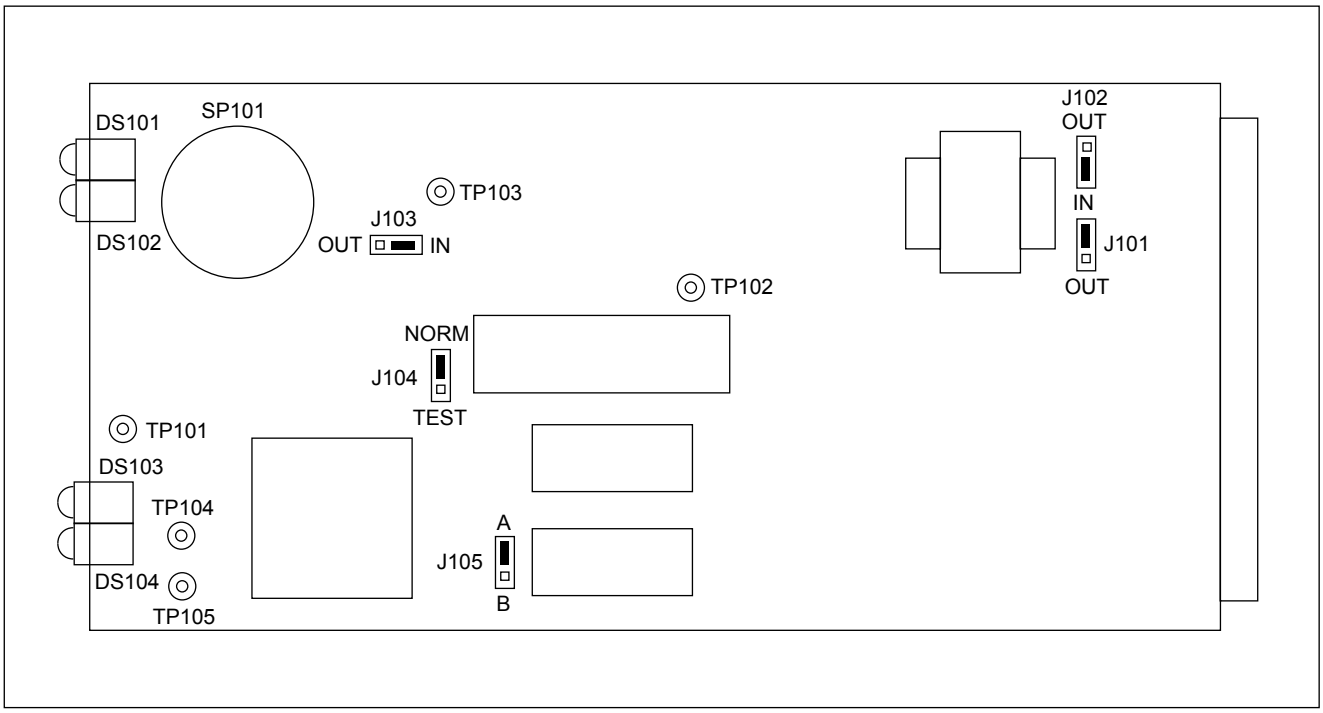


Figure 9-3. Controls and indicators for oscillography board, used in RFL 93B DISPLAY module

LED INDICATORS

DS101 TRIP 1 - Front-panel indicator; lights when the TRIP 1 relay contacts are carrying trip currents of at least 0.2 amperes. This indicator is latched in non-volatile memory, and can only be reset by pressing RESET switch SW302 on the display controller board.

DS102 TRIP 2 - Front-panel indicator; lights when the TRIP 2 relay contacts are carrying trip currents of at least 0.2 amperes. This indicator is latched in non-volatile memory, and can only be reset by pressing RESET switch SW302 on the display controller board.

DS103 LOR 1 - Front-panel indicator; lights when the LOR 1 dc trip circuit carries currents of at least 0.2 amperes. This indicator is latched in non-volatile memory, and can only be reset by pressing RESET switch SW302 on the display controller board.

DS104 LOR 2 - Front-panel indicator; lights when the LOR 2 dc trip circuit carries currents of at least 0.2 amperes. This indicator is latched in non-volatile memory, and can only be reset by pressing RESET switch SW302 on the display controller board.

TEST TURRETS

TP101 Ground reference

TP102 IRIG-B test point

TP103 IRIG-B test point

TP104 ACTEL probe test point

TP105 ACTEL probe test point

JUMPERS

101	Enables or disables the IRIG-B demodulator section (leave in the "in" position for modulated IRIG-B signals).
J102	Enables or disables the IRIG-B demodulator section (leave in the "in" position for modulated IRIG-B signals).
J103	Enables or disables the IRIG-B demodulator section (leave in the "in" position for modulated IRIG-B signals).
J104	Enables or disables the watchdog timer (leave in the "norm" position for normal operation).
J105	Selects the size of the EPROM to be used (leave in the factory selected position).

9.3.3 THEORY OF OPERATION

For the following discussion refer to Figure 9-7, sheets 1 and 2.

MICROCONTROLLER

The heart of the oscillography board is U125, an 80C320 8-bit microcontroller. It runs a program stored in EPROM U116. It has access to the battery backed, non volatile RAM, U117. The microcontroller is monitored by a microcontroller supervisor circuit, U115. This circuit contains power up circuitry and a watchdog timer. The controller timing is crystal controlled by Y101.

PROGRAMMABLE LOGIC

An ACTEL FPGA (field programmable gate array) provides the logic for many of the functions of the oscillography board. It forms registers which can be written to by the controller. It also decodes the addresses for the registers and external hardware registers. The ACTEL, U124, also provides control signals to the bidirectional data bus with the display controller. It allows the processor to read the state of the trip and current sense signals for display and recording purposes.

U109 is a programmable logic device that contains AND gates and fixed OR gates. It will latch the AUX TRIP and LOR TRIP signals active, even when the input trip or DTT signal disappears.

DISPLAY CONTROLLER COMMUNICATIONS

The oscillography board acts as a slave and responds to transmission requests from the Display Controller board. (Refer to the section "Oscillography Board Communications" above for more details.) The receive flag is generated inside the Actel chip, along with most of the control signals. Inverter U120 is used to buffer the signals.

IRIG-B RECEIVER

The oscillography board also contains a circuit to demodulate the IRIG-B signal from an amplitude modulated 1Khz carrier. This circuit is made up of transformer T101, U108, U112, and U113. If jumpers J101, J102 and J103 are in the "in" position, this circuit strips off the carrier and leaves a digital representation of the IRIG-B signal. If the jumpers are in the "out" position, the signal is passed to the processor without demodulation. This is used when an unmodulated signal is supplied to the RFL 9300.

TRIP SIGNALS

Optoisolators, U101-U105 are used to electrically isolate the trip and DTT input signals from the logic circuits.

OSCILLOGRAPHY DATA

A four channel 8-bit analog to digital converter, U119 is used to convert the analog current information into a digital format. The input signals pass through a first order low pass filter and a voltage clamping circuit for noise filtering and U119 for input protection. ADC U119 samples all inputs simultaneously, and then converts the data in sequence. The results are read out by U125 after all conversions have been completed. The -5 volt power for U119 is generated from the -15 volt supply by linear voltage regulator U118.

BUZZER

When the /BUZZER signal at edge connector terminal P1-A8 goes low, transistors Q101 and Q102 turn on. This provides drive voltage for audible sounder SP101. SP101 is normally turned on and off intermittently by the microcontroller on the display controller.

9.4 FRONT PANEL

For the following discussion refer to Figure 9-7, sheet 3.

9.4.1 THEORY OF OPERATION

DISPLAY

The front panel contains an alphanumeric display that is under the control of the microcontroller on the display controller.

Buffer/line drivers U201 and U204 accept the data and address buses from the display controller. Decoder/demultiplexer U205 decodes the STROBEA0 and STROBEA1 inputs, A6 and A7 from the microcontroller. It uses these inputs to select either the U202 display or the U203 display, to reset both displays, or to enable the keypad. U205 is enabled by the STROBE input going low. This is the microcontroller's I/O port 2.5.

The FLASH input (A5) from the microcontroller goes to transistor Q206. Jumper J202 can be used to invert the FLASH signal. J202 must be in Position B (non-inverting) if Hewlett-Packard displays are used. If Siemens displays are used, J202 must be in Position A (inverting).

KEYPAD

The front panel also has a keypad for user entries. When STROBEA0 and STROBEA1 are both high and STROBE is low, U205-7 is made low. This enables the strobing of the keypad. The A0 and A1 lines from the microcontroller scan each column in the keypad. For example, when both A0 and A1 are low, U205-12 will be low. This will turn on the transistor connected to it. RZ201-10 will be low, placing a low on the first keypad column (pin K). If any key on this column is pressed, one or more of the KEY0 through KEY3 lines will be made low. This allows the microcontroller to determine which keys are pressed. The KEY0 through KEY3 lines are connected to pull-up resistors on the display controller. If the keypad column is made low but no key is pressed, the KEY0 through KEY3 lines will all be high. The microcontroller continuously scans all the columns on the keypad looking for pressed keys.

Table 9-2. Replaceable parts for display controller board, used in RFL 9300 display module. (Assembly No. 106325-2)

Circuit Symbol (Figs. 9-4 & 9-7)	Description	Part Number
	CAPACITORS	
C301-324, 329	Capacitor, ceramic, 0.01μF, GMV, 50V	1007 1366
C325, 326	Capacitor, ceramic, 22pF, 5%, 200V	0125 22205
C327, 328	Capacitor, tantalum, 33μF, 10%, 10V	1007 1142
	RESISTORS	
R301, 302, 307-310, 312-314, 323	Resistor, metal film, precision, 10K, 1%,1/4W	0410 1384
R303, 304, 311, 319-321	Resistor, metal film, precision, 1K, 1%, 1/4W	0410 1288
R316, 322	Resistor, metal film, precision, 221Ω, 1%, 1/4W	0410 1225
R317	Resistor, metal film, precision, 1.62K, 1%, 1/4W	0410 1308
R318	Resistor, metal film, precision, 845Ω, 1%, 1/4W	0410 1281
RZ301, 304	Resistor network, 10K, 5R/PKG, SIP	32664
RZ302, 303, 305, 307	Resistor network, 10K, 9R/PKG, SIP	32622
RZ306	Resistor network, 221Ω, 9R/PKG, SIP	30165
	SEMICONDUCTORS	
DS301	Opto device, LED, bi-color, red-green	102801
DS302	Opto device, LED	30162
DS303-305	Opto device, LED, red	99294
Q301	Transistor, silicon, PNP,2N3906	21565
U301	IC, MOS, quad buffer/line driver	0615 292
U302	IC, MOS, quad 2-input NOR gate	0615 160
U303	IC, interface transceiver, RS-485	0680 14
U304	IC, MOS, tri-state octal buffer	0615 176
U305	IC, MOS, PEEL, 25NS	0615 365
U306	IC, MOS, Dual D-flip flop	0615 166
U307, 319	IC, MOS, Hex inverter, Schmitt trigger	0615 242
U308	IC, Peripheral, Microprocessor supervisor	0635 27
U309	IC, CHMOS, Microcontroller	0615 459

>> table continues on next page <<

Table 9-2 continued. Replaceable parts for display controller board, used in RFL 9300 display module

Circuit Symbol (Figs. 9-4 & 9-7)	Description	Part Number
	SEMICONDUCTORS - continued.	
U311	IC, MOS, Nonvolatile timekeeping RAM	0615 437
U312, 313	IC, MOS, Octal, tri-state latch	0615 382
U314, 315	IC, MOS, EPROM, 32Kx8, 70NS	call factory
U316, 317	IC, MOS, Octal, buffer/driver	0615 381
U318	IC, MOS, Quad 2-input NAND gate	0615 159
U320, 321, 324	IC, MOS, Octal, tri-state, D-flip flop	0615 298
U322	IC, MOS, Octal, D-flip flop	0615 383
U323	IC, MOS, Octal, tri-state, non-inverting, buffer/line driver	0615 297
	MISCELLANEOUS COMPONENTS	
J301	Connector, JK male, 26-pin, vertical	95617
J302	Connector, header, single 3-circuit	32802 3
SW302	Switch, SPDT, RT angle, PC board mount	98488
TP301-306	Test point, terminal, orange	98441 3
Y301	Crystal, quartz, 16.000 MHz	30297

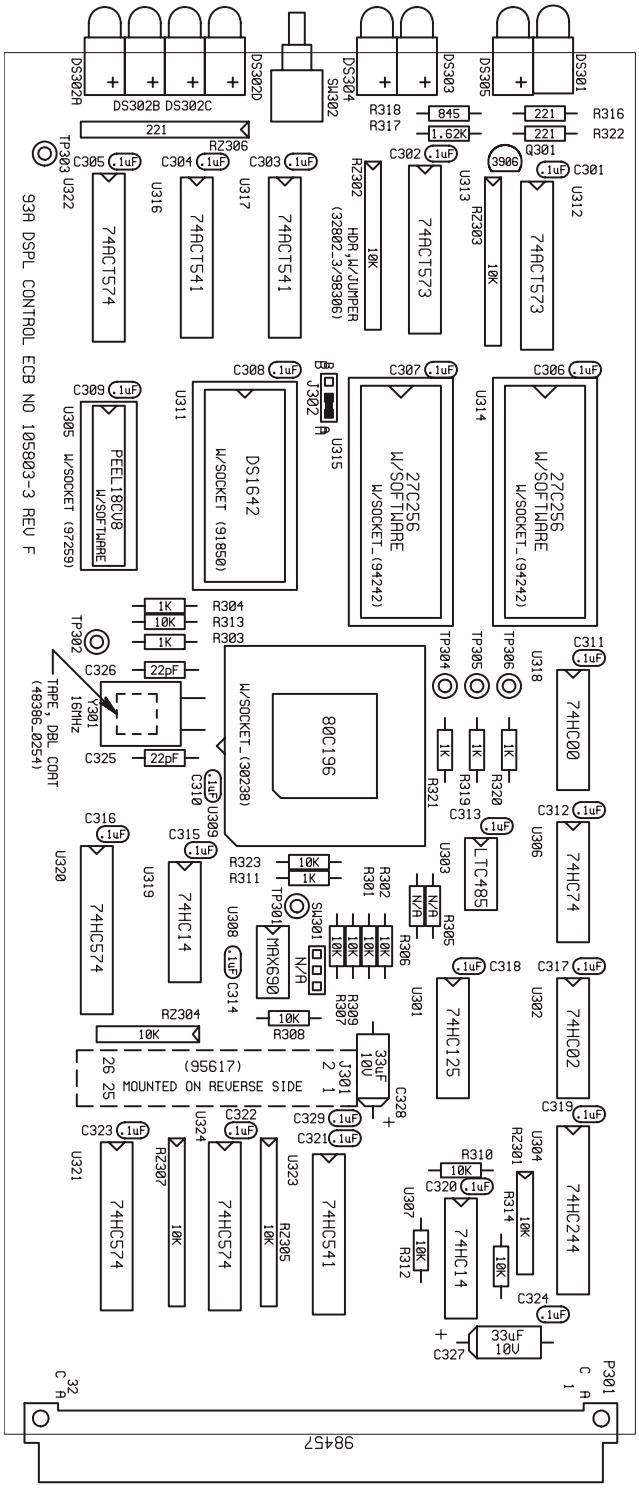


Figure 9-4. Component locator drawing for display controller board, used in RFL 9300 display module (Assembly No. 106325-2)

Table 9-3. Replaceable parts for oscillography board, used in RFL 9300 display modules (Assembly No. 106330)

Circuit Symbol (Figs. 9-5 & 9-7)	Description	Part Number
	CAPACITORS	
C101	Capacitor, tantalum, 33μF, 10%, 10V	1007 1142
C102, 103	Capacitor, electrolytic, 47μF, 20%, 25V	1007 1578
C104-106, 110, 113-118, 131-149	Capacitor, ceramic, 0.1μF, GMV, 50V	1007 1366
C107-109, 123-126	Capacitor, ceramic dipped, 0.01μF, 5%, 100V	1007 1645
C111	Capacitor, tantalum, 3.3μF, 20%, 35V	1007 1260
C112, 128, 129	Capacitor, electrolytic, 47μF, 20%, 16V	1007 1629
C119	Capacitor, polystyrene, .0039μF, 2%, 10V	5115 15
C120, 121	Capacitor, ceramic, 33pF, 10%, 200V	0125 23301
C122	Capacitor, ceramic, 120pF, 5%, 200V	0125 21215
C127	Capacitor, tantalum, .33μF, 10%, 35V	1007 1281
C130	Capacitor, tantalum, 4.7μF, 20%, 20V	1007 711
	RESISTORS	
R101	Resistor, metal film, precision, 5.9KΩ, 1%, 1/4W	0410 1362
R102	Resistor, metal film, precision, 3.01KΩ, 1%, 1/4W	0410 1334
R103	Resistor, metal film, precision , 9.76KΩ,1%, 1/4W	0410 1383
R104	Resistor, metal film, precision , 3.16KΩ, 1%, 1/4W	0410 1336
R105, 127, 154, 155	Resistor, metal film, precision , 1KΩ, 1%, 1/4W	0410 1288
R106	Resistor, metal film, precision , 24.9KΩ, 1%, 1/4W	0410 1422
R107	Resistor, metal film, precision , 49.9KΩ, 1%, 1/4W	0410 1451
R108	Resistor, metal film, precision, 7.15KΩ, 1%, 1/4W	0410 1370
R120, 126, 132, 135-138, 143-146	Resistor, metal film, precision, 4.99KΩ, 1%, 1/4W	0410 1355
R121, 122	Resistor, metal film, precision, 909Ω, 1%, 1/4W	0410 2284
R123, 124, 134, 151-153	Resistor, metal film, precision, 10KΩ, 1%, 1/4W	0410 1384
R125	Resistor, metal film, precision, 20KΩ, 1%, 1/4W	0410 1413
R128	Resistor, metal film, precision, 1432Ω, 1%, 1/4W	0410 2253
R129	Resistor, metal film, precision, 8.25KΩ, 1%, 1/4W	0410 1376
R130	Resistor, metal film, precision, 237KΩ, 1%, 1/4W	0410 1516
R131	Resistor, metal film, precision, 2.0 MegΩ, 1%, 1/4W	0410 1605
R133	Resistor, metal film, precision, 4.02KΩ, 1%, 1/4W	0410 1346

Table 9-3 continued. Replaceable parts for oscillography board, used in RFL 9300 display module

Circuit Symbol (Figs. 9-5 & 9-7)	Description	Part Number
	RESISTORS (continued)	
RZ101, 102	Resistor network, 10K, 5R/PKG, SIP	32664
RZ103	Resistor network, 220Ω, 5R/PKG, SIP	99117
RZ104, 105	Resistor network, 10K, 8R/PKG, SIP	95571
RZ107	Resistor network, 1K, 5R/PKG, SIP	101439
RZ108	Resistor network, 680Ω, 7R/PKG, SIP	98448
RZ109	Resistor network, 6.8K, 9R/PKG, SIP	101776
	SEMICONDUCTORS	
CR101-110	Diode, silicon, 1N914B/1N4448	26482
Q101	Transistor, silicon, PNP, 2N3906	21565
Q102	Transistor, NPN, 40V, 2N4401	42574
U101-105	Opto device, photo isolator, 4N35	47104
U106, 113	IC, MOS, timer	0615 441
U107	IC, MOS,dual retriggerable, monostable multivibrator	0615 282
U108	IC, linear, quad, comparator	0620 241
U109	IC, MOS, PEEL	call factory
U110, 123	IC, MOS, octal, buffer/driver	0615 381
U111	IC, linear, adjustable, precision, shunt regulator	0620 320
U112	IC, analog switch, quad, SPST, CMOS	0605 17
U114	IC, MOS quad, buffer/line driver	0615 292
U115	IC, peripheral, microprocessor, supervisor	0635 31
U116	IC, EPROM 8Kx8	0630 47
U117	IC, non-volatile SRAM, 8Kx8	0630 67
U118	IC, linear, voltage regulator, neg 5V	0620 210
U119	IC, A/D convertor, high speed	0625 35
U120	IC, MOS, hex inverter, schmitt trigger	0615 242
U121	IC, MOS, quad 2-input NOR gate	0615 160
U122	IC, MOS, octal, tri-state, D-flip-flop	0615 298
U124	IC, MOS, field programmable, gate array	0615 422
U125	IC, microprocessor, 8-bit	0640 36
	MISCELLANEOUS COMPONENTS	
DS101-104	Optoelectric device, red LED	99294
SP101	Audible warning device	30048
T101	Transformer	34199
TP101-105	Test point	98441 3
Y101	Crystal	30555

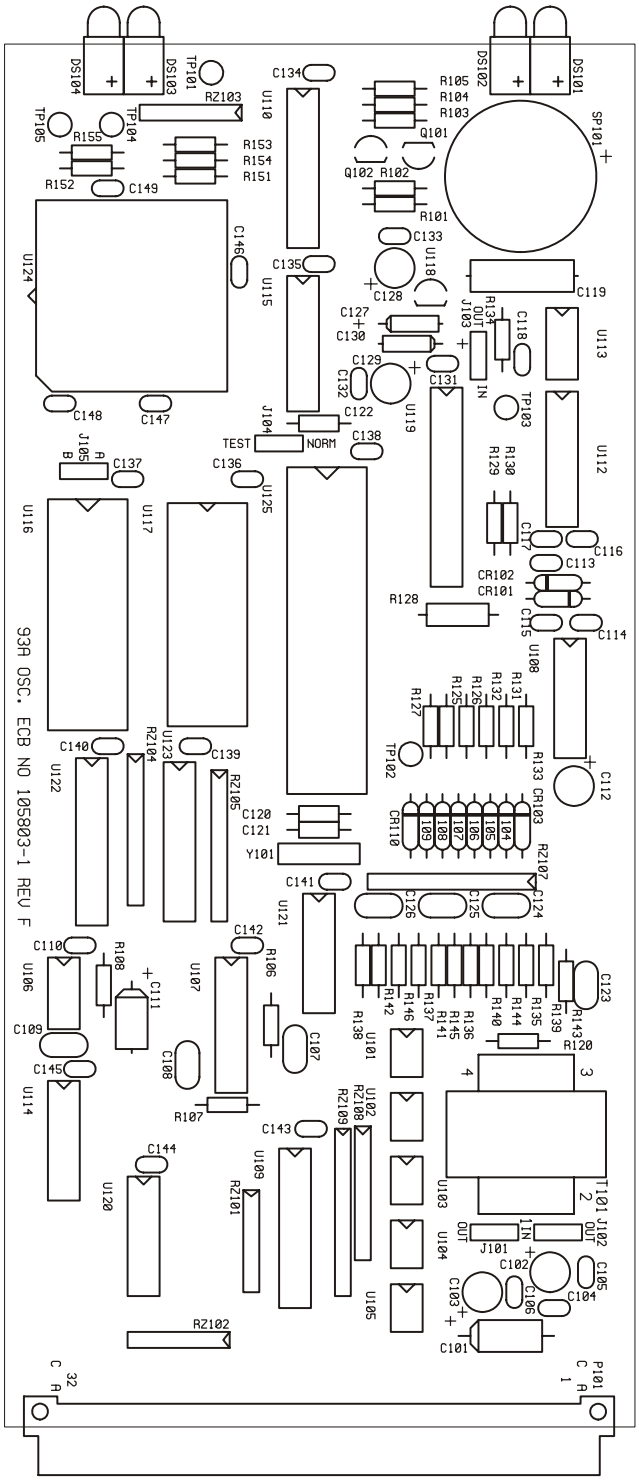


Figure 9-5. Component locator drawing for oscillography board, used in RFL 9300 display module (Assembly No. 106330)

Table 9-4. Replaceable parts for front panel assembly, used in RFL 9300 display module (Assembly No. 106335)

Circuit Symbol (Figs. 9-6 & 9-7)	Description	Part Number
	CAPACITORS	
C201-205	Capacitor, ceramic, 0.1μF, 10%, 50V	0130 51041
C206-208	Capacitor, tantalum, 33μF, 10%, 10V	1007 1142
	RESISTORS	
R201	Resistor, metal film, precision, 2.21K, 1%, 1/4W	0410 1321
RZ201	Resistor network, 2.2K, 9R/PKG, SIP	103897
	SEMICONDUCTORS	
U201, 204	IC, MOS, Octal, 3st, Noninverting, BFR/LD	0615 297
U202, 203	Display, alphanumeric, 8-digit	101285
U205	IC, MOS, 2 to 4 line decoder, multiplexer	0615 269
U206	Transistor array, MPQ 2222	49478
	MISCELLANEOUS COMPONENTS	
J202	Jumper connector, programmable	98306
KP201	Keypad, 12-button (3 x 4), Post Mtg.	101232

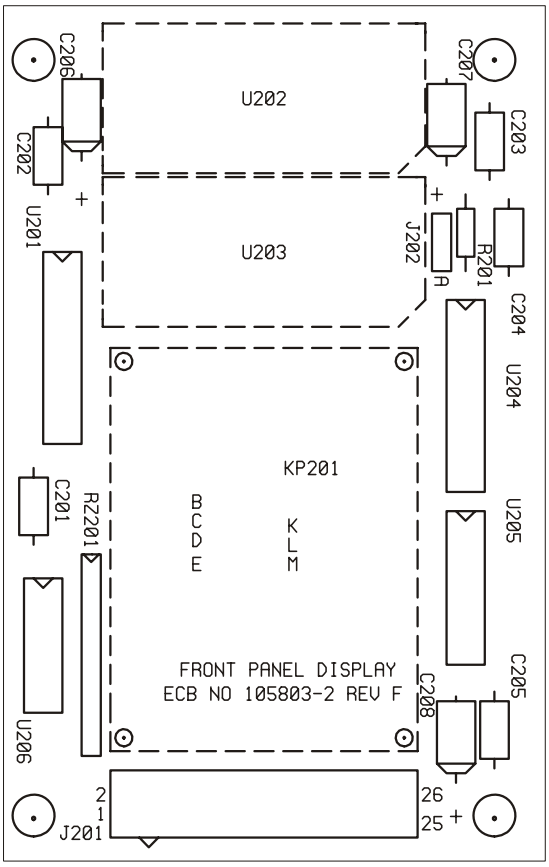


Figure 9-6. Component locator drawing for front panel assembly, used in RFL 9300 display module (Assembly No. 106335)

Figure 9-7. Oscillography Board, part of RFL 9300 display module (Assembly No. 106330; Schematic No. D-106764-A) Sheets 1 of 5 through 5 of 5

Please see Figure 9-7, Sheets 1 of 5 through 5 of 5, in Section 32: Schematics

SECTION 10: SUPERVISOR CONTROLLER MODULE

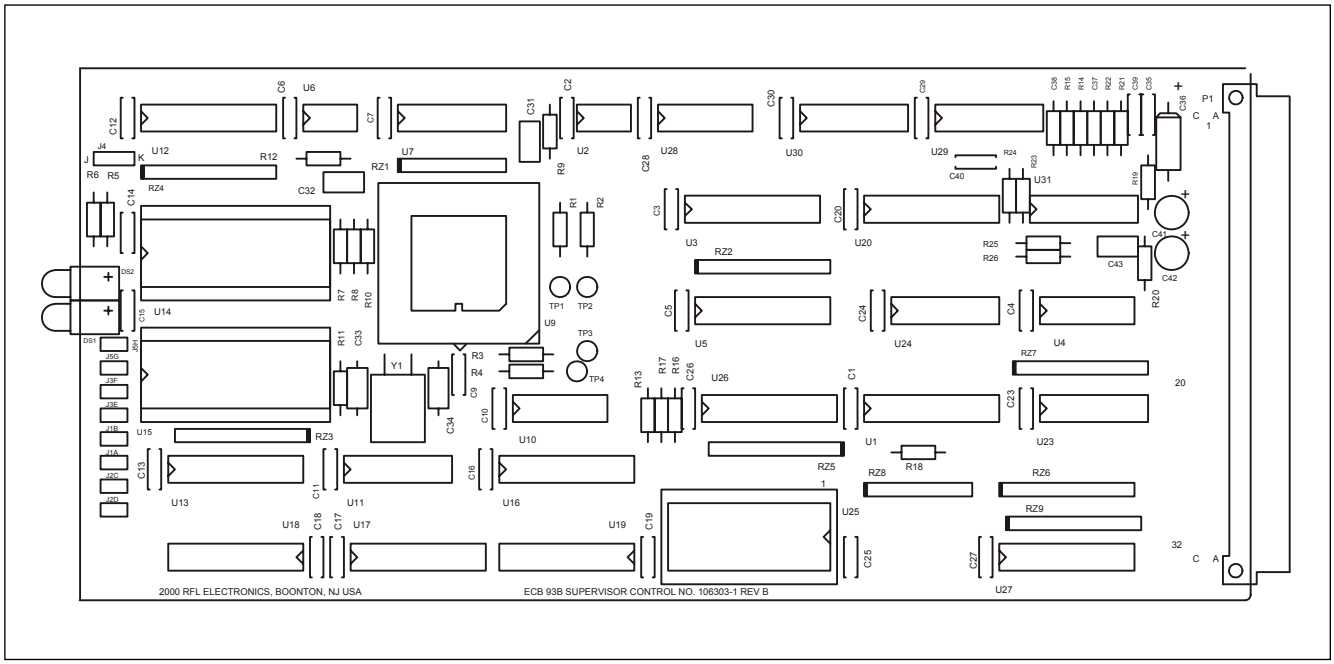


Figure 10-1. RFL 9300 supervisor controller module

10.1 DESCRIPTION

The RFL 93B SV supervisor controller module (Figure 10-1) serves as the communications hub for the RFL 9300. The supervisor controller module generates the system clock, which is the "heartbeat" of all RFL 9300 activity. During power-up, the supervisor controller module controls the initialization of all modules in the RFL 9300. It also monitors and controls many system-wide functions, such as alarms and Direct Transfer Trip (DTT) signals.

10.2 CONTROLS AND INDICATORS

Figure 10-2 shows the location of all controls and indicators on the RFL 93B SV. These controls and indicators are described below. Those described as front-panel controls are accessible with the RFL 93B DISPLAY installed in the RFL 9300 chassis; all others are only accessible when the RFL 93B SV is removed from the chassis, or is on a card extender.

LED INDICATORS

DS1 SYS ALARM - Front-panel indicator; lights red when a system-wide problem is detected.

DS2 TX/RX ALARM - Front-panel indicator; lights red when a communications failure is detected.

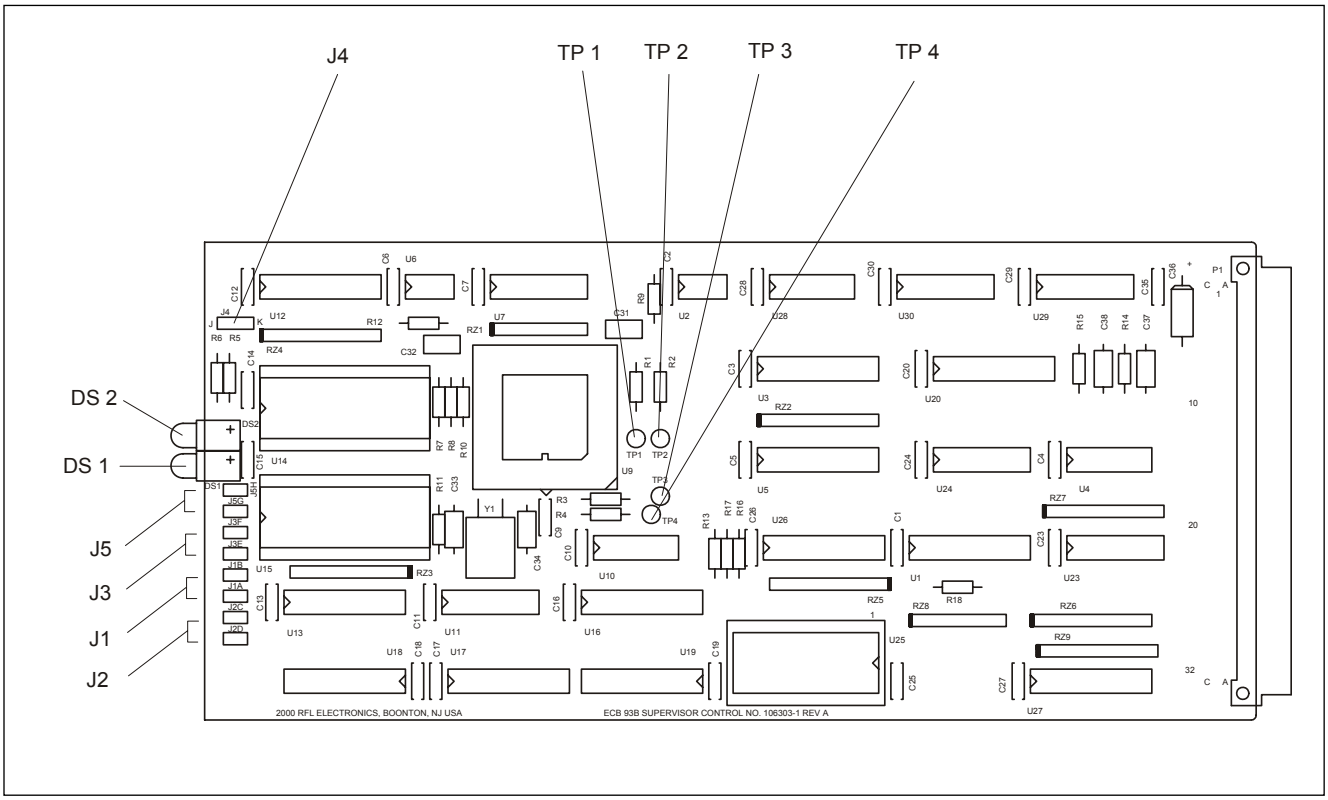


Figure 10-2. Controls and indicators, RFL 9300 supervisor controller module

CONFIGURATION JUMPERS

J1 Selects operating frequency: Position A for 60 Hz, Position B for 50 Hz.

J2 Selects terminal configuration: Position C for two-terminal, Position D for three-terminal.

J3 Selects ACT current: Position E for 5 Arms, Position F for 1 Arms.

J4 Set at the factory according to the EPROM devices installed for U14 and U15. Position J is used for 64K devices, and Position K for 256K devices. **Do not change the setting of this jumper in the field, unless U14 and U15 are being replaced with another device type.**

J5 Selects 3-pole or single pole tripping: Position G for 3-pole, Position H for single pole.

TEST TURRETS

TP1 Monitoring point for positive-going watchdog timer strobe signal.

TP2 Monitoring point for the system clock signal. This will be a 2.0-kHz signal if J1 is in Position A, or 1.667-kHz signal if J1 is in Position B. If the relay is configured for 3-terminal operation, the system clock is phase locked at 33 x the line frequency in Hz.

TP3 Monitoring point for the low-going READY/BUSWIDTH signal that signifies the start of a memory mapped I/O bus cycle.

TP4 Measuring point for the microcontroller's CLKOUT signal. It should be 8 MHz, or half the internally-generated clock frequency.

10.3 THEORY OF OPERATION

The RFL 93 SV Supervisor Controller Module serves as the communications hub of the RFL 9300. It also performs the following tasks:

1. It generates the system clock, which is the "heartbeat" of all RFL 9300 activity.

2. It controls the initialization of all modules in the RFL 9300 during turn-on.

3. It monitors and controls many system-wide functions, such as alarms, Direct Transfer Trip (DTT) signals, reclose block signals, and the single-pole trip algorithms.

4. It works hand-in-hand with the Display Controller to both initialize the single-pole chassis and to monitor the serial link between the single-pole chassis and the RFL 9300. (See 9.2.3 - Single-Pole Interfacing - for an explanation of this process).

10.3.1 SYSTEM CLOCK

Timer 2, an on-board software timer, is programmed to generate the system clock. The Supervisor Controller checks jumper J1's setting to determine the desired clock frequency. If J1 is set for 50-Hz operation, a 1.667-kHz system clock signal will be generated. If J1 is set for 60-Hz operation, system, a 2-kHz clock signal will be generated. If the relay is configured for 3-terminal operation, the system clock is phase locked at 33 x the line frequency in Hz. The clock signal is output on the HS0.0 pin, and is transmitted to the Phase Controllers, communications controllers, and single-pole logic through U3-3. This clock signal is used to synchronize the Phase Controller, communications controller, single-pole logic and Supervisor Controller programs.

10.3.2 INTERBOARD COMMUNICATIONS MANAGEMENT

The primary task of the RFL 93B SV is to control the flow of messages between the RFL 93B PC Phase Controller Modules, the RFL 93B Display Controller Module, and the RFL 93B CC Communications Controller Module. The Supervisor Controller algorithms are executed by 16-bit microcontroller U9. U9's 16-MHz clock signal is generated by an on-board clock oscillator, controlled by crystal Y1 and capacitors C33 and C34.

The RFL 93B PC Phase Controller Modules and the RFL 93B CC Communications Controller Module do not communicate directly with the RFL 93B SV, or with each other. These three controllers use a non-volatile static RAM (U25) for this purpose. Each controller is assigned two "mailboxes" within U25: READ and WRITE. Each mail-box contains eight bytes, but only the first three are presently used. Messages passed between controllers all have the same three-byte format: an address byte, a data byte, and a security code byte. The security code byte is calculated as the "XOR" of the address and data bytes. All three bytes are stored in the appropriate mailbox.

At the start of each 0.5-ms program interval, the RFL 93B SV will write whatever messages it has available for a given controller to that controllers' READ mailbox in U25. U25 is treated as memory-mapped I/O. Whenever the target memory address is greater than or equal to 8000H (AD15 = logic 1), a memory-mapped I/O operation occurs. When this signal is high, EPROMS U14 and U15 are disabled by their Chip Select line. This signal is also inverted by U10A and applied to the READY/BUSWIDTH input pins of the microcontroller, with the following results:

1. The RFL 93B SV treats all memory-mapped I/O bus cycles as eight-bit operations.

2. Two wait states are inserted into each memory-mapped I/O bus cycle to accommodate U25's rather slow 200-ns access time

When the RFL 93B SV wants to write to the mailboxes, the following events take place:

1. The SUPR/W signal (U3-12) is set to a logic 1. This gives the RFL 93B SV's WR, RAM, and RD control signals access to U25 through multiplexer U24. At the same time, buffer U23's outputs are disabled; this isolates U25 from the external controller strobe signals. The MEMADDR output signal from PLD U20-14 goes low to enable address latch U19.

2. The PCR/WEN signal (U3-7) is set to a logic 1. This signal clears INT-X address counter U28A to the INT-A address (000), and disables INT-X address decoder device U30. The memory access control timer U29 is disabled by the PLDs TIMEREN signal (U20-13).

3. The COMM_EN signal (U3-9) is set to a logic 1 to isolate the RFL 93B CC module (or modules) from U25.

At the start of the I/O bus cycle, the target address appears on the microcontroller pins AD15 to AD0 (U9-45 through U9-60), and on the outputs of address latches U12 and U13. When ALE goes low, the target address remains latched on the output pins of these devices. The low READY/BUSWIDTH signal on U10-1 also enables decoder device U11B. SUPR/W is the B address signal for this decoder, while AD14 is the A address signal. Therefore, if AD14 is a logic zero, U11-10 will be low. This does two things: U11A is enabled, and the RAM signal goes low.

The RAM signal serves as the Chip Enable signal for U25. If AD13 is low during a bus cycle, address line ADR100 will go low and provide one enable signal to U17. When the RD signal goes low, U25's outputs will be enabled and the data from the memory location addressed by U19 will appear on the bi-directional data bus and the input of U17. The low RD signal provides the remaining enable signal required by U17 and enables the memory data to appear on its output pins and be read by microcontroller U9. Memory address 8XXXH is used for memory-mapped I/O mailbox READ cycles, and memory address AXXXH is used for mailbox WRITE cycles. U10B decodes a WRITE strobe (the WRSTRB signal) for bi-directional data bus latch U18. Memory address CXXXH will enable the Output Control latch (U16) to be accessed through U10C, U10D, and the ADR110 signal.

After the RFL 93B SV is finished writing data to the mailbox registers, it grants the phase controllers access to the memory. The SUPR/W signal is reset to logic zero. This enables the outputs of input buffer U23, allowing externally-generated strobe signals access to U25 through multiplexer U24. The PCR/WEN signal is also reset to logic zero. This enables U28A along with INT-X decoder U30. U28A supplies the interrupt address to decoder U30. When the PCR/WEN signal first goes low the address supplied to U30 by U28A will be "000." U30 will decode this signal and generate a communications interrupt signal to the Phase A controller through the INT-A signal. The TIMERSTR signal from the PLD (U20-17) disables U30's input address lines when U28A is clocked by the BLKADDR signal (U20-16). This prevents glitches on the output of U30 that would provide false interrupt signals to the phase controllers. U29, a 45 μs memory access control timer, is also started. This timer insures that a non-responsive or disabled phase controller does not use more than its share of mailbox access time. If U29 times out, it will signal counter U28A to address the next phase controller. U30 will decode the new address and redirect the INT-X signal to the addressed phase controller. The offending phase controller will then be disconnected from the mailbox.

The external controller modules use one of the 4-bit binary counters in U28 (U28B) to address their mailbox locations in the non-volatile static RAM. U28B provides the three least-significant bits of the address. This counter is advanced by the ADDRCLK signal supplied by the PLD (U20-18). Whenever the external RD signal goes high, the address is advanced. Higher order address bits are supplied by the outputs of U28A and programmable logic array U20.

The external WRITE DATA EN strobe provides the address bit that determines whether access is granted to a read or write mailbox location. This signal also provides the direction control for bi-directional data bus transceiver U27. The COMM2-ADDR signal determines which communications controller mailbox is being addressed. If COMM2-ADDR is at logic one, the mailbox for Communications Controller #1 is addressed; the other mailbox is addressed when COMM2-ADDR is at logic zero.

At the end of the mailbox access routine, each phase controller will toggle its RD and WR strobes simultaneously to re-start the access control timer through U20-17. At the same time, the BLKADDR signal (U20-16) will be issued to advance the interrupt signal to the next phase controller. When all phase controllers have had access to their mailboxes during the current 0.5-ms program interval, U28A-5 will go high. The access control timer will be disabled and the SUPER_RD interrupt signal will be issued to the Supervisor Controller. The Supervisor Controller will respond by once again setting SUPR/W high, isolating the external controller modules from the mailbox memory.

The Supervisor Controller will then read the messages passed by the phase and communications controllers. After all mailbox registers have been read, the Supervisor Controller will reset the SUPR/W line and issue a low COMM_EN (U3-9) signal. This will enable the Communications Controller to access the mailbox memory. The Communications Controller will maintain access to the mailbox memory for the rest of the 0.5-ms program interval. The Supervisor Controller will use this time to process the data it has received from the other controllers, and to perform the other tasks assigned to it.

Program instructions are accessed whenever the target address is less than 8000H during external bus cycles. The READY/BUSWIDTH signal will be high, indicating a 16-bit bus operation with no wait states. With AD15 low, EPROM's U14 and U15 will be enabled; these devices hold the program instructions. Output address decoder U11 will be disabled through U10-1. This insures that the internal microcontroller data bus will be isolated from the memory-mapped I/O bi-directional data bus. During these intervals, the non-volatile static RAM is made available to the phase and communications controllers.

10.3.3 OUTPUT CONTROL LATCH

D-type flip-flop U16 serves as the output control latch, accessed through address CXXX. U16 provides the following signals to the phase controllers:

Signal	Pin No.
A SUP EN	U16-19
B SUP EN	U16-18
C SUP EN	U16-17
G SUP EN	U16-16

A logic high on any of these lines will disable trip on the corresponding phase controller. The phase controller has the ability to override this disable signal if it enters the back-up mode and forces its BACK-UP EN signal low. If the Supervisor Controller resets, it will drive these lines high and disable all phase controller trip signals.

The Supervisor Controller has the ability to access any memory location within static RAM U25, not just the mailbox locations. U16-12, U16-13 and U16-14 provide the three most-significant address bits to U25. These signals give the Supervisor Controller the ability to address the upper 1792 bytes of memory within U25. The external controllers have the ability to access only their mailbox registers.

10.3.4 SERIAL COMMUNICATIONS LINK WITH DISPLAY CONTROLLER

The Supervisor Controller communicates with the display controller through its serial port (U9-18 and U9-17). This serial link uses RS-485 transceiver U2, along with the SC READY (U16-15) and DC RDY (U1-4) control lines. Serial data is transmitted and received over the SERIAL I/O + and SERIAL I/O - signal lines. The PORT1.7 signal is used to control the transmit/receive status of U2.

A logic low signal on SC READY indicates that the RFL 93B SV is ready to receive serial data from the display controller in the RFL 93B DISPLAY. A logic high signals the display controller not to transmit. This signal provides a hardware enable/disable signal to the RS-485 transceiver located on the display controller board.

The DC RDY signal is supplied by the display controller. If this signal is a logic one, the display controller is not ready to communicate with the RFL 93B SV.

10.3.5 SERIAL COMMUNICATIONS LINK WITH THE SINGLE-POLE CHASSIS

The Supervisor Controller utilizes the SV_DAT (U9-25), SP_DETECT (U9-26) and SP_CHASSIS (P1-C29) inputs to interface with the Single-Pole chassis. Messages from the Single-Pole chassis are received on the SV_DAT input. SP_DETECT is used to detect the presence or absence of the Single-Pole chassis. A low signal on this line indicates that the Single-Pole chassis is connected to the RFL 9300. In order for single-pole trip to be active, SNGPOLE (U1-2) must be a logic low. This can only happen when jumper J5 on the 93B SV card is in the single-pole position (G), and the Single-Pole chassis is connected to the RFL 9300 via a ribbon cable which in turn connects SP_CHASSIS (P1-C29) to ground. If the 93B SV detects that any of these connections have changed since the interface with the Single-Pole chassis was initialized it will declare a SINGLE-POLE CHASSIS ALARM locally (#54) and transmit the alarm message to the Display Controller. If the Single-Pole chassis is connected to the RFL 9300 but jumper J5 is in the H position, the Single-Pole chassis is said to be in three-pole mode. In this mode none of the single-pole trip algorithms apply and the RFL 9300 operates as a normal two-terminal or three-terminal relay with six additional output trip contacts per phase.

Once initialized by the Display Controller, the single-pole logic begins transmitting a 16-bit status word to the Supervisor at 264ms intervals. The transmission is asynchronous with a start bit (active low), 16 data bits and one stop bit (active high) The message bits are synchronized to the system clock and are in the mark, or logic 1 condition when no messages are being transmitted. The Supervisor will not accept any status changes as valid until it receives two identical 16-bit messages in succession. If a status change is accepted as valid the Supervisor transmits byte 2 of the status message, as received from the single-pole logic, to the Display Controller. As long as there are no changes in single-pole logic status detected by the Supervisor, byte 2 of every 10th status message (2.64 second interval) is transmitted to the Display Controller. This is to insure that the Display Controller will not miss a change in single-pole logic status.

If the Supervisor goes 600ms without receiving a status message it will declare a SINGLE-POLE CHASSIS ALARM locally and transmit the alarm message to the Display Controller.

10.3.6 SINGLE-POLE TRIP ALGORITHMS

Open Breaker - When the RFL 9300 is configured for single-pole operation the open breaker condition is determined on a phase-by-phase basis. Any Phase Controller sending a ZTC signal to the RFL 93B SV will wait to declare its' breaker to be open until the RFL 93B SV returns the open breaker signal.

Reclose Block - The RFL 93B SV monitors all trip signals originating at both the local and remote terminals. If the RFL 9300 is configured for single-pole trip operation and a trip signal is detected, a 3-second timer is started. If trip signals, originating either at the local or remote terminals, are detected on the remaining two phases before the 3-second timer expires the reclose block output relay will be energized for 50ms.

Selective Pole Relaying - If Selective Pole Relaying is not enabled and multiphase trips are calculated locally, all three single-pole breakers will be tripped and a reclose block output signal will be issued. If Selective Pole Relaying is enabled and multiphase trips are calculated locally, only the breakers on the faulted phases will be tripped.

Backup Mode Trip - If the RFL 9300 is configured for single-pole trip operation and the relay is operating in backup mode, any trip signal that is calculated locally will result in all three single-pole breakers being tripped and a reclose block signal being issued. This is the case regardless of the status of Selective Pole Relaying which does not apply when backup mode is active. In three-terminal systems it is very possible that during a communications outage between two of the terminals, the third terminal may still be providing differential protection. Only the two terminals experiencing the communications problem may be in backup mode (if enabled). If the third terminal calculates a permissive trip it will transmit trip signals to the two terminals operating in backup mode. Since the trip was not calculated locally these terminals will trip only on the faulted phase(s).

3I0 Trip Algorithm - When the RFL 9300 relay is configured for single-pole operation the GROUND DELAY function takes on an additional role. If GROUND DELAY is not enabled, trips calculated by the 3I0 controller will have no effect. In certain applications, such as tapped loads, the ground bias may be set much more sensitive than the phase bias and only a 3I0 trip signal will be available to clear low-level internal faults. In this case GROUND DELAY must be enabled to insure that there will be adequate time to allow the individual Phase Controllers to trip their breakers. Then, when the 93B SV receives a trip signal from the 3I0 controller, if none of the Phase Controllers has issued a trip signal all three will be commanded to trip since the 3I0 controller can't pass its trip signal to the 93B SV unless the programmed GROUND DELAY has already expired.

When GROUND DELAY is enabled specifically for the purpose of allowing 3I0 single-pole trips it is recommended that a setting of 50ms be used. Keep in mind that the ground delay timer doesn't start until a 3I0 trip signal would have been issued in a three-pole application i.e. after the normal 3I0 trip delay. This means that with a 50ms setting the timer may not expire until as much as 80 to 90ms after the fault. Remember that trip signals are calculated at the conclusion of positive half-cycles of line current. Should a positive half-cycle terminate just prior to the 50ms time-out it will be an additional 16ms before the 3I0 trip will be passed to the 93B SV which must then pass the trip command to the phase controllers.

10.3.7 JUMPERS, ALARMS, WATCHDOG TIMER, AND POWER SUPPLY SUPERVISOR

Jumpers J1, J2 and J3 are used to configure the CCS system as follows:

J1 Position A for a 60-Hz system.
Position B for a 50-Hz system.

J2 Position C for a two-terminal configuration.
Position D for a three-terminal configuration.

J3 Position E for a 5A rms system.
Position F for a 1A rms system.

J4 Position J is used for 64K EPROM memory devices (U14 and U15). In this position pin 27 is connected to +5Vdc. For a 64K EPROM with the standard JEDEC footprint, pin 27 is the programming pin. Jumper position K is used for 256K EPROM memory devices. For a 256K EPROM with the standard JEDEC footprint pin 27 is address bit A14. In this circuit this address pin is grounded to limit access to the lower 128K of EPROM memory.

J5 Position G for 3-pole tripping.
Position H for single pole tripping. (See Section 24 for more information on single pole tripping)

The jumper status signals and the BACK-UP EN signal received from the other phase controllers are read through the 1A inputs of U5. All of the phase controllers share the BACK-UP EN signal line through an open collector inverter. This line will be pulled low if only one of the phase controllers enters back-up mode. In a normal situation, this can't happen because the phase controllers will either all enter back-up mode or none of them will. The 1Y and 2Y outputs share the PORT0.0 - PORT0.3 inputs of the microcontroller. The jumper signals and the BACK-UP EN signal are available on this 4-bit bus whenever the PORT1.0 signal is a logic 1. When this signal is a logic 0 the alarm signals from the phase controllers are available on the bus.

The PORT1.0 signal is the watchdog timer strobe pulse. Each time this signal goes high the 1500 μs watchdog timer (U7) is restarted and the jumper settings (J1, J2 and J3) and back-up status inputs are read. After this signal is brought low the phase controller alarm input signals are read. The alarm signals are active high.

If the first stage of the watchdog timer is not pulsed within about 1530 μs, it will time out and the B input of the second stage will be pulsed. This will cause a 30 μs reset pulse to be applied to the microcontroller through U6-5. The watchdog timer strobe pulse is also applied to U6-6. In the event that the microcontroller stops strobing the watchdog timer, a counter-driven watchdog timer inside power supply supervisor U6 will time out and deliver a 50 ms reset pulse to the microcontroller. This acts as a back-up to the main watchdog timer. In addition to providing a back-up watchdog timer function, the power supply supervisor provides a 50-ms reset pulse any time the power supply voltage drops below 4.5 Vdc. This guarantees a reset pulse to the microcontroller if a "brown-out" condition occurs.

10.3.8 OTHER MICROCONTROLLER I/O PORT SIGNALS

Some other microcontroller I/O port signals are described below. Their pin numbers are listed next to their names.

COMM1 ALARM (U4-1)
COMM2 ALARM (U4-4)

These are active-high alarm signals that show the alarm status of the Communications Controller Module (or modules). In a two-terminal system environment, COMM2 ALARM will always be active high (logic 1); however, the microcontroller is programmed to ignore it.

TRIP EN (U4-9)

This signal is received from the Relay I/O module (Section 20). This signal is a logic low when the display controller has disabled trip by de-energizing relay K1 on the Relay I/O module. This indicates that trip is disabled.

SUPER_RD (U4-12)

This is a locally-generated, positive-going interrupt signal received from U28A-5. It goes high when the phase controllers have completed their access to the non-volatile static RAM mailbox memory, telling the Supervisor Controller that it should grant the Communications Controller access to the memory.

60/50_HZ (U3-18)

This is a hardware signal directly from Jumper J1 through U3-18. It is supplied to the display controller and all phase controllers. It is a logic one when the 60-Hz position is selected, and logic zero for 50-Hz operation.

SUPR/W (U3-12)
COMM_EN (U3-9)
PCR/WEN (U3-7)

These are control signals associated with mailbox access. The COMM_EN and PCR/WEN signals will be disabled if the watchdog timer fails to operate. In this case, the HI-Z signal (U20-19) will disable the U3 2Y1-U3 2Y4 outputs and the U1 Y1-U1 Y4 outputs.

DTT EN (U3-5)

This is the active-low trip signal supplied to the oscillography board as a result of receiving a direct transfer trip message from the remote RFL9300. DTT EN is disabled if the watchdog timer expires.

SYSTEM CLOCK (U3-3)

This signal synchronizes the Supervisor Controller with all four phase controller, communications controller and single-pole logic programs. It guarantees that all phase controllers sample the CT waveforms at the same instant. This signal is disabled if the watchdog timer expires. If the RFL9300 is set for 60-Hz operation, SYSTEM CLOCK is a 2-kHz square wave; it is 1.667 kHz for 50-Hz units. If the relay is configured for 3-terminal operation, the system clock is phase locked at 33 x the line frequency in Hz.

SP_CHASSIS (P1-C29)
SV_DAT (U9-25)
SP_DETECT (U9-26)

These are signals associated with the single-pole trip function. See 10.3.5 for a description of these signals.

DC RDY (U1-4)

This is a serial communications handshake control signal. received from the display controller (Section 9). Its function was described in paragraph 10.3.4 of this manual.

89B (U1-6)

This signal is received from the Alarm I/O module (Section 21). It reflects the status of a disconnect switch at the local station. It is a logic low whenever the disconnect switch is opened, and a logic high when it is closed. When the supervisor detects an opened disconnect switch, the relay is placed in stub-bus active mode. See paragraph 3.13.

DTT TX (U1-8)

This signal is also received from the Alarm I/O module. It reflects the status of the Direct Transfer Trip signal at the local station. A logic zero indicates an active DTT signal. The Supervisor Controller sends this signal to the remote RFL 9300 through the Communications Controller.

RECLOSE (U1-7)

This is an active-low logic signal sent to the Alarm I/O module. It is generated by the Supervisor Controller whenever a three-phase trip is detected. It causes a reclose block signal to be generated on the Alarm I/O module. This is designed to prevent the main breaker at the local station from reclosing into a three-phase fault. This signal is disabled if the watchdog timer expires.

LOCAL ALARM RELAY (U1-3)
COMM ALARM RELAY (U1-5)

These are alarm signals generated by the Supervisor Controller. They control the electromechanical System and Communications Alarm relays on the Alarm I/O module. These normally-open relays are de-energized when an alarm condition is detected, so a logic one output signifies the alarm condition.

These signals are disabled if the watchdog timer expires. This will de-energize both relays and cause alarms to be issued.

SPARE (U9-27)

This input signal line has no function at this time.

Table 10-1. Replaceable parts, supervisor controller module for RFL 9300
RFL 93B SV (Assembly No. 106300-1)

Circuit Symbol (Figs. 10-3 & 10-4)	Description	Part Number
	CAPACITORS	
C1-7,9-20,23-30,35,39,40	Capacitor,ceramic dip,0.1μF,10%,50V	0120 38
C31,32,43	Capacitor,ceramic dip,0.01μF,5%,100V,AVX SR301A103JAA or equiv.	1007 1645
C33,34	Capacitor,ceramic,22pF,5%,200V	0125 22205
C36	Capacitor,tantalum,33μF,10%,10V	1007 1142
C37,38	Capacitor,ceramic,0.001μF,5%,100V	0125 11025
C41,42	Capacitor,electrolytic,47μF,20%	1007 1578
	RESISTORS	
R1-4,14	Resistor,metal film axial,1K,1%,1/4W,Type RN1/4	0410 1288
R5,6	Resistor,metal film axial,221Ω,1%,1/4W,Type RN1/4	0410 1225
R7,8,11-13,16,17,18	Resistor,metal film axial,10K,1%,1/4W,Type RN1/4	0410 1384
R9	Resistor,metal film axial,5.62K,1%,1/4W,Type RN1/4	0410 1360
R10	Resistor,metal film axial,154K,1%,1/4W,Type RN1/4	0410 1498
R15	Resistor,metal film axial,46.4K,1%,1/4W,Type RN1/4	0410 1448
R19-21	Resistor,metal film axial,1.24K,1%,1/4W,Type RN1/4	0410 1297
R22	Resistor,metal film axial,6.19K,1%,1/4W,Type RN1/4	0410 1364
R23	Resistor,metal film axial,2.49K,1%,1/4W,Type RN1/4	0410 1326
R24	Resistor,metal film axial,15K,1%,1/4W,Type RN1/4	0410 1401
R25	Resistor,metal film axial,1.5K,1%,1/4W,Type RN1/4	0410 1305
R26	Resistor,metal film axial,1.06K,1%,1/4W, Type RN1/4	0410 1375
RZ1,8	Resistor network,seven 10K,2% resistors,1.1W total,8-pin SIP, CTS of Berne 750-81-R10K or equiv.	47878
RZ2-7,9	Resistor network,nine 10K,2% resistors,1.25W total,10-pin SIP, Bourns 4310R-101-103 or equiv	32622

<< table continues on next page>>

Table 10-1 continued. Replaceable parts, supervisor controller module for RFL 9300 Charge Comparison System

Circuit Symbol (Figs. 10-3 & 10-4)	Description	Part Number
	SEMICONDUCTORS	
DS1,2	Light-emitting diode,red,right-angle PC mount, extended length, Industrial Devices 5300H1 or equiv.	99294
U1,3	MOS octal buffer/driver,20-pin DIP, Motorola MC74ACT244N or equiv.	0615 379
U2	RS-485 transceiver,8-pin DIP, Linear Technology LTC485IN8 or equiv.	0680 14
U4	MOS quad 2-input AND gate,14-pin DIP, National Semiconductor MM74HC08N or equiv.	0615 161
U5	MOS octal buffer/line driver,20-pin DIP,RCA CD74HC241E or equiv.	0615 319
U6	Microprocessor supervisor,8-pin DIP, Maxim MAX690EPA or equiv.	0635 27
U7,29	MOS dual retriggerable monostable multivibrator,16-pin DIP, National Semiconductor MM74HC123N or equiv.	0615 282
U9	Microcontroller, N80C196KD	0615 459
U10	MOS quad 2-input NOR gate,14-pin DIP, Motorola MC74ACT02N or equiv.	0615 376
U11	MOS dual 2- to 4-line decoder,16-pin DIP, Motorola MC74ACT139N or equiv.	0615 378
U12,13,18,19	MOS octal latch,tri-state,20-pin DIP, Motorola MC74ACT573N or equiv.	0615 382
U14,15	EPROM,32K x 8,70-ns access time, programmed at factory	Contact factory
U16	MOS octal D-type flip-flop,20-pin DIP, Motorola MC74ACT574N or equiv.	0615 383
U17	MOS octal buffer/driver,20-pin DIP, Motorola MC74ACT541N or equiv.	0615 381
U20	Programmable logic array (PAL),programmed at factory	Contact factory
U23	MOS tri-state buffer,16-pin DIP, National Semiconductor MM74HC367N or equiv.	0615 290
U24	MOS quad 2-input multiplexer,16-pin DIP, Motorola MC74ACT257N or equiv.	0615 380
U25	MOS static RAM, nonvolatile w/internal lithium battery,24-pin DIP, SGS-Thomson MKI48Z12B-20 or equiv.	0615 385
U26	MOS octal tri-state D-type latch,20-pin DIP, Texas Instruments SN74HC573N or equiv.	0615 308
U27	MOS tri-state octal transceiver 20-pin DIP, National Semiconductor MM74HC245N or equiv.	0615 177
U28	MOS dual 4-bit binary counter,14-pin DIP, National Semiconductor MM74HC393N or equiv.	0615 192
U30	MOS 3 to 8-line decoder/demultiplexer w/address latches,16-pin DIP, Texas Instruments SN74HC137N or equiv.	0615 322
U31	IC, linear quad fault monitor	0620 368
	MISCELLANEOUS COMPONENTS	
J1-5	Shorting bar, single,Molex 90059-0009 or equiv.	98306
Y1	Crystal,quartz,16.000 MHz	30297

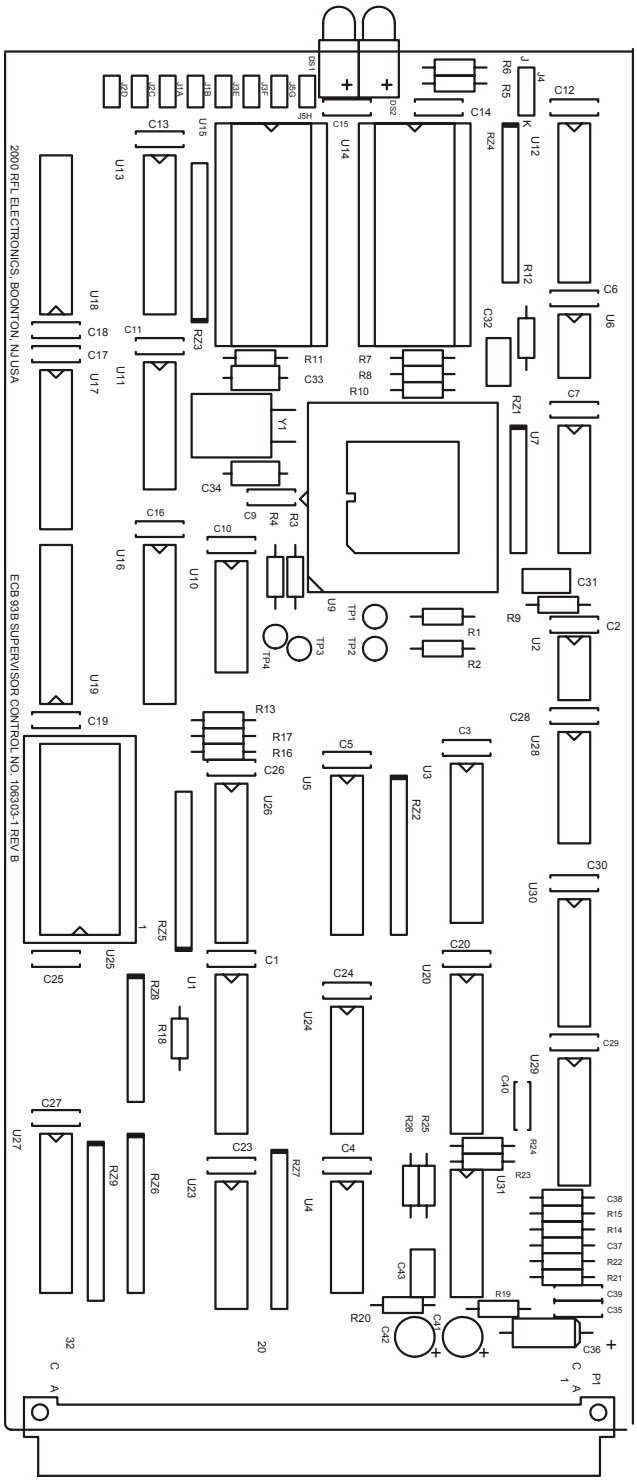


Figure 10-3. Component locator drawing, supervisor controller modules for RFL 9300 (Assembly No. 106300-1; Drawing No. D-106300-1-A)

Figure 10-4. Supervisor Controller module for RFL 9300 Charge Comparison System(Assembly No. 106300; Schematic No. D-106304-1-B) Sheets 1 of 2 and 2 of 2

Please see Figure 10-4, Sheets 1 of 2 and 2 of 2, in Section 32: Schematics

SECTION 11: AUXILIARY CURRENT TRANSFORMER I/O MODULE

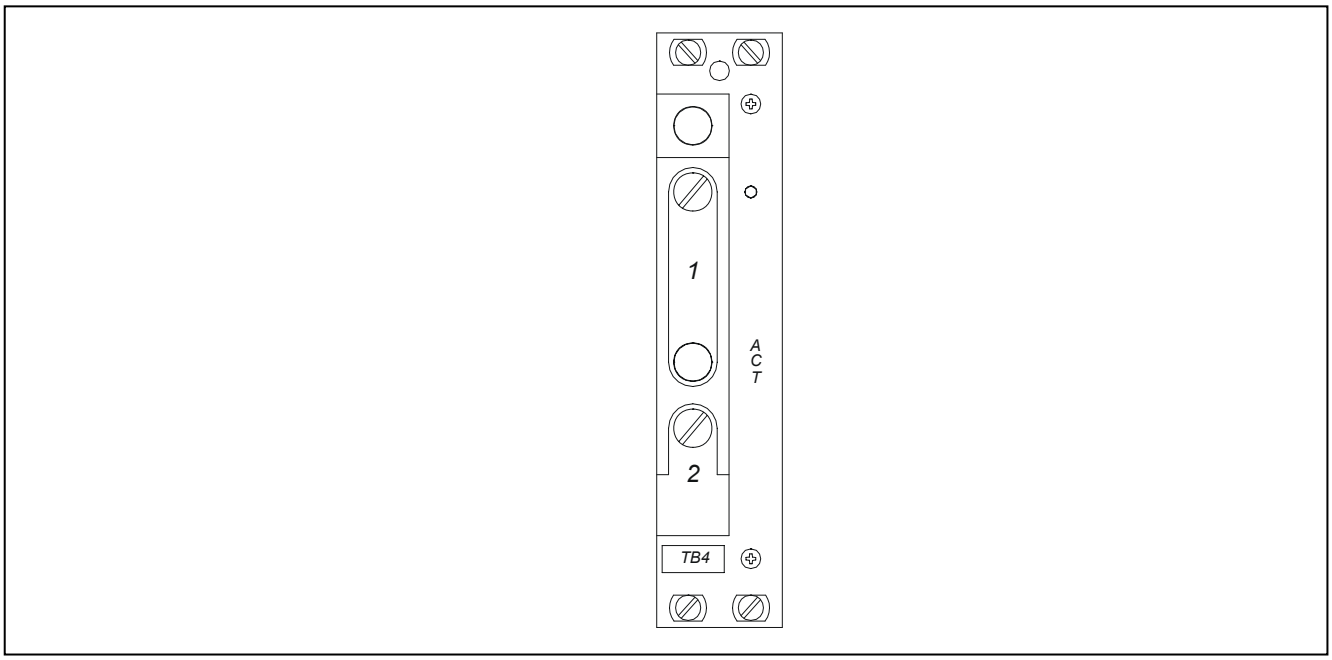


Figure 11-1. RFL 93B ACT I/O Auxiliary Current Transformer I/O Module

11.1 DESCRIPTION

Each RFL 9300 contains four RFL 93B ACT I/O Auxiliary Current Transformer I/O modules (Fig. 11-1) These I/O modules monitor the currents being passed to them by the current transformers (CT's) on the protected line, and pass these currents on to the phase controller modules (Section 12).

11.2 CONTROLS AND INDICATORS

Figure 11-2 shows the location of all controls and indicators on the RFL 93B ACT I/O Auxiliary Current Transformer I/O Module. These controls and indicators are described below. Only the rear-panel terminal block (TBX) is accessible with the RFL 93B ACT I/O installed in the RFL 9300 chassis; all others are only accessible when the RFL 93B ACT I/O is either removed from the chassis, or placed on a card extender.

TERMINAL BLOCKS

TBX Connecting point for input leads from the current transformer on the protected line.

TEST TURRETS

TP1 Monitoring point for the A1 AUX IN line.

TP2 Signal ground.

TP3 5-volt return (ground).

TP4 Monitoring point for the DC RESTORE line.

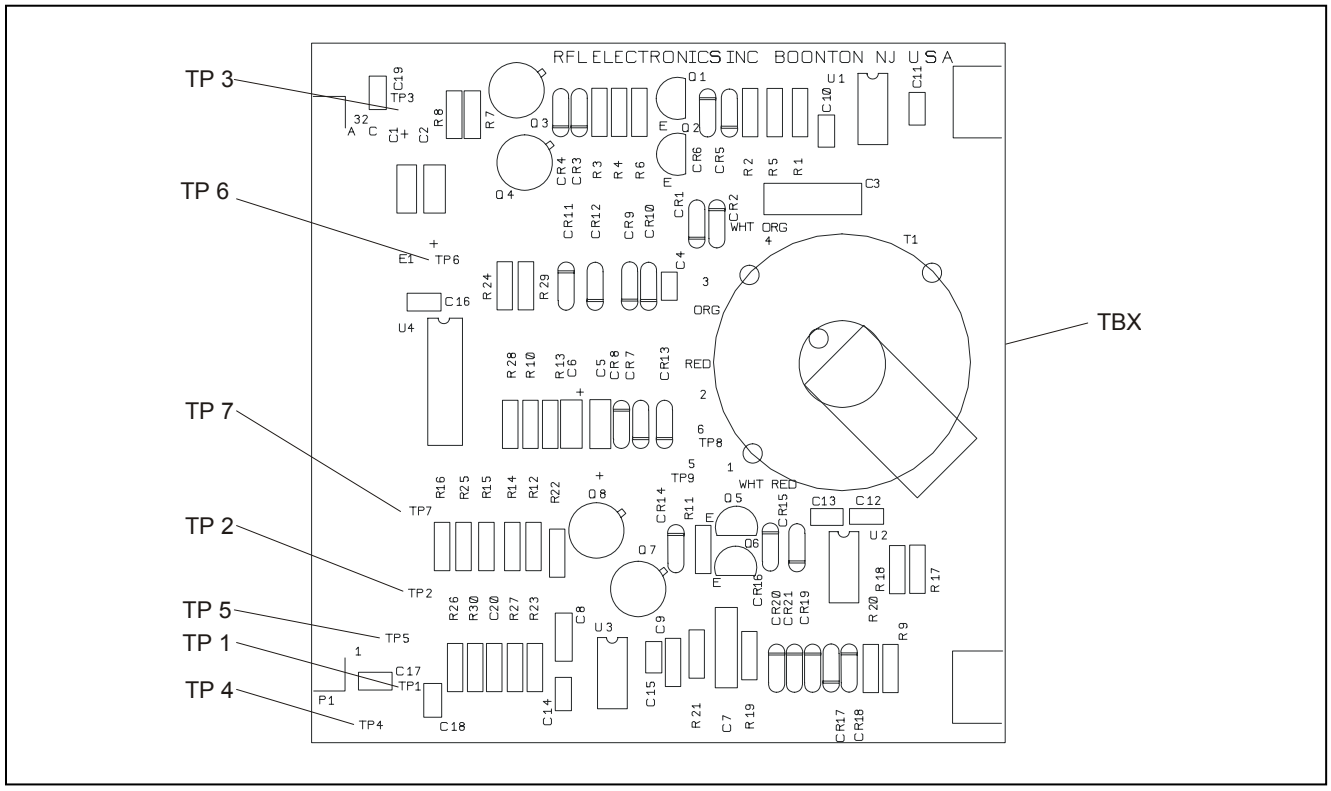


Figure 11-2. Controls and indicators, RFL 93B ACT I/O Auxiliary Current Transformer I/O Module

TP5 Monitoring point for PWR UP RESET line.

TP6 Monitoring point for high-current buffer output.

TP7 Monitoring point for full-wave rectifier output.

11.3 THEORY OF OPERATION

The RFL 93B ACT I/O Auxiliary Current Transformer I/O Module is an active current transformer that converts power system currents to voltages. These voltages are passed on to the phase controller modules for further processing. Normal steady-state input currents are 5 A_{rms} @ 60 Hz, and currents during power system disturbances could be as high as 250 A_{rms}. The RFL 93B ACT I/O uses the following formula for output scaling:

$$V_{out} = I_{in} / 6.35$$

The RFL 93B ACT I/O uses a flux cancellation technique that creates a near-perfect current transformer.

The RFL 93B ACT I/O contains a current transformer, a sense amplifier with high-current buffer, an analog switch, a current-to-voltage converter with high-current buffer, and a buffered 200-Hz low-pass filter. A block diagram of the RFL 93B ACT I/O appears in Figure 11-3.

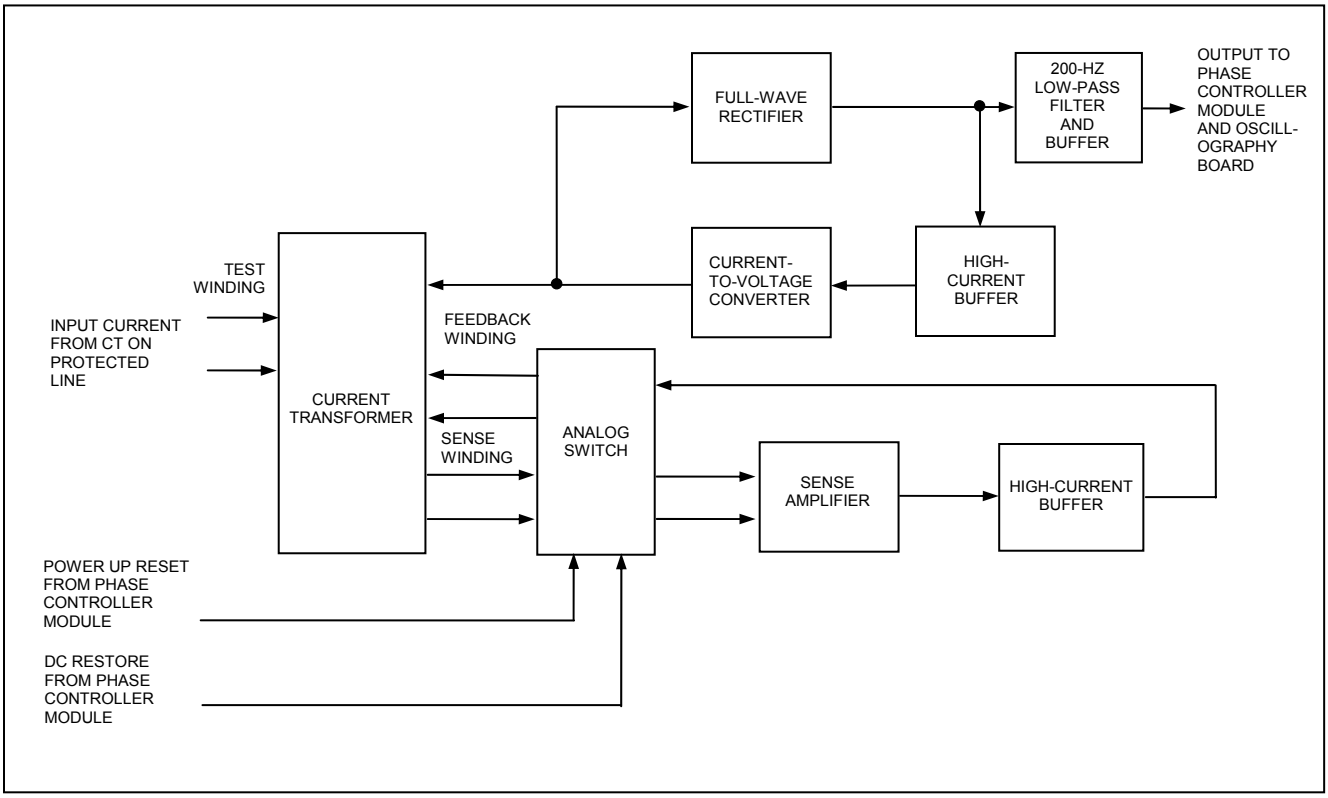


Figure 11-3. Block diagram, RFL 93B ACT I/O Auxiliary Current Transformer I/O Module

Current transformer T1 has one primary winding which is a single-turn winding for normal operating currents. When current is applied to the T1 primary, sense amplifier U1 senses the signal developed on the 1000-turn secondary winding. U1 inverts this signal and converts it to a current used to drive T1's 4000-turn feedback winding. This current is fed to the feedback winding through three sections of analog switch U4. The current in the feedback winding reduces the signal on the sense winding to near zero, canceling the flux in the transformer core. The current needed in the feedback winding is equal to the primary current multiplied by the primary/feedback winding turns ratio.

The current in the feedback winding is fed to operational amplifier U2, which serves as a current-to-voltage converter. U2's output is fed to a high-current buffer formed from transistors Q5 through Q8 and their associated components. The scaling factors for the current-to-voltage converter are determined by resistors R17 and R18. R18 is a factory-selected part; its value is selected to compensates for low-pass filter losses and errors in the 4000-turn transformer winding. The output of the current-to-voltage converter is limited to 10.3 volts by the full-wave rectifier formed from diodes CR17 through CR20 and Zener diode CR21. The limiting function only limits the output voltage; the circuit will cancel flux and prevent saturation of T1's core for input currents as large as 250 A_{rms}.

The final output stage of the RFL 93B ACT I/O is a three-pole, 200-Hz, low-pass filter formed from resistors R21 through R23 and capacitors C7 through C9. The output of this filter is buffered by operational amplifier U3. This filter provides anti-aliasing for the A/D converter on the phase controller module (Section 12.)

The Phase Controller also has some additional control over the RFL 93B ACT I/O, in terms of power-up and power system disturbances with a dc component. Two logic-level signals from the RFL 93B PC control analog switch U4: POWER UP RESET (edge connector terminal P1-C2) and DC RESTORE (P1-A2). During system initialization, POWER UP RESET is held high, keeping the output of the sense amplifier disconnected from T1's feedback winding. This is done for 650 ms, and provides a smooth power-up sequence for the RFL 93B ACT I/O.

The DC RESTORE signal is normally held high for steady-state power system currents. During disturbances that contain a dc component, the phase controller module drops DC RESTORE low. This closes section D of analog switch U4 and shorts out capacitor C3. Since the circuit is basically operating open-loop, there must be some form of dc stability around the overall loop. The output of the current-to-voltage converter is fed back through a voltage divider formed from resistors R28 and R29. Resistor R24 and capacitor C3 form a low pass filter. This filter strips out the ac component, and provides dc feedback to sense amplifier U1.

During disturbances with a dc component, the phase controller module modulates the DC RESTORE line. This allows reproduction of the transient without charging C3 to a false dc level that could saturate sense amplifier U1.

Table 11-1. Replaceable parts, RFL 93B ACT-5 5-Ampere Auxiliary Current Transformer to I/O Module (Assembly No. 106345-5)

Circuit Symbol (Figs. 11-4 & 11-5)	Description	Part Number
	CAPACITORS	
C1,2	Capacitor,tantalum,4.7μF,20%,20V,Kemet T322B475M020AS or equiv.	1007 711
C3,7	Capacitor,metallized polycarbonate,0.22μF,2%,50V,Wesco 32MPC or equiv.	1007 1329
C4	Capacitor,X7R ceramic,0.001μF,10%,100V,AVX SA101C102KAA or equiv.	0130 11021
C5,6	Capacitor,tantalum,1μF,10%,35V,Kemet T110A105K035AS or equiv.	1007 1156
C8	Capacitor,ceramic,0.01μF,5%,100V,AVX SR301A103JAA or equiv.	1007 1645
C9	Capacitor,ceramic,0.001μF,5%,100V,AVX SA201A102JAA or equiv.	0125 11025
C10-19	Capacitor,ceramic,0.1μF,GMV,50V,Centralab CY20C104P or equiv.	1007 1366
C20	Capacitor,ceramic,10pF,10%,100V,AVX SA101A100KAA or equiv.	0125 11001
	RESISTORS	
R1,9	Resistor,metal film,1K,1%,1/4W, Type RN1/4	0410 1288
R2,4,10,12	Resistor,metal film,4.75K,1%,1/4W, Type RN1/4	0410 1353
R3,11	Resistor,metal film,39.2K,1%,1/4W, Type RN1/4	0410 1441
R5,6,13,14	Resistor,metal film,221Ω,1%,1/4W, Type RN1/4	0410 1225
R7,8,15,16	Resistor,metal film,10Ω,1%,1/8W,Type RN55D	1510 1092
R17	Resistor,metal film,649K,0.1%,0.2W,200V maximum working voltage, Dale CMF-55-6490BT9 or equiv.	1510 2274
R18	Resistor,metal film,factory-selected value	Contact factory
R19,20	Resistor,metal film,1.62K,1%,1/4W, Type RN1/4	0410 1308
R21	Resistor,metal film,2.32K,1%,1/4W, Type RN1/4	0410 1323
R22	Resistor,metal film,10K,1%,1/4W, Type RN1/4	0410 1384
R23	Resistor,metal film,100K,1%,1/4W, Type RN1/4	0410 1480
R24	Resistor,metal film,301K,1%,1/4W, Type RN1/4	0410 1526
R25,26	Resistor,metal film,4.99K,1%,1/4W, Type RN1/4	0410 1355
R27	Resistor,metal film,113K,1%,1/4W, Type RN1/4	0410 1485

Table 11-1 continued. Replaceable parts, RFL 93B ACT-5 5-Ampere Auxiliary Current Transformer I/O Module

Circuit Symbol (Figs. 11-4 & 11-5)	Description	Part Number
	RESISTORS - continued	
R28	Resistor,metal film,20K,1%,1/4W, Type RN1/4	0410 1413
R29	Resistor,metal film,2K,1%,1/4W, Type RN1/4	0410 1317
R30	Resistor,metal film,100Ω,1%,1/4W, Type RN1/4	0410 1192
	SEMICONDUCTORS	
CR1-20	Diode,silicon,1N914B or 1N4448	26482
CR21	Diode,Zener,9.1V,5%,400mW,1N960B	41014
Q1,5	Transistor,PNP,plastic package,2N2907A	37439
Q2,6	Transistor,NPN,plastic package,2N2222A	37445
Q3,7	Transistor,NPN,TO-5 case,2N2219A	39569
Q4,8	Transistor,PNP,TO-5 case,2N2905A	39567
U1,3	Linear operational amplifier,low offset voltage,8-pin ceramic DIP, Precision Monolithics OP77EZ or equiv.	0620 340
U2	Linear operational amplifier,JFET input,8-pin DIP,Texas Instruments TL081IP or equiv.	0620 228
U4	MOS quad analog switch,SPST,ON resistance 100W maximum @ +85^{O}C,16-pin DIP, Siliconix DG441DJ or equiv.	0605 17
	MISCELLANEOUS COMPONENTS	
T1	Transformer, current drive	100541

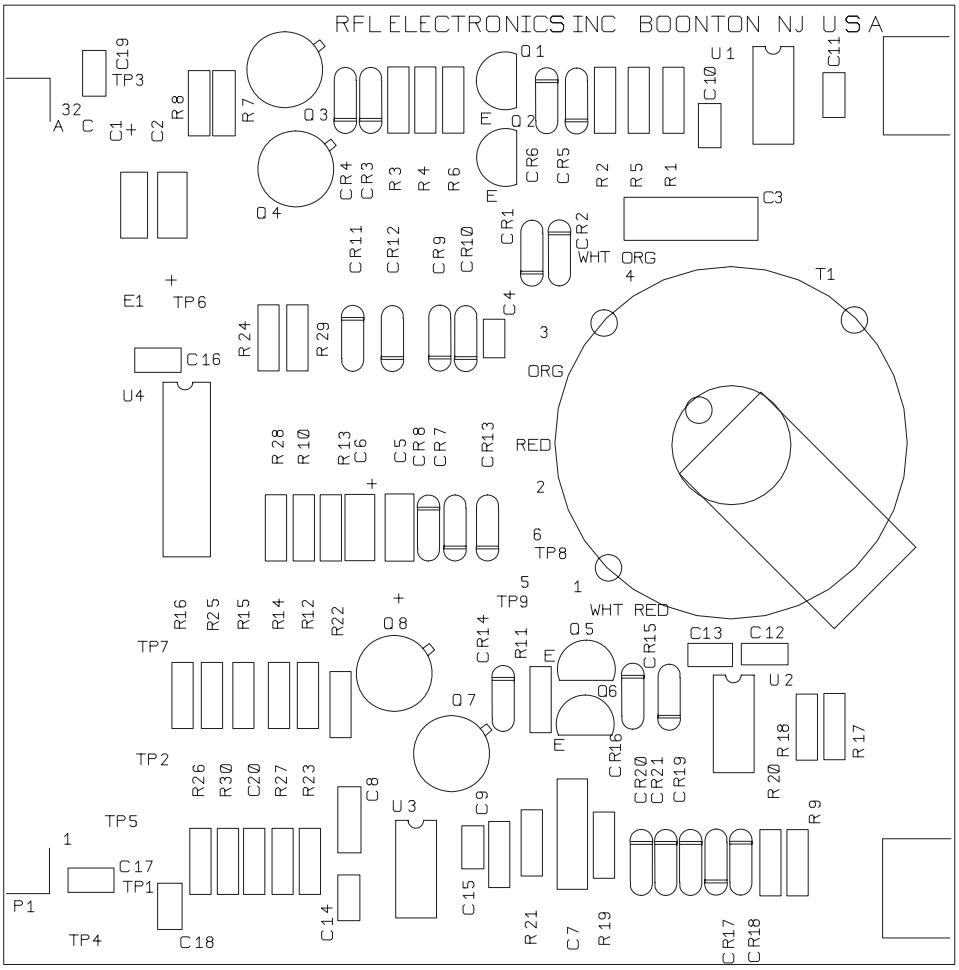


Figure 11-4. Component locator drawing, RFL 93B ACT-5 5-Ampere Auxiliary Current Transformer I/O Module (Assembly No. 106345-5; Drawing No. C-106345, Rev. A)

Figure 11-5. RFL 93B ACT-5 5-Ampere Auxiliary Current Transformer I/O Module (Assembly No. 106345; Schematic No. D-105814, Rev. C)

Please see Figure 11- 5 in Section 32: Schematics

This page intentionally left blank

SECTION 12: PHASE CONTROLLER MODULE

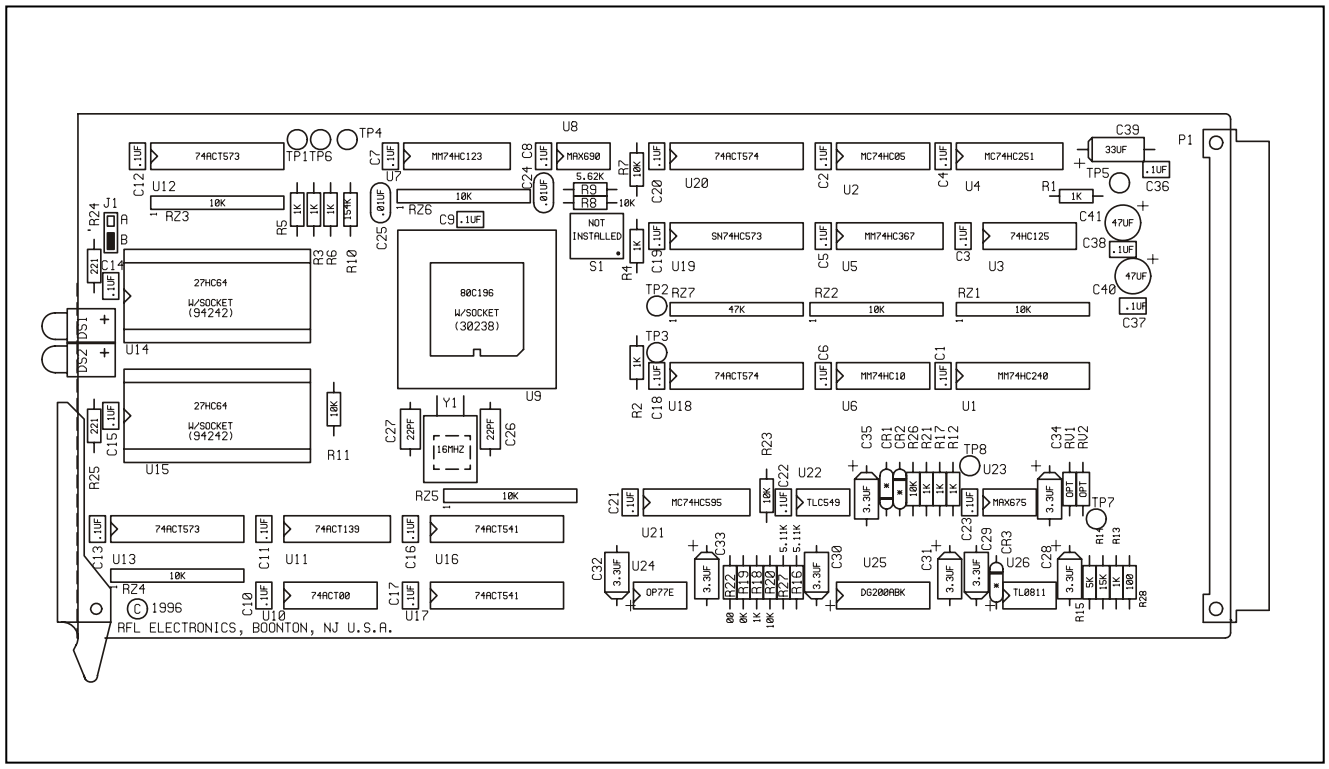


Figure 12-1. RFL 9300 phase controller module

12.1 DESCRIPTION

The RFL 93B PC Phase Controller Module is shown in Figure 12-1. Each RFL 9300 contains four RFL 93B PC Phase Controller modules: one for each phase, and one for ground. The phase controller modules monitor the currents passed to them by the ACT I/O modules (Section 11), and execute the RFL 9300's protection algorithms. Except for DTT (which is controlled by the RFL 93B SV module), the individual phase controller modules make all trip/no trip decisions for the RFL 9300.

12.2 CONTROLS AND INDICATORS

Figure 12-2 shows the location of all controls and indicators on the RFL 93B PC Phase Controller Module. These controls and indicators are described below. Those described as front-panel controls are accessible with the RFL 93B PC installed in the RFL 9300 chassis; all others are accessible when the RFL 93B PC is removed from the chassis, or is placed on a card extender.

LED INDICATORS

DS1 ALARM - Front-panel indicator; lights when a problem is detected in a specific phase controller module.

DS2 FD - Front-panel indicator; lights when the fault detector for that phase produces an output.

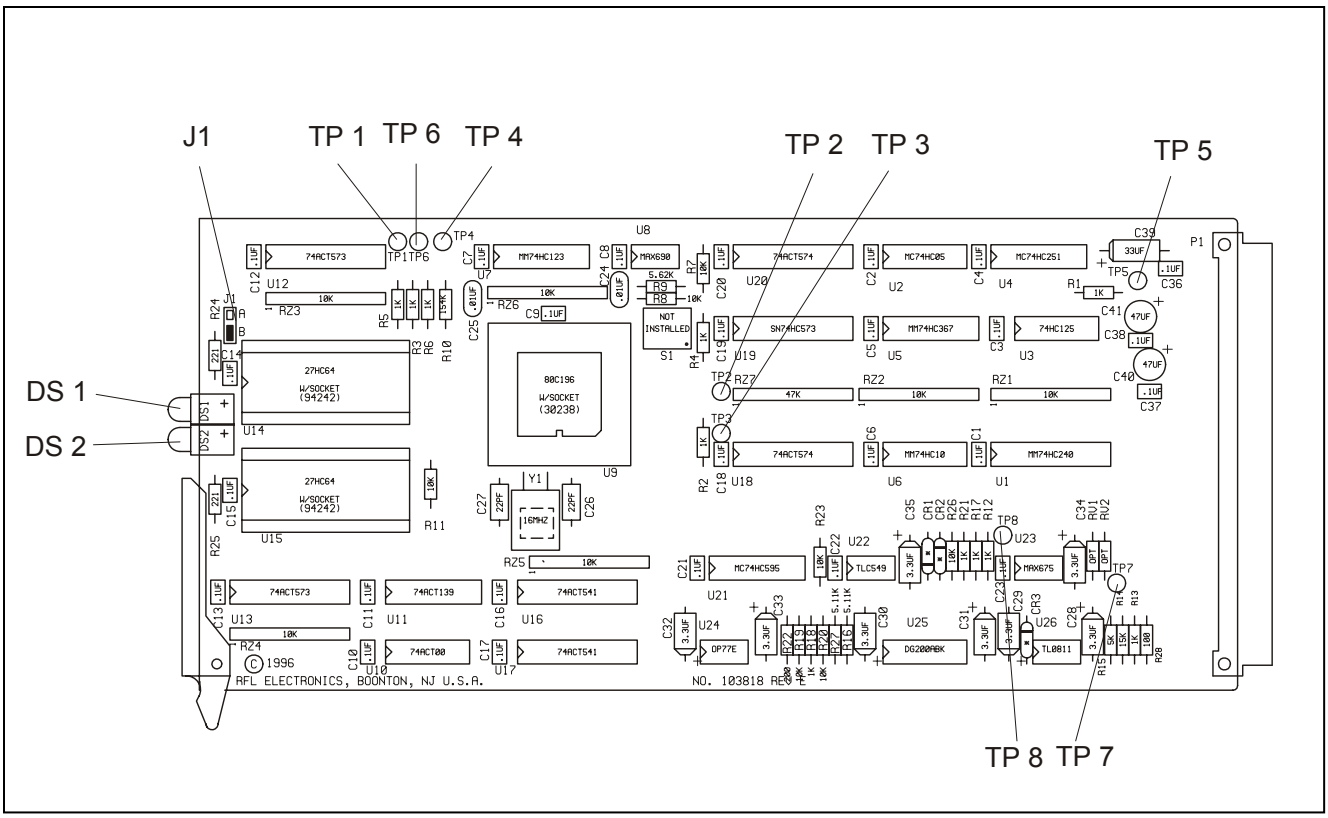


Figure 12-2. Controls and indicators, RFL 9300 phase controller modules

JUMPERS

J1 Set at the factory according to the type of device installed for U14 and U15. Position A is used for 27C256 devices, and Position B is used for 27C64 or 27C128 devices. **Do not change the setting of this jumper, unless U14 and U15 are being replaced with another device type.**

TEST TURRETS

TP1 Positive watchdog timer pulse signal. This narrow-pulse signal should appear at 500-ms intervals for 60-Hz systems, and 600-ms intervals for 50-Hz systems.

TP2 Monitoring point is a 1μs positive clock pulse starting 497μs after the rising edge of the system clock signal applied to U9-24 (HSI.0). For 50-Hz systems, this pulse will start 597μs after the leading edge of the system clock signal.

TP3 Monitoring point for the system clock signal supplied by the RFL 93B SV Supervisor Controller. The clock frequency is 2 kHz for 60-Hz systems, and 1.667 kHz for 50-Hz systems. When the relay is configured for 3-terminal operation, the system clock is phase locked to the line current at a frequency equal to 33 times the line frequency in Hz.

TP4 Monitoring point for the READY/BUSWIDTH signal. This signal should go low whenever a memory-mapped I/O access is executed. All memory-mapped I/O resides at addresses of 8000H or higher, or when U12-19 is high. Whenever TP4 is low, one wait state is added to the external bus cycles, and the microcontroller's bus width dynamically switches from 16 bits to 8 bits.

TP5 Monitoring point for a copy of the low-going INT-X signal on edge connector terminal P1-A6; this signals a communications interrupt request. This signal will go low about 45 ms after the leading edge of the system clock signal.

The phase controller has access to the non-volatile static RAM mailbox memory chip on the RFL 93B SV Supervisor Controller Module whenever this signal is low. It is derived from a one shot timer on the Supervisor Controller, and should never last for more than about 50 ms. The strobe signals on edge connector terminals P1-A24, P1-A25, P1-C24, and P1-C25 are active only when this signal is low. They are in tri-state mode at all other times.

TP6 8-MHz clock signal. The system clock signal is divided by two within the microcontroller.

TP7 Monitoring point for AUX IN signal.

TP8 Monitoring point for 5-volt reference voltage.

12.3 THEORY OF OPERATION

The RFL 9300's protection algorithms are executed by U9, a 16-bit microcontroller. Timers inside U9 are programmed to monitor the system clock signal supplied by the Supervisor Controller through edge connector terminal P1-C11. When the relay is configured for 2-terminal operation the period of the clock signal must remain between 498μs and 502μs (598μs and 602μs for 50-Hz systems). If the period goes beyond these limits, U9 will reset. When the relay is configured for 3-terminal operation, the system clock is phase locked to the line current at a frequency equal to 33 times the line frequency in Hz. Write or read operations from address locations of 8000H or higher will result in a low signal on pins U9-43 and U9-64 through NAND gate U10. This causes U9 to switch to its 8-bit external bus mode and to insert a 125 ns wait state into the bus cycle.

The microcontrollers' internal clock signal is provided by an on-board gate oscillator. Crystal Y1 and capacitors C26 and C27 are the frequency-determining components for this oscillator.

An external microcontroller bus cycle utilizes the WR, RD, and ALE signals. Instructions and data are read from EPROM's U14 and U15, while octal flip-flops U18 and U20, octal latch U19, and shift register U21 serve as memory-mapped I/O ports.

At the start of the external bus cycle, the three control signals are high. The ALE signal provides a high latch control signal to latch the address bits into U12 and U13, which serve as a memory address buffer. The external target address appearing on lines AD0 through AD15 also appears on the buffer output pins. When the ALE signal goes low the address remains latched on the buffer outputs.

The RD signal (U9-61) serves as the output enable signal for EPROM's U14 and U15, the read address decoder section of U11, and buffer/driver U17. If the memory address is less than 8000H, AD15 is low. This serves as the EPROM chip select and enables 16-bit program instruction words to be read by U9. If U9 is executing a byte operation, the unwanted 8-bit portion of the 16-bit word is discarded. Also, when AD15 is low, buffers U16 and U17 will be tri-stated, and the external memory-mapped I/O ports (U18 through U21) will be isolated from the microcontroller bus.

Memory-mapped I/O bus cycles differ from instruction fetch I/O bus cycles in several respects:

1. The width of the data bus is dynamically altered from 16 bits to 8 bits.

2. Both read and write bus cycles take place.

3. Memory-mapped I/O bus cycles are mapped at memory addresses 8000H and above (line AD15 high).

4. A 125-ns wait state is inserted into the bus cycle.

When the address is 8000H or higher, the EPROMS are disabled. At the same time, U10-8 (which provides the ready/buswidth signal) is low. This configures the data bus as an 8-bit bus, and the bus cycle is extended by one wait state. This signal also enables the Y0 and Y1 outputs on both halves of memory-mapped I/O decoder U11 in conjunction with the microcontroller RD and WR signals, depending on the desired type of bus cycle. U11-1 through U11-7 form the read decoder section, and U11-9 through U11-16 form the write decoder section.

The phase controller can pass messages to and from the mailbox on the Supervisor Controller (Section 10) when the INT-X signal (edge connector terminal P1-A6) goes low. The low-going leading edge of this signal is inverted by U2 and generates the microcontroller communications interrupt signal. The external strobes required to access the mailbox are enabled through buffer/line driver U3 when this signal is low. The strobe signals are RD (edge connector terminal P1-A24), WR (P1-A25), CS (P1-C24), and WRITE DATA EN (P1-C25).

Messages being sent to the Supervisor Controller are latched into octal flip-flop U18. Messages are read from the Supervisor Controller through octal latch U19. Address 8000H, decoded by U11, is used for both of these buffers. The Supervisor Controller has an on-board timer that monitors the INT-X signal. The Phase Controller is allowed 50μs to complete the mailbox access before the Supervisor Controller will pull INT-X high, disabling all strobe lines.

Address 8001H is also decoded by U11. It is used to access buffers U20 and U21. Phase current waveform data is supplied by the ACT I/O module through edge connector terminal P1-A32. Operational amplifier U26 and analog switch U25 are used in a range-switching scheme that makes 8-bit serial A/D converter U22 appear to provide an equivalent 10-bit conversion (9 bits plus sign). The 2.5-V_{peak} full-scale signal received from the ACT I/O module is equivalent to 15.875 A_{peak}. Operational amplifier U24 amplifies this by two to bring the full-scale signal level to 5 volts. Voltage reference U23 supplies a precise 5-volt dc reference to A/D converter U22. The input to the A/D converter (U22-2) will be at 2.5 volts when the ACT I/O output is zero. As the ACT I/O signal covers its full range (+5 volts to –5 volts), the A/D converter's input signal will range from +5 volts to zero. U22 converts this unipolar input to a bipolar output using an offset binary code.

Microcontroller U9 uses the A/D CHIP SEL and A/D CLOCK signals to serially convert the analog signal to a digital value and latch the result into buffer chip U21. The A/D CLOCK is an 8-cycle 1-MHz clock signal, generated by using the microcontrollers' serial port in the synchronous mode. The eighth clock pulse starts a new conversion, and it is this value that will be read during the following 0.5-ms interval. Because of this, the value read by the microcontroller is always 0.5 ms old. If the peak CT current exceeds 14 amperes, analog switch U25 will be commanded to switch channels and the input signal will be supplied through U26. This effectively reduces the gain by a factor of 4, allowing the maximum level of the ACT I/O output to increase to 63.5 A_{peak}. When operating in this mode the resolution of the A/D converter's least-significant bit is reduced by a factor of 4 from 1/8 ampere to ½ ampere. Diodes CR1 and CR2 and resistor R21 protect U22 against negative input signal levels.

The front-panel ALARM and FD indicators are accessed through output buffer U21. Additional signals supplied by this buffer are L1.5 EN and L3A EN OUT. These two signals are part of the loss-of-load hardware bus that runs between all phase controller modules. L1.5 EN is low when phase CT current is 1.5 A_{rms} or more. L3A EN OUT is high when phase CT current is 3 A_{rms} or more. This signal is inverted by an open-collector inverter in U2 (U2-8 out), and pulls down the 3 ampere loss-of-load signal line (R3A EN IN) when the CT current is 3 A_{rms} or more.

Additional loss-of-load function signals are received from the other phase controller modules through octal buffer U1. They are R1.5 EN1, R1.5 EN2 and R3A EN IN. These are the 1.5 ampere and 3 ampere remote signals required for the loss-of-load function. If any phase current exceeds 3 A_{rms}, the R3A EN IN line will be pulled low. This backup function has the capability of operating even if the Supervisor Controller can't communicate with the phase controller modules. U20 also supplies the ACT gain range switch signals mentioned above.

Dual retriggerable monostable multivibrator U7 and its associated components form a 1500μs watchdog timer. The timer is pulsed at regular 500μs intervals in 60-Hz systems, or 600μs intervals in 50-Hz systems. These pulses are provided by the microcontroller's Port1.0 signal once during each 0.5-ms program interval. Should the microcontroller not pulse the watchdog timer before it times out, it will deliver a 30μs reset pulse to U9 through microprocessor supervisor U8 and NAND gate U6. In the unlikely event that the watchdog timer fails to reset U9, a backup 1.6-second watchdog timer inside U8 will reset U9.

The primary function of U8 is to monitor the +5-volt power supply, and insure that microcontroller U9 is reset during turn-on or "brown-out" conditions. A 50-ms reset pulse is guaranteed if the supply voltage falls below 4.5 volts. Simple RC-type reset circuits can't guarantee a reset under "brown-out" conditions.

If the reset signal is active, the communications interrupt signal and all mailbox strobe lines are isolated from the outside world. The same is true of the A/D CLOCK, PWR UP RESET, DC RESTORE, and the phase controller trip signal. When the reset signal is low, it tri-states several input devices, including multiplexer U4, buffer/line driver U3, and parts of inverting buffer U1 and buffer U5.

The DC RESTORE signal is applied to the ACT circuit whenever a peak change fault is detected. The signal operates an analog switch that shorts the filter capacitor in the ACT's feedback circuit. This prevents fault current waveforms with large amounts of dc offset from saturating the ACT input transformer.

The PWR UP RESET signal controls an analog switch that opens the secondary of the ACT's input current transformer during power-down conditions. The transformer is switched back into the circuit during phase controller initialization, and the PWR UP RESET signal remains low for the duration of phase controller operation.

Multiplexer U4 supplies the trip signal to an opto-coupler located on the test board in the display module (Section 9). This current signal gives the trip signal good immunity against noise transients as the opto-coupler has a slow turn-on time.

Table 12-1. Replaceable parts, phase controller modules for RFL 9300 Charge Comparison System RFL 93B PC (Assembly No. 106370)

Circuit Symbol (Figs. 12-3 & 12-4)	Description	Part Number
	CAPACITORS	
C1-23,36-38	Capacitor,ceramic,0.1μF,GMV,50V,Centralab CY20C104P or equiv.	1007 1366
C24,25	Capacitor,ceramic,0.01μF,5%,100V,AVX SR301A103JAA or equiv.	1007 1645
C26,27	Capacitor,ceramic,22pF,5%,100V,AVX SA101A220JAA or equiv.	0125 12205
C28-35	Capacitor,tantalum,3.3μF,20%,35V,Kemet T322C335M035AS or equiv.	1007 1260
C39	Capacitor,tantalum,33μF,10%,10V,Kemet T322D336K010AS or equiv.	1007 1142
C40,41	Capacitor,electrolytic,47μF,+50-10%,25V,Panasonic ECEA1EV470S or equiv.	1007 1578
	RESISTORS	
R1-6,12,13,21	Resistor,metal film,1K,1%,1/4W, Type RN1/4	0410 1288
R7,8,11,23,26	Resistor,metal film,10K,1%,1/4W, Type RN1/4	0410 1384
R9	Resistor,metal film,5.62K,1%,1/4W, Type RN1/4	0410 1360
R10	Resistor,metal film,154K,1%,1/4W, Type RN1/4	0410 1498
R14	Resistor,metal film,15K,0.1%,1/8W,10 ppm/^{O}C,Dale Type PTF56-15K0-B-T13 or equiv.	1510 2149
R15	Resistor,metal film,5K,0.1%,1/8W,10 ppm/^{O}C,Dale Type PTF56-5K00-B-T13 or equiv.	1510 2145
R16,27	Resistor,metal film,5.11K,1%,1/4W, Type RN1/4	0410 1356
R17,18	Resistor,metal film,1K,0.1%,1/8W,10 ppm/^{O}C,Dale Type PTF56-1K00-B-T13 or equiv.	1510 2129
R19,20	Resistor,metal film,10K,0.1%,1/8W,10 ppm/^{O}C,Dale Type PTF56-10K00-B-T13 or equiv.	1510 2132
R22	Resistor,metal film,200Ω,1%,1/4W, Type RN1/4	0410 1221

Table 12-1 continued. Replaceable parts, phase controller modules for RFL 9300 Charge Comparison System

Circuit Symbol (Figs. 12-3 & 12-4)	Description	Part Number
	RESISTORS - continued.	
R24,25	Resistor,metal film,221W,1%,1/4W, Type RN1/4	0410 1225
R28	Resistor,metal film,100W,1%,1/4W, Type RN1/4	0410 1192
RZ1-6	Resistor network,nine 10KW 2% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-103 or equiv.	32622
RZ7	Resistor network,nine 47KW 2% resistors,2.7W total,10-pin SIP,TRW/IRC 810-1-473G or equiv.	49511
	SEMICONDUCTORS	
CR1-3	Diode,silicon,1N914B or 1N4448	26482
DS1,2	Light-emitting diode,red,right-angle PC mount,extended length,Industrial Devices 5300H1 or equiv.	99294
U1	MOS tri-state octal buffer,inverting,20-pin DIP,National Semiconductor MM74HC240N or equiv.	0615 182
U2	MOS hex inverter,14-pin DIP,Motorola MC74HC05N or equiv.	0615 371
U3	MOS quad buffer/line driver,14-pin DIP,Signetics 74HC125N or equiv.	0615 292
U4	MOS multiplexer,8-input,tri-state outputs,16-pin DIP,Motorola MC74HC251N or equiv.	0615 372
U5	MOS tri-state buffer,16-pin DIP,National Semiconductor MM74HC367N or equiv.	0615 290
U6	MOS triple 3-input NAND gate,14-pin DIP,National Semiconductor MM74HC10N or equiv.	0615 162
U7	MOS dual retriggerable monostable multivibrator,16-pin DIP,National Semiconductor MM74HC123N or equiv.	0615 282
U8	Microprocessor supervisor,8-pin DIP,Maxim MAX690EPA or equiv.	0635 27
U9	CHMOS microcontroller,16-bit/16-MHz,ROM-less,68-pin PLCC package, Intel N80C196KD or equiv.	0615 459
U10	MOS quad 2-input NAND gate,14-pin DIP,Motorola MC74ACT00N or equiv.	0615 375
U11	MOS dual 2- to 4-line decoder,16-pin DIP,Motorola MC74ACT139N or equiv.	0615 378
U12,13	MOS octal latch,tri-state,20-pin DIP,Motorola MC74ACT573N or equiv.	0615 382
U14,15	MOS EPROM,32K x 8, 28-pin ceramic DIP, AMD AM27C256-70DI or equiv.	0615 401
U16,17	MOS octal buffer/driver,20-pin DIP,Motorola MC74ACT541N or equiv.	0615 381
U18,20	MOS octal D-type flip-flop,20-pin DIP,Motorola MC74ACT574N or equiv.	0615 383
U19	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U21	MOS shift register,8-input,tri-state outputs,16-pin DIP,Motorola MC74HC595N or equiv.	0615 373
U22	Analog-to-digital converter,8-bit,8-pin plastic DIP,Texas Instruments TLC549IP or equiv.	0625 30
U23	Linear precision voltage reference,+5V,8-pin DIP,Maxim MAX675EPA or equiv.	0620 342
U24	Linear operational amplifier,low offset voltage,8-pin ceramic DIP, Precision Monolithics OP77EZ or equiv.	0620 340
U25	MOS dual analog switch,SPST,14-pin ceramic DIP,Siliconix DG200ABK or equiv.	0605 14
U26	Linear operational amplifier,JFET input,8-pin DIP,Texas Instruments TL081IP or equiv.	0620 228
	MISCELLANEOUS COMPONENTS	
J1	Shorting bar,single,Molex 90059-0009 or equiv.	98306
Y1	Crystal,quartz,16.000 MHz	30297

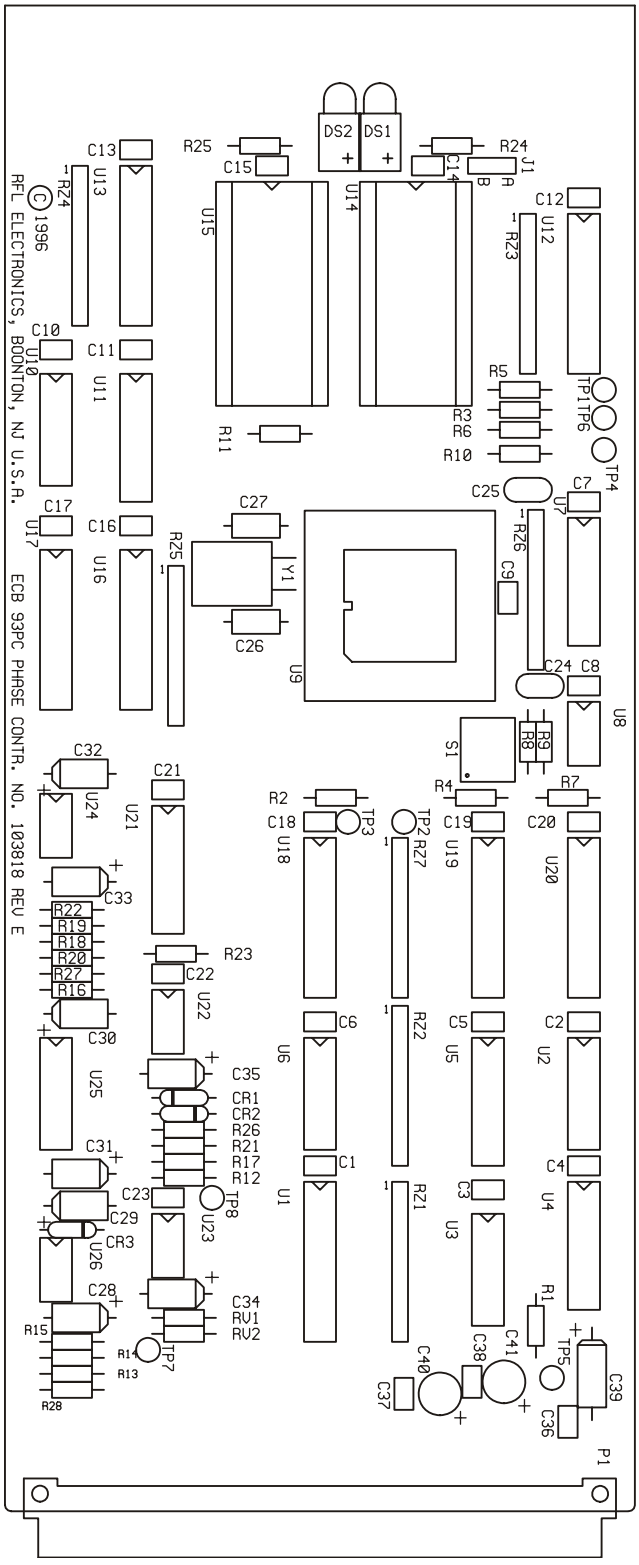


Figure 12-3. Component locator drawing, phase controller modules for RFL 9300 Charge Comparison System (Assembly No. 106370)

Figure 12-4. Phase Controller modules for RFL 9300 Charge Comparison System (Assembly No. 106370; Schematic No. D-103819, Rev. D) Sheets 1 of 2 an 2 of 2

Please see Figure 12-4, Sheets 1 of 2 and 2 of 2, in Section 32: Schematics

SECTION 13: COMMUNICATIONS CONTROLLER MODULE



a. RFL 93A CC-H (horizontal mount.)



a. RFL 93A CC-V (vertical mount.)

Figure 13-1. RFL 9300 communications controller module

13.1 DESCRIPTION

The RFL 93B CC Communications Controller Module (Fig. 13-1) regulates all messages sent from one RFL 9300 to another. The communications can be any one of the following:

1. 7.2-Kbps data using the RFL 93B MO Modem Module.

2. 56-Kbps or 64-Kbps data using the RFL 93 DD Direct Digital I/O Module.

3. 56-Kbps or 64-Kbps data using the RFL 93 FT/FR fiber optic I/O module.

During turn-on, the RFL 93B CC module learns the RFL 9300's communication configuration. It does this by measuring the clock rate, testing control lines, and reading the strap settings on the RFL 93B SV Supervisor Controller Module. It then uses this information to control communications.

13.2 CONTROLS AND INDICATORS

Figure 13-2 shows the location of all controls and indicators on the RFL 93B CC Communications Controller Module. These controls and indicators are described below. Those described as front-panel controls are accessible with the RFL 93B CC installed in the RFL 9300 chassis; all others are only accessible when the RFL 93B CC is removed from the chassis, or is on a card extender.

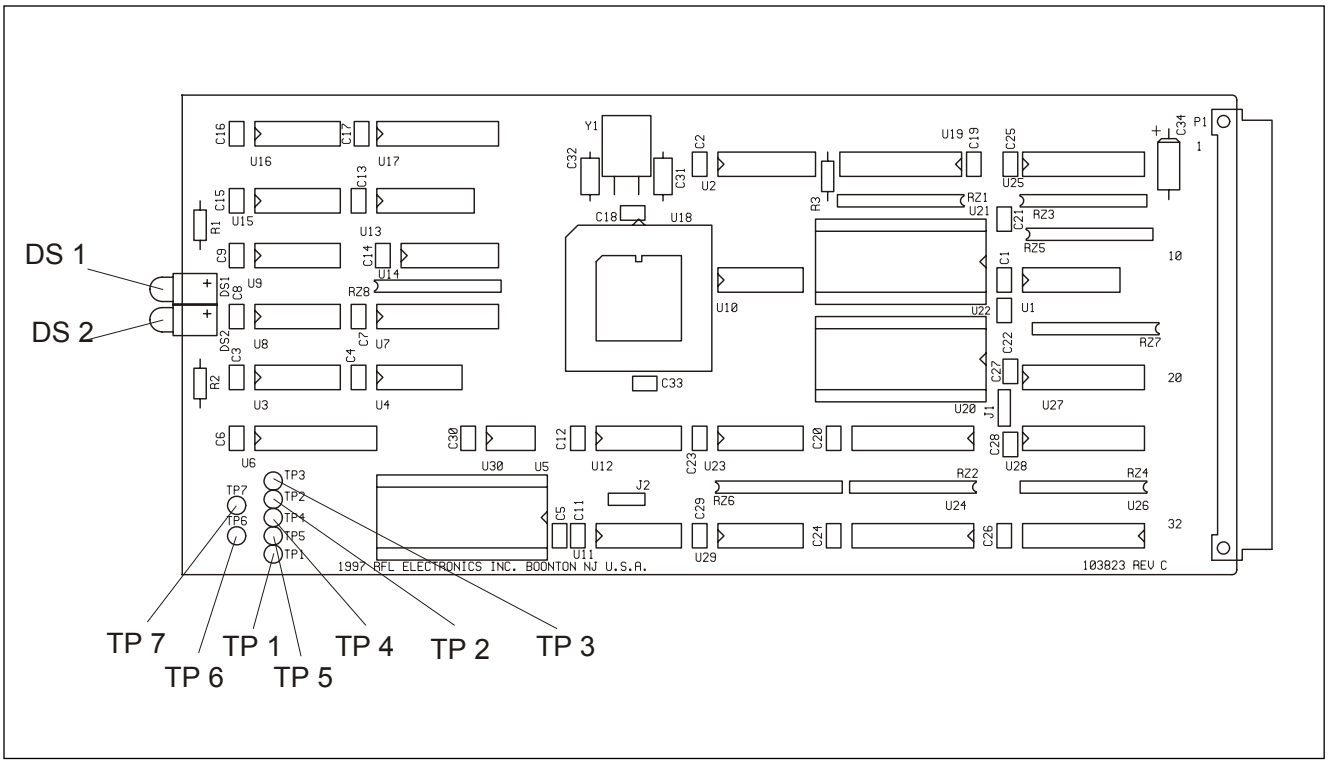


Figure 13-2. Controls and indicators, RFL 9300 communications controller module

LED INDICATORS

DS1 P-P - Front-panel indicator; lights green when a ping-pong test (round-trip delay measurement) is in progress.

DS2 BER OK - Front-panel indicator; lights green when the bit error rate (BER) is within limits.

JUMPERS

J1 Set at the factory according to the device type installed for EPROM's U21 and U22. **Do not change the setting of this jumper, unless U21 and U22 are being replaced with another device type.**

TEST TURRETS

TP1 Measuring point for TX SYNC pulse, which must occur once per word sent.

TP2 Measuring point for TC DATA, which must be valid on positive clock edge at TP3.

TP3 Measuring point for TX CLOCK.

TP4 Measuring point for RX DATA, which must be valid on positive clock edge at TP5.

TP5 Measuring point for RX CLOCK.

TP6 Ground reference.

TP7 Measuring point for RX NOT VALID signal.

13.3 THEORY OF OPERATION

The RFL 93B CC controls all communications between one RFL 9300 and another. A block diagram of the RFL 93B CC appears in Figure 13-3.

13.3.1 OVERVIEW

The RFL 93B CC Communications Controller Module contains a 16-bit microcontroller that works with dedicated logic circuits. These circuits work together to regulate all messages sent from one RFL 9300 to another. The communications can be any one of the following:

1. 7.2-Kbps data over a modem, such as the RFL 93B MO Modem Module.

2. 56-Kbps or 64-Kbps data using a direct digital interface, such as the RFL 93 DD module.

3. 56-Kbps or 64-Kbps data over fiber optic cables, using a RFL 93 FT/FR fiber optic module.

During turn-on, the RFL 93B CC module learns the RFL 9300's communication configuration. It does this by measuring the clock rate, testing control lines, and reading the strap settings on the RFL 93B SV Supervisor Controller Module. The RFL 93B CC does not have any strap settings for different communication configurations. Its software switches internally, depending on the system's communication configuration and data rate. Those functions that are common to all communication configurations and speeds will be described first; more specific configurations will be described later.

Messages can originate in any one of seven modules within the system. Most messages pass through the RFL 93B SV Supervisor Module to the RFL 93B CC module by way of an eight-bit bus. When a message arrives, the microcontroller establishes its priority and stores it in the microcontroller's internal RAM. If the message contains time values, the microcontroller increments the time and erases the message if overflow occurs before the message can be sent.

The microprocessor compresses the message with the highest priority and loads it into the transmitter shift registers, along with CRC bits. The RFL 93B CC module at the remote RFL 9300 will use the CRC bits to test the message when it receives it. All messages between RFL 9300's are sent synchronous and serial. The simplest messages consist of single fifteen-bit word; the most complicated requires two fifteen-bit words. Each word contains eight data bits and six CRC bits.

The transmitter logic circuits insert a frame bit to mark the beginning of each word. This bit toggles from one group of data and CRC bits to the next group of data and CRC bits. Words are continually sent, even if there is nothing to communicate; null words fill in the voids. By always sending valid words, the remote RFL 9300 can frame, regardless of the state of the transmitting RFL 9300. Incoming words pass through the receiver shift registers, where a comparator and EPROM look-up table combine to test the CRC security of each word. The security test is done in hardware because of the high speeds possible with 56 or 64-Kbps communication.

The microcontroller frames the data by resetting a fifteen-state counter when the data, CRC, and frame bits line up. The counter then automatically generates a latch signal for future data reads by the microcontroller. After the microcontroller accepts a valid secure word, it translates and expands it into a message. The message usually passes to the RFL 93 SV module for distribution to other modules in the system.

After two RFL 9300's establish a bi-directional communication link, each unit measures the average one-way channel delay. This delay, called "CDC-P" (channel delay compensation - ping-pong), is passed on to the supervisor. The RFL 93B CC module continually monitors the channel delay, and reports any significant changes to the supervisor.

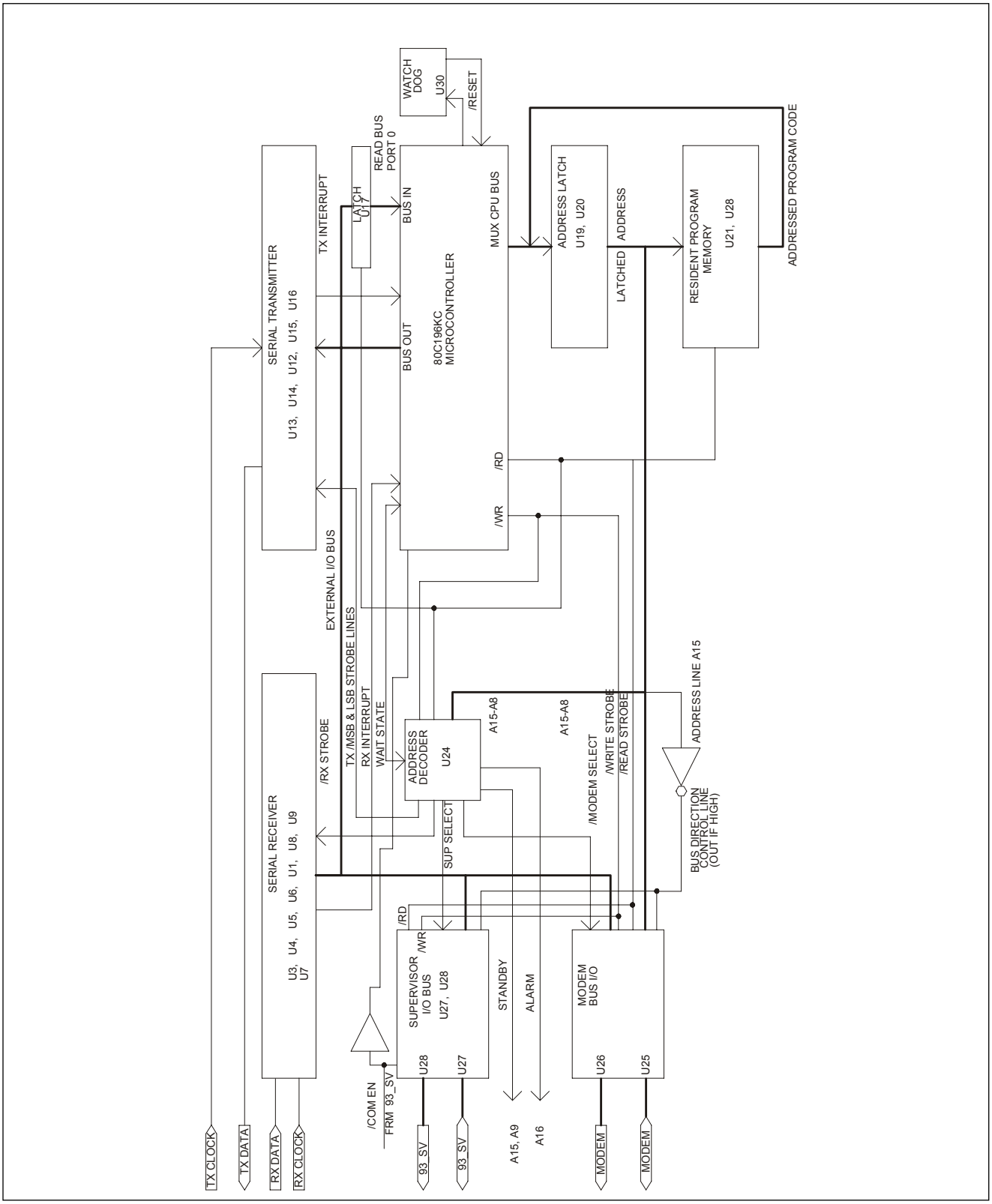


Figure 13-3. Block diagram, RFL 9300 communications controller module

13.3.1.1 SINGLE-CHANNEL MODEM OPERATION

If the RFL 9300 contains an RFL 93B MO Modem Module in the first module slot, the RFL 93B CC module will initialize and reset the modem over a dedicated sixteen-bit bus. Control bits in the RFL 93B MO module are set or cleared to configure the modem for CCITT V.29 operation at 7.2 Kbps.

Modems occasionally require training from the remote RFL 9300; when necessary, training request messages are generated in the RFL 93B CC module. The words passed between the RFL 93B MO and RFL 93B CC modules at both units are synchronous and serial. The squelch rules that define word validity depend on the communication system; the modem rules are tested with each received word. These rules also determine if an alarm should be sent to the RFL 93B SV module, or if the serial communications coming in from the modem needs to be framed.

13.3.1.2 HOT STANDBY TWO-CHANNEL MODEM OPERATION

If the RFL 9300 contains a second RFL 93B MO modem module in the second module slot and the system is not configured for three-terminal operation, it is configured for hot standby operation. The RFL 93B CC module in the third module slot learns the system during turn-on and controls both modems. It sends and receives initialization and training commands to maintain communications over both modems. The RFL 93B CC module controls the channels and automatically switches if the active channel fails. After switching over, the RFL 93B CC sends a message to the remote RFL 9300; when the remote RFL 9300 receives this message, it will switch its modems. In every other way, the RFL 93B CC module acts the same as single-channel modem operation.

13.3.1.3 SINGLE-CHANNEL 56-Kbps OR 64-Kbps DIGITAL OR FIBER OPTIC OPERATION

If the RFL 9300 contains an RFL 93 DD Direct Digital I/O Module or an RFL 93 FT/FR module, the RFL 93B CC module learns the communication configuration based on the clock rate received and the strap settings passed over from the RFL 93B SV. The RFL 93B SV uses modified high bit-rate squelch rules and alarm conditions. Each word is repeated three times during transmission, and a voting scheme determines validity. The remote RFL 93B CC module super-frames on the blocks of three, and uses two-out-of-three voting logic. Direct digital operation is synchronous, with the transmit and receive clocks supplied by the data communication equipment (DCE). A port for TX DATA and RX DATA is also provided.

13.3.1.4 HOT STANDBY TWO-CHANNEL 56-Kbps OR 64-Kbps DIRECT DIGITAL OPERATION

If the RFL 9300 contains two RFL 93 DD Direct Digital I/O Modules, the RFL 93B CC module learns the communication configuration based on the clock rate and the strap settings passed over from the RFL 93A SV module. The RFL 93B CC modules in both RFL 9300's use high bit-rate squelch rules and commands to control switchover if a channel should fail several frame attempts.

NOTE

Refer to Table 2-1 for valid Hot-Standby configurations

13.3.2 HARDWARE DESCRIPTION

13.3.2.1 WATCHDOG RESET FUNCTION

The RFL 93B CC module contains a 16-bit microcontroller (U18). U18 must be reset during turn-on or if the internal software program counter causes a program jump to a wrong location. Watchdog timer U30 pulls U18-7 (/RESET) if there are no transitions into U18-6 (WDI) for 1.6 seconds; this causes a reset. U30 also will assert a low on U18-7 for at least 50 ms if the voltage into U30-2 (Vcc) falls below 4.65 volts. In the software, each routine toggles a test bit internal to U18. After all routines have successfully executed and the test bits are correct, the port 2.6 line out of U18 toggles. This pushes back the 1.6-second timer inside U30. U30-7 also connects to the transmitter shift registers (U13-10 and U14-10). Zeroes are forced out of the shift register; these are invalid word that prevent old or extraneous messages from being sent.

13.3.2.2 TRANSMITTER CIRCUIT

A timing diagram for the RFL 93B CC's transmitter circuit appears in Figure 13-4.

Transmitter shift registers U13 and U14 are loaded with data and CRC bits through a software created bus located on port 1 of microcontroller U18. U18 loads eight data bits out of port 1, and then writes them to address location 6600H. This causes pin 16 on programmable logic device U24 to strobe low. This is fed to U14-12, latching the data into U14. Next, the CRC bits are loaded into port 1 U18 and written into address location 6400H. This causes U24-15 to strobe low, latching the CRC into U13. U9 and U15 form a fifteen-state counter. During each TX CLOCK negative edge, a bit is shifted out of the transmitter shift and the counter is incremented. On the fifteenth count, a frame bit stored at U12-12 toggles and passes through U16-1. This creates the word pattern of a toggled frame bit followed by eight data bits and then six CRC bits followed by another toggled frame bit. Two interrupt lines come from the fifteen-state counter and connect to U18-25 and U18-26.

If the data rate is high (56 or 64 Kbps), a negative edge on U18-25 will cause U18 to enter the transmitter interrupt routine. If the data rate is low (7.2 Kbps), a positive edge on U18-26 will cause U18 to enter the transmitter interrupt routine. The RFL 93B CC selects the interrupt pin to use during turn-on, when it learns the communication configuration. There are two different interrupt lines because U18 needs more lead time during 56-Kbps or 64-Kbps operation; the interrupt must service the shift registers before the end of the fifteenth pulse interval. If nothing new is latched into the shift registers the same word and CRC bit combination repeats indefinitely until another word/CRC bit combination is loaded. While framing the receiver, the same (null word) word is repeated. This is done because framing requires the full use of the microcontroller for a five-word interval.

13.3.2.3 RECEIVER CIRCUIT

A timing diagram for the RFL 93B CC's receiver circuit appears in Figure 13-5.

The receiver logic hardware consists of shift registers U3 and U4, comparator U6, EPROM U5, a fifteen-state counter formed from U8 and U9, and latches U7 and U12. When correctly framed, the frame bit plus eight data bits are present on U5's address lines. The fifteen-state counter latches the data into U7 when U7-11 goes low. The received CRC and trailing flag bit are also present on U6's "P" inputs. A look-up table in U5 contains the valid matching CRC and trailing frame bit; the look-up value is present on U6's "Q" inputs. U6-19 goes low if the CRC plus trailing frame bit matches the look-up code base on the received data and leading (opposite) frame bit. This low signal is latched into U12 on U12-5 and fed to U18-17. The latch strobe also goes to the microcontroller U18-38, where an interrupt occurs on the low-to-high transition. U18 reads the data latched in U7 and tests U18-17 (P2.1) to see if the data is valid during the processing of the word.

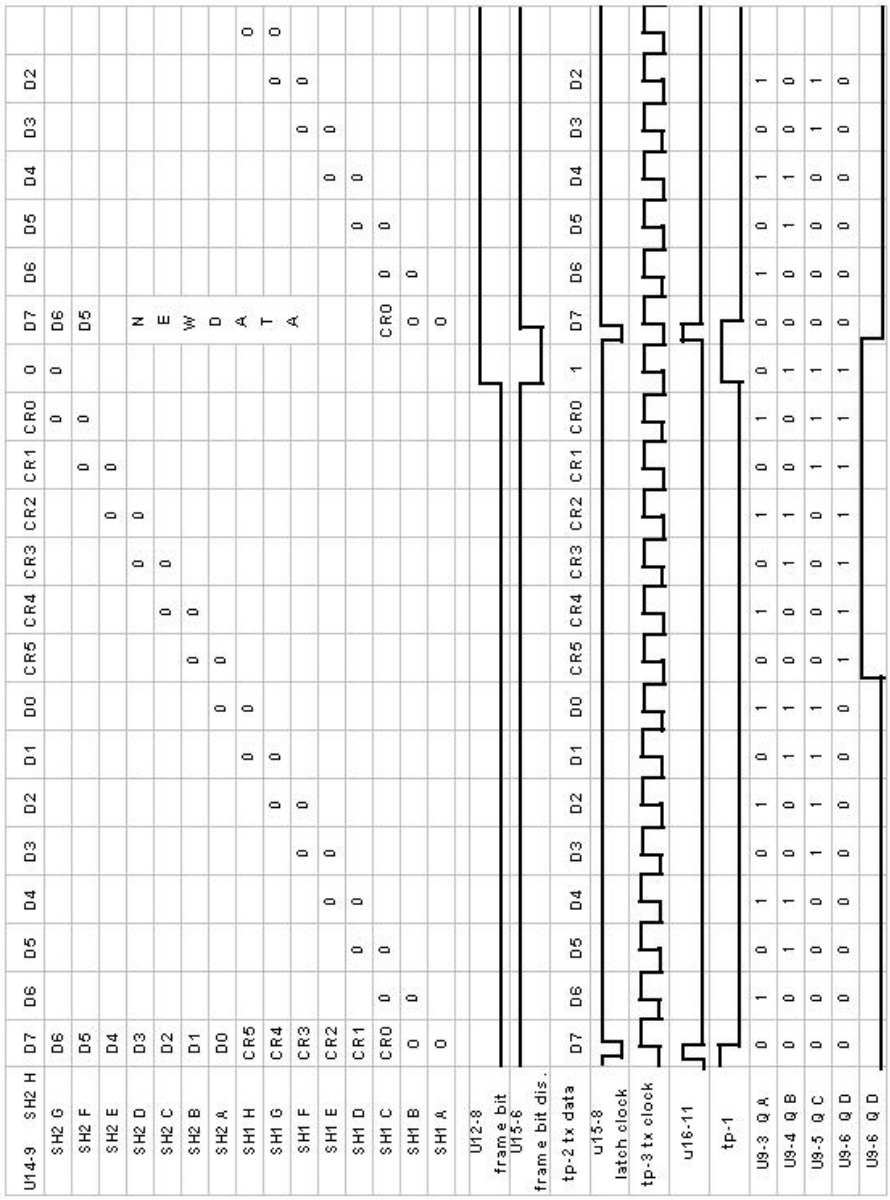


Figure 13-4. Transmitter timing diagram, RFL 9300 communications controller module

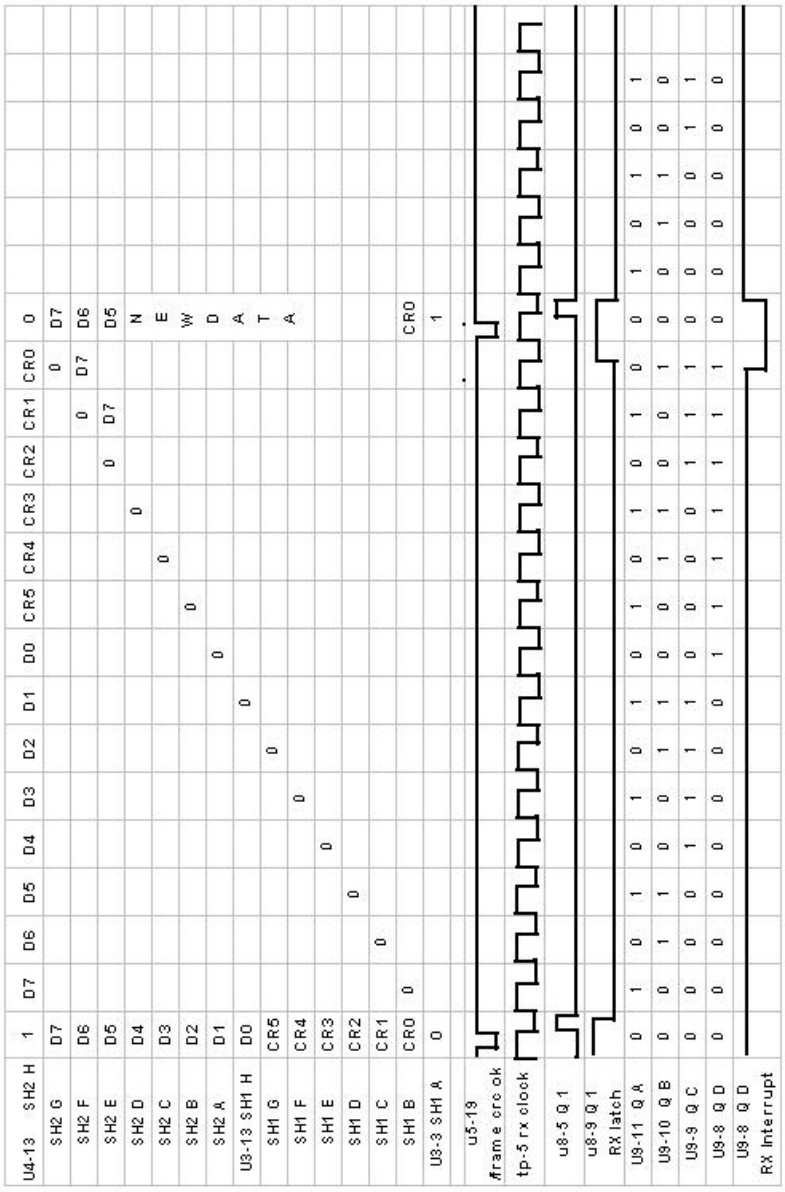


Figure 13-5. Receiver timing diagram, RFL 9300 communications controller module

To read the data latched into U7, U18 executes a read operation at address A400H. This causes U24-14 to go low, enabling U7's output pins. The data is then latched into U17 by the low-going READ strobe issued from the microcontroller during the read operation. The received data is now present on port 0 of U18 and read in.

13.3.2.4 READ AND WRITE CIRCUITS FOR RFL 93B SV SUPERVISOR CONTROLLER

Reading and writing over the eight-line bus between the RFL 93B CC and RFL 93B SV modules uses octal transceiver U27, octal buffer U28, quad buffer/line driver U29, and programmable logic array (PAL) U24; octal latch U17 is only used during READ operations. When the /COMM EN line from the RFL 93B SV supervisor goes low on edge connector terminal P1-A14, U10-6 goes low, feeding U18-27. This low-going signal causes an interrupt within U18 that starts the supervisor read/write routine ("SUPER:"). The /COMM EN interrupt should take place every 500 ms if the supervisor is functioning properly. U28-1 and U27-19 will unconditionally be high if the /COMM EN line is high; this disables U27 and U28, blocking any possible contention on the supervisor bus.

During a WRITE sequence with the supervisor, U28-16 drives the /CS line low; the data to be written is then present out microcontroller port 1. U18 then performs a WRITE operation to address 6200H; this causes U24-13 to go low. The write strobe line into U28 (U28-15) goes low, then high. The write protocol causes three write operations in a row: address, data, and security byte.

During a READ sequence with the supervisor, the /CS line is driven low by U28-16. Then, U18 performs a read operation from address A200H, causing U24-13 to go low. This is followed by a read strobe signal that goes low into U28-13 and latches the data read into U17. U18 then reads the data present on port 0. The read protocol initiates three read operations in a row: address, data, and security byte.

13.3.2.5 READ AND WRITE CIRCUITS FOR RFL 93B MO MODEM MODULE

Reading and writing over the eight-bit bus connecting the RFL 93B CC module and the RFL 93B MO module uses octal transceiver U25, octal buffer/line driver U26, and programmable logic array (PAL) U24; octal latch U17 is used during read operations. The address is sent over the bus first, followed by the data. When U6-16 is high, the data out of U25 is the address or reset command for the RFL 93B MO module. During a write sequence, the address of the register in the modem that will accept the data is outputted on U18 port 1. A write operation is executed at address 6020H; this forces U6-16 high and U24-12 low, enabling U25 and U26. This is followed by a write strobe (/WR) issued from the microcontroller on U26-18.

Next, the data to be written to the RFL 93B MO module is presented on port 1, and a write operation is executed at address 6000H. This causes U24-12 to go low, enabling U25 and U26. A write strobe will occur while U6-16 is low, loading the data through U25 into the RFL 93B MO module.

During a read sequence from the RFL 93B MO module, the address to be read from is first written to the RFL 93B MO module as described above. Next, the microcontroller executes a read operation by reading memory at address location A000H. This forces U24-12 low, enabling U25 and U26. The /RD read strobe is then outputted to edge connector terminal P1-A30 through U26-17.

U25 is a bi-directional transceiver that receives from "B to A" if U25-1 is low. The data is then latched into U17 and present on port 0. The microcontroller then reads the data from the RFL 93B MO module on port 0.

13.3.2.6 ADDRESS DECODER

Address decoder U24 is a programmed logic device that provides a decoder for external bus reads, a wait-state signal for microcontroller U18, and latched outputs for the alarm and hot standby lines. U24's inputs are microcontroller address bus A15 through A8, and the /READ and /WRITE strobe lines. A logic diagram for U24 appears in Figure 13-6.

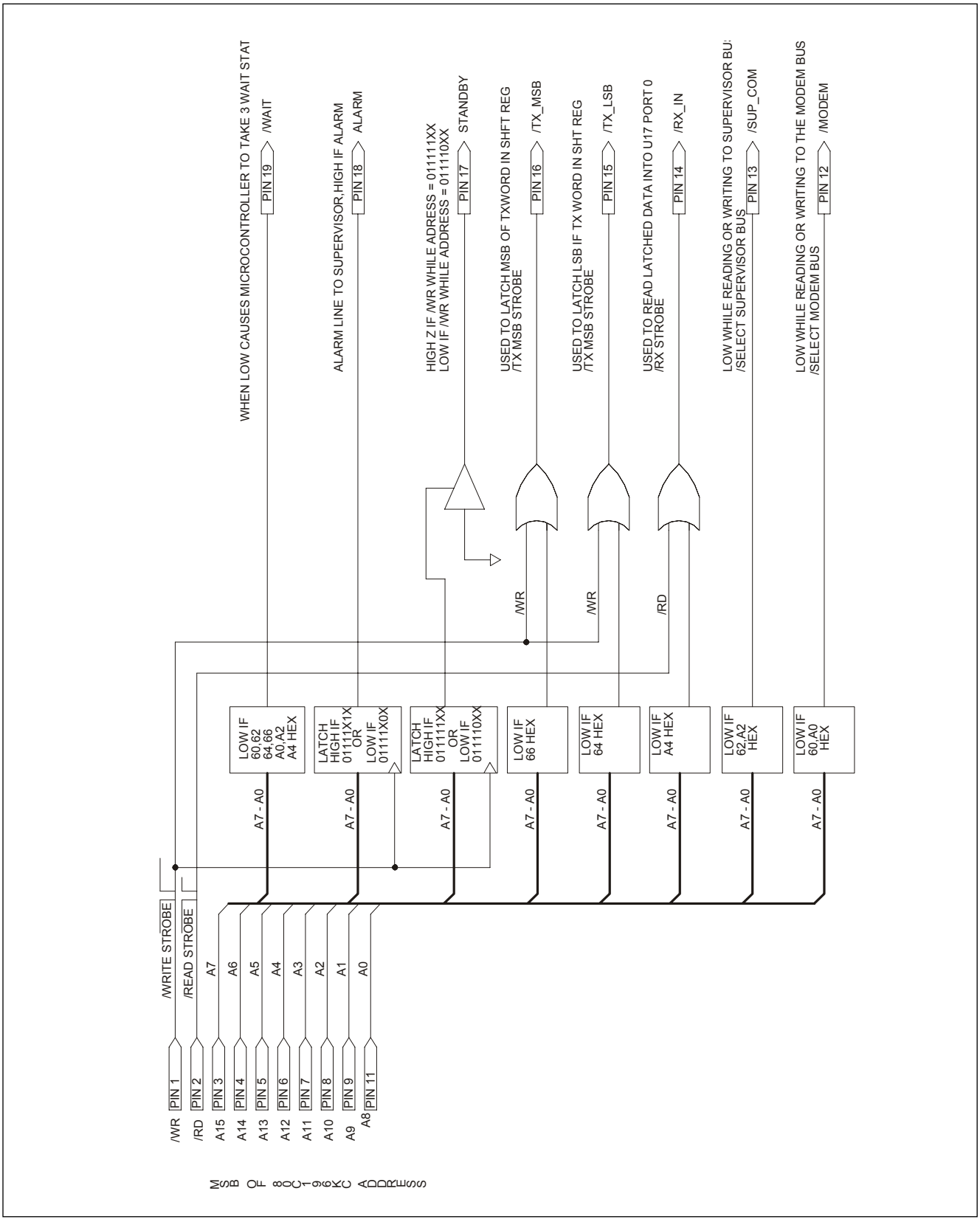


Figure 13-6. Logic diagram for programmable logic device U24

All external read and write operations from the microcontroller use U24 to create a dedicated strobe or select line. For example, when data is to be written into transmitter shift register U14, a write operation is performed in the microcontroller. This operation is an intrinsic operation built into the microcontroller. The bus cycle within the microcontroller first outputs an address onto address lines AD15 through AD0, and then issues a low-going write strobe (/WR) 115 ns later.

If the address presented to U24 is equal to 6600H (0110011000000000), U24-16 goes low when the /WR input goes low. This provides a latch strobe for U14. U24-19 also goes low for any external memory read or write operation that is fed back into the microcontroller on U18-43. This line controls the number of wait states taken by external operations; slowing the /WR and /RD strobe line down for the slower peripheral logic devices, such as U14.

Table 13-1. Replaceable parts, communications controller modules for RFL 9300 Charge Comparison System RFL 93B CC (Assembly No. 106365)

Circuit Symbol (Figs. 13-7 & 13-8)	Description	Part Number
	CAPACITORS	
C1-9,11-30,33	Capacitor,ceramic,0.1mF,GMV,50V,Centralab CY20C104P or equiv.	1007 1366
C10	Not used.	
C31,32	Capacitor,ceramic,22pF,5%,100V,AVX SA101A220JAA or equiv.	0125 12205
C34	Capacitor,tantalum,33mF,10%,10V,Kemet T322D336K010AS or equiv.	1007 1142
	RESISTORS	
R1,2	Resistor,metal film,221W,1%,1/4W, Type RN1/4	0410 1225
R3	Resistor,metal film,10KW,1%,1/4W, Type RN1/4	0410 1384
RZ1-4,8	Resistor network,nine 10KW 2% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-103 or equiv.	32622
RZ5	Resistor network,five 150W,2% resistors,2.5W total,10-pin SIP,Dale MSP10C03151G or equiv.	100571
RZ6,7	Resistor network,nine 47KW 2% resistors,2.7W total,10-pin SIP,TRW/IRC 810-1-473G or equiv.	49511
	SEMICONDUCTORS	
DS1,2	Light-emitting diode,green,right-angle PC mount,Industrial Devices 5300H5 or equiv.	32567
U1	MOS quad differential line receiver,16-pin DIP,National Semiconductor DS34C86N or equiv.	0615 394
U2	MOS quad differential line driver,16-pin DIP,National Semiconductor DS34C87N or equiv.	0615 395
U3,4	MOS shift register,8-bit,serial in/parallel out,16-pin DIP, National Semiconductor MM74HC164N or equiv.	0615 173
U5,21,22	EPROM,UV-eraseable,8K x 8,programmed at factory	Contact factory
U6	MOS 8-bit magnitude comparator,20-pin DIP,National Semiconductor MM74HC688N or equiv.	0615 183
U7,17	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U8,12,15	MOS dual D-type flip-flop w/preset and clear,14-pin DIP, National Semiconductor MM74HC74N or equiv.	0615 166
U9	MOS dual 4-bit binary counter,14-pin DIP,National Semiconductor MM74HC393N or equiv.	0615 192
U10	MOS quad 2-input Exclusive-OR gate,14-pin DIP,RCA CD74HCT86E or equiv.	0615 390

Table 13-1 continued. Replaceable parts, communications controller module for RFL 9300 Charge Comparison System

Circuit Symbol (Figs. 13-7 & 13-8)	Description	Part Number
	SEMICONDUCTORS - continued.	
U11	MOS hex inverter,14-pin DIP,National Semiconductor MM74HC04N or equiv.	0615 185
U13,14	MOS shift register,8-input w/input flip-flop,16-pin DIP,Motorola MC74HC597N or equiv.	0615 374
U16	MOS quad 2-input OR gate,14-pin DIP,National Semiconductor MM74HC32N or equiv.	0615 165
U18	CHMOS microcontroller,16-bit/16-MHz,ROM-less,68-pin PLCC package, Intel TN80C196KC-16 or equiv.	0615 384
U19,20	MOS octal latch,tri-state,20-pin DIP,Motorola MC74ACT573N or equiv.	0615 382
U23	MOS quad 2-input NOR gate,14-pin DIP,Motorola MC74ACT02N or equiv.	0615 376
U24	MOS programmable logic array (PAL), programmed at factory	Contact factory
U25,27	MOS tri-state octal transceiver 20-pin DIP,National Semiconductor MM74HC245N or equiv.	0615 177
U26	MOS octal tri-state non-inverting buffer/line driver,20-pin DIP, National Semiconductor MM74HC541N or equiv.	0615 297
U28	MOS tri-state octal buffer,20-pin DIP,National Semiconductor MM74HC244N or equiv.	0615 176
U29	MOS quad buffer/line driver,14-pin DIP,Signetics 74HC125N or equiv.	0615 292
U30	Microprocessor supervisor,8-pin DIP,Maxim MAX690EPA or equiv.	0635 27
	MISCELLANEOUS COMPONENTS	
J1,2	Shorting bar,single,Molex 90059-0009 or equiv.	98306
Y1	Crystal,quartz,16.000 Mhz	30297

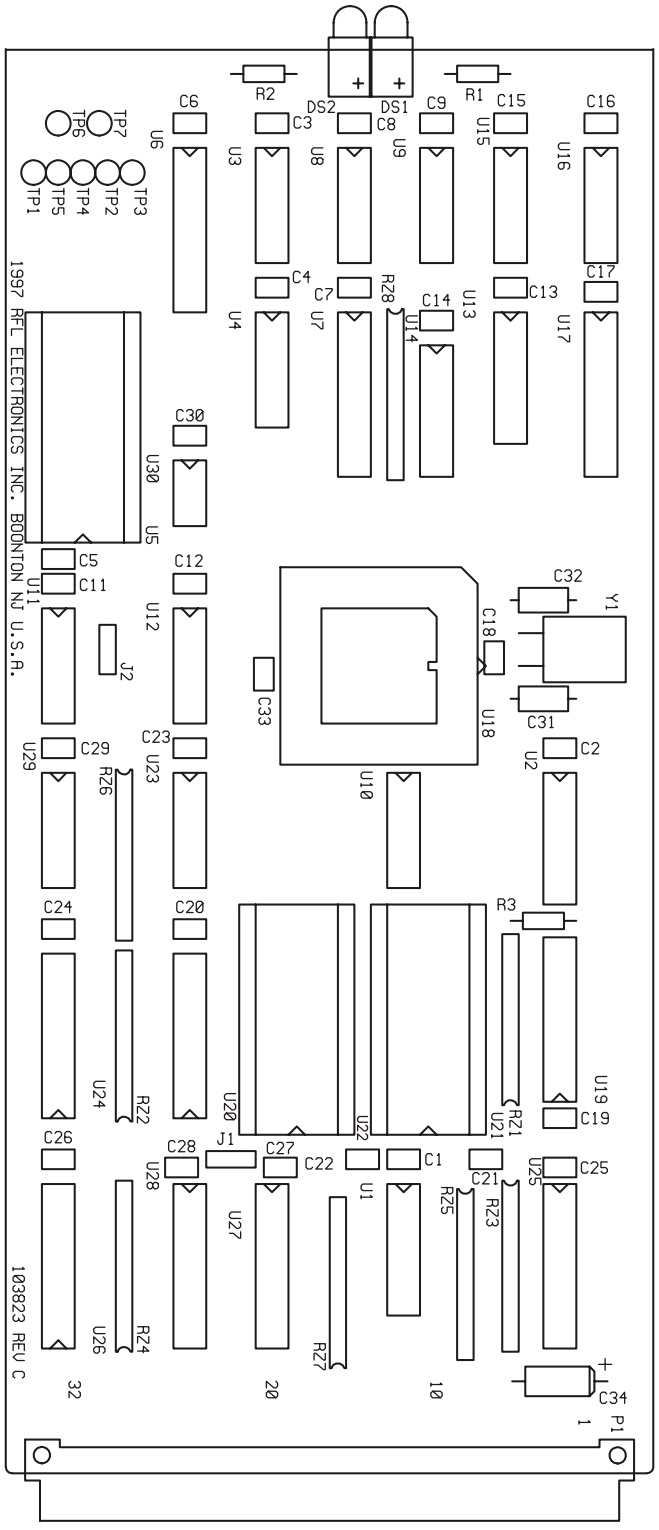


Figure 13-7. Component locator drawing, communications controller module for RFL 9300

Figure 13-8. Communications Controller modules for RFL 9300 Charge Comparison System (Assembly No. 106365; Schematic No. D-103824, Rev. A) Sheets 1 of 2 and 2 and 2

Please see Figure 13-8, Sheets 1 of 2 and 2 of 2, in Section 32: Schematics

SECTION 14: MODEM MODULE

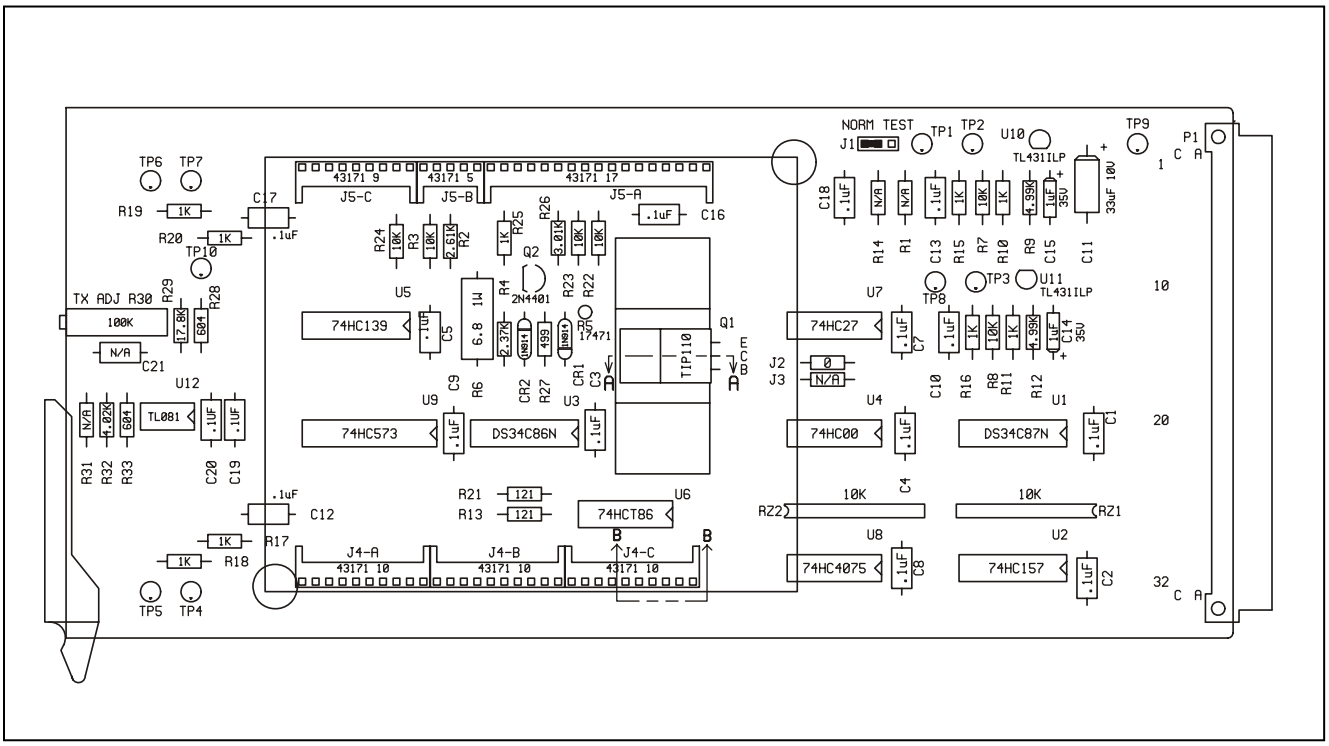


Figure 14-1. RFL 9300 modem module

14.1 DESCRIPTION

The RFL 93B MO Modem Module (Fig. 14-1) contains a receiver for converting incoming analog signals into digital signals for use in the RFL 93B CC module, and a transmitter for converting digital signals from the RFL 93B CC into analog signals that are passed to the RFL 93 LC I/O and on to the telephone line. The RFL 93B CC module has two links with the RFL 93B MO; a synchronous serial data link that sends and receives relay data, and a parallel control bus that monitors and controls the RFL 93B MO.

14.2 CONTROLS AND INDICATORS

The RFL 93B MO contains controls and indicators that are used to prepare the RFL 93B MO for use and to monitor its operation. Figure 14-2 shows the location of these controls and indicators; they are described below. None of the RFL 93B MO's controls and indicators are accessible with the module installed in the RFL 9300 chassis; they can only be accessed when the RFL 93B MO is removed from the chassis, or is on a card extender.

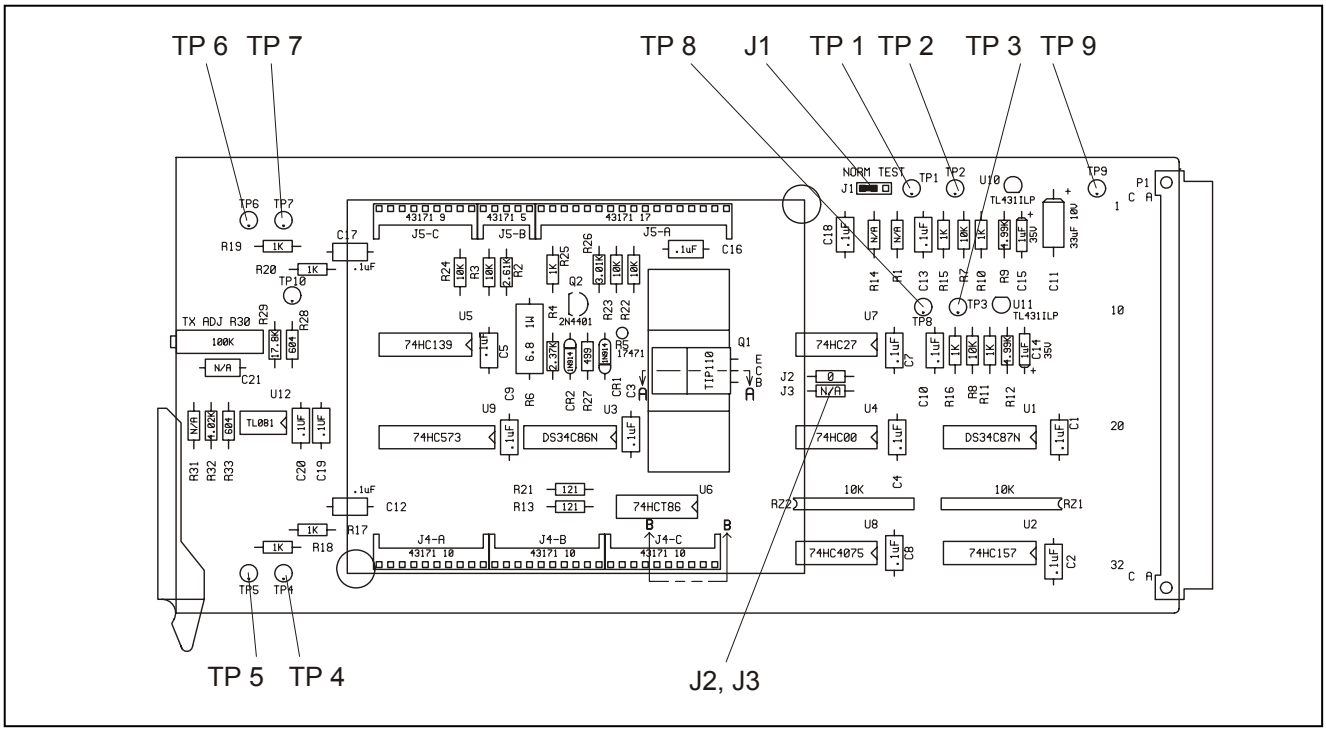


Figure 14-2. Controls and indicators, RFL 9300 modem module

JUMPERS

J1 Controls attenuation between RFL LC I/O module and RFL 93B MO. Place in Position A for no attenuation, or Position B for 3 dB of attenuation.

J2, J3 These jumpers control the polarity of the RD (read) line:

J2 in, J3 out - Normal polarity (RD).
J2 out, J3 in - Inverted polarity (/RD).

J2 and J3 are set at the factory according to the requirements of the plug-on modem card. **Do not move these jumpers, unless the modem card is being replaced with a different type.**

TEST POINTS

TP1 Monitoring point for RX IN; this is an analog signal that should be around -18 dBm if jumper J1 is in Position A.

TP2 Monitoring point for +12-volt regulator; should be between +11.4 and +12.6 volts.

TP3 Monitoring point for -12-volt regulator; should be between -11.4 and -12.6 volts.

TP4 Monitoring point for RX clock; this is a digital signal that varies between 0 and 5 volts at a rate of 7.2 Kbps.

TP5 Monitoring point for RX data (recovered data); this is a digital signal that varies between zero and 5 volts.

TP6 Monitoring point for TX data received from RFL 93B CC module; this is a digital signal that varies between zero and 5 volts.

TP7 Monitoring point for TX clock; this is a digital signal that varies between zero and 5 volts at a rate of 7.2 Kbps.

TP8 Monitoring point for TX OUT; this is an analog signal (+2 dBm nominal).

14.3 THEORY OF OPERATION

14.3.1 OVERVIEW

The RFL 93B MO Modem Module contains a receiver and a transmitter. The receiver converts analog signals into digital signals, and the transmitter converts digital signals into analog signals. All the digital signals flow between the RFL 93B CC module and the RFL 93B MO; the RFL 93B MO is also the source of all serial communication clocks. The RFL 93B CC module has two links with the RFL 93B MO; a synchronous serial data link, and a parallel control bus. The serial link sends and receives the relay data, while the control bus monitors and commands operations within the RFL 93B MO.

When the RFL 9300 is initialized, the RFL 93B CC module uses the control bus to configure the RFL 93B MO for CCITT .29 operation at a 7.2-Kbps data rate. The RFL 93B MO uses a modulation scheme known as "QAM" (quadrature amplitude modulation). QAM works by outputting eight tones of different phase and amplitude at a rate of 2400 times per second (2400 baud). Each different tone or "constellation point" (vector) represents a different 3-bit value. Since points are sent at a rate of 2400 per second, the digital data rate is 7200 bits per second (2400 x 3 = 7200).

The RFL 93B MO must establish a reference point before it can start decoding the data. The reference is established when the modem receives a special series of tones called a "training sequence." An internal DSP phase-lock loop latches onto the received signals, and the RX clock is now phase-locked to the remote TX clock. If the modems are not locked onto each other, the phase-lock loop will free-wheel. There will be TX and RX clocks, but they will not be in agreement with the clocks at the remote modem. Under normal conditions, bi-directional communication is established and both local and remote clock pairs are locked together.

The transmit and receive data is valid during positive clock edges. The RFL 93B MO's AGC circuit allows a wide dynamic range of received signals (0 dBm to –39 dBm, as measured into the RFL 93 LC I/O module). If the incoming signal level drops below -43 dBm, the INITALRM control line from the RFL 93B MO to the RFL 93B CC module flags the signal loss.

When the RFL 93B CC module sends the RESET command to the RFL 93B MO through the control bus, the modem's internal registers are cleared to their default values. The RFL 93B CC module follows up the reset with a series of commands written into the "interface" memory located in the modem. Before this is completed, there are no TX or RX clocks coming out of the modem. If there are no clocks coming out of the modem, the problem may be in the control bus between the RFL 93B CC module and the RFL 93B MO module.

14.3.2 HARDWARE DESCRIPTION

The RFL 93B MO Modem Module contains a plug-on modem card, RS-422 interface devices, reset and address latch circuits, multiplex control devices, two voltage regulator circuits, and a solid-state heater for the analog controller. Test points are provided for monitoring the RX and TX serial clocks and data, the voltage regulator outputs, and the RX and TX analog signals from the RFL 93 LC I/O module.

Reset, Address Latch Circuits, And Control Selector. Control bytes are read out of and written into the RFL 93B MO's interface memory by the RFL 93B CC module. The first step for reading or writing to a specific interface memory register is to send the interface memory address. The address on lines D6 through D0 is latched into U9 whenever line A5 is high and the /WR line is strobed. D7 is also latched into U9; this line is used to give a hardware reset to the modem. During normal addressing, this line is sent high to disable resetting. After the address has been latched into U9, the next step would be a read or a write operation from the interface memory. Lines D7 through D0 are also used as the data bus; line A5 is held low while the RD or /WR strobe occurs.

Since there can be two modem modules in a system, input lines SEL0 and SEL1 select which RFL 93B MO module is being accessed. The SEL0 line must be low and the SEL1 line must be high to enable (U5-10) the /WR and RD (U8, U7) strobe lines from reaching the modem interface memory.

Jumpers J2 and J3 determine the polarity of the RD strobe. For devices requiring an RD strobe, a zero-ohm resistor is placed in the J2 position. If this resistor is moved to the J3 position, an /RD strobe is produced.

Voltage Regulator Circuits. The power supply for the RFL 9300 system produces ±15-volt outputs, and the modem on the RFL 93B MO requires ±12 Vdc. U10, R9, and R10 form an equivalent 3-volt precision Zener. The voltage between the anode and the gate of shunt regulator U10 is set at 2.5 volts by U10's internal gap band reference. A divider formed by R9 and R10 results in a fixed 3-volt drop across the cathode and anode of U10. Since this is in series with the +15-volt regulated input from the system power supply, the voltage at the anode of U10 is a regulated +12 volts. A similar circuit is used to reduce the -15-volt system power supply input to -12 volts. This circuit consists of U11, R11, and R12.

Test points TP2 and TP3 monitor the regulator outputs. When the circuits are functioning properly, the voltage at TP2 should be between +11.4 volts and +12.6 volts, and the voltage at TP3 should be between -11.4 volts and -12.6 volts.

RS-422, Serial Clock, And Data Multiplexer Circuits. Several different system configurations are supported by the RFL 93B MO module. The most typical configuration would be a single RFL 93B MO module and a single RFL 93B CC module. However, a system using the hot standby feature or one being used in a three-terminal application would contain two RFL 93B MO modules.

In hot standby, when one modem loses communication, the other modem is switched in and the system continues to function over the alternate modem. In this configuration, both modems send the same transmitted data from the RFL 93B CC module, and the RFL 93B CC module selects which modem it receives clocks and data from.

In the normal configuration (one RFL 93B CC module and one RFL 93B MO module), the TX control line is high and the STANDBY line is low. The TX control line is fixed by a pull-up resistor (RZ1-10) and the STANDBY control line comes from the RFL 93B CC module. The SELECT line on U2-1 is always low, so the data and clock from the "on-board" modem is sent to the RFL 93B CC module. The path for this is from the "on-board" modem into U2's "A" inputs. U2's "Y" outputs are then fed to RS-422 interface U1. U1 controls serial communication with the RFL 93B CC module. The TX control line is always high and the TX data always comes from the RFL 93B CC module in Slot 1. The TX data comes from the RFL 93B CC module at the TX DATA A and TX DATA B inputs (edge connector terminals P1-A10 and P1-C10). U3 converts the balanced RS-422 inputs into unbalanced 5-volt logic at U3-3. The unbalanced 5-volt logic TX DATA is looped out the X TX DATA line (edge connector terminal P1-C22) and back in again at the X TX DATA line input (edge connector terminal P1-A22). This looped connection is on the chassis motherboard. This external connection allows the same hardware to be used in a number of different configurations.

In the hot standby configuration (one RFL 93B CC module and two RFL 93B MO modules), the TX control line is high for both RFL 93B MO modules. This places the same transmit data in both RFL 93B MO modules; the source is the RFL 93B CC module in Slot 1. The X TX DATA on from the modem in Slot 1 (edge connector terminal P1-C22) is fed through the motherboard to edge connector terminal P1-A22 on both modem modules. The STANDBY line on edge connector terminal P1-A15 is controlled by the RFL 93B CC module. If the line is high, the RFL 93B MO module in Slot 2 is selected and the X data and clocks on edge connector terminals P1-C18, P1-C19, and P1-C21 are fed into U2's "B" inputs. The STANDBY input is connected to U2-1, and feeds the "off board modem" data and clocks onto the U2's "Y" outputs.

In the three-terminal configuration (two RFL 93B CC modules and two RFL 93B MO modules), the TX control line and the standby lines are pulled low by connecting lines in the RFL 93B CC module placed in CC Slot 2. When both TX control and the STANDBY lines are low, both RFL 93B MO modules get TX DATA and give RX DATA and clocks from their respective RFL 93B CC modules. The RFL 93B CC module in CC Slot 1 talks only to the RFL 93B MO in Modem Slot 1, and the RFL 93B CC module in CC Slot 2 only talks to the RFL 93B MO module in Modem Slot 2.

Solid-State Heater Circuit. Transistor Q1 is normally biased off if the temperature sensed by thermistor R5 is greater than +20^{O}C. As the temperature falls below +10^{O}C, Q1 turns on and acts like a current source that draws up to 500 mA from the +15-volt supply line. The resultant 7.5 watts is dissipated in resistor R6 and the heat sink for Q1. This heat sink is located below the plug-on modem card, and keeps its ambient temperature above its specified minimum (0^{O}C.) Resistor R27 limits the current through R5 and prevents thermal runaway as the R5's resistance decreases with temperature. Transistor Q2 is normally off unless the -15-volt supply fails. If the -15-volt supply fails, Q2 turns on; this turns off Q1 and prevents the heater from coming on unless all supplies are present.

14.3.3 INITIALIZATION

When the RFL 9300 is initialized, the RFL 93B CC module sends commands over the modem bus. These commands reset the RFL 93B MO and configure it for 7.2-Kbps operation. The RFL 93B MO must receive a "training sequence" from the remote modem before received analog signals can be converted into digital signals. When the RFL 93B MO modem module gets the commands for reset and configuration, the final phase of this operation sends a training sequence to the remote modem. The RFL 93B CC module gives a message to the modem which requests a training sequence from the remote terminal. The remote modem should be receiving messages and the remote RFL 93B CC module decodes the training sequence request signal. The RFL 93B CC module at the remote terminal then commands the remote RFL 93B MO module to send a training sequence and communications are now established in both directions.

The messages sent over the control bus between RFL 93B CC and RFL 93B MO modules are arbitrated by the RFL 93B SV supervisor module. In a three-terminal configuration, two RFL 93B CC modules must talk over the same bus to two RFL 93B MO modules. Contention is avoided because the RFL 93B CC module in Slot 1 sends one step in the initialization sequence, and then gives control over to RFL 93B CC module in Slot 2 by lowering the /COM2 address line. The RFL 93B CC module in Slot 2 then sends the next step in its initialization sequence to the RFL 93B MO module in Slot 2. If too much time has passed, the RFL 93B SV raises all the /COM address lines and the procedure is tried again at the next 0.5-ms system tick from the RFL 93B SV. The result is a 0.5-ms delay between each step in the initialization sequence; this delay gives the RFL 93B MO a chance to react to the control commands (especially the reset command).

The messages sent from the RFL 93B CC module on initialization are as follows:

Step	Address	Bits Set	Bits Cleared	Comments
1	00000000	00000000	00000000	/RESET line low
2	10000000	00000000	00000000	/RESET line high
(If sending training only, start here.)				
3	10100111	00000010	00000000	Set T/2 bit
4	10000111	00000000	10000010	Clear RTS and X CLOCK
5	10000110	00010010	00000000	Set TX for 7.2 Kbps
6	10100110	00010010	00000000	Set RX for 7.2 Kbps
7	10101110	00001000	00000000	RX SET bit ON
8	10001110	00001000	00000000	TX SET bit ON
9	10000111	10000000	00000000	RTS ON (send train)

Table 14-1. Replaceable parts, modem modules for RFL 9300 Charge Comparison System RFL 93B MO (Assembly No. 106355)

Circuit Symbol (Figs. 14-3 & 14-4)	Description	Part Number
	CAPACITORS	
C1-5,7-10,12,13,16-20	Capacitor,X7R ceramic,0.1μF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C11	Capacitor,tantalum,33μF,20%,10V,Kemet T322D336M010AS or equiv.	1007 653
C14,15	Capacitor,tantalum,1μF,20%,35V,Kemet T322B105M035AS or equiv.	1007 496
	RESISTORS	
R1	Resistor,metal film,1.21KΩ,1%,1/4W, Type RN1/4	0410 1296
R2	Resistor,metal film,2.61KΩ,1%,1/4W, Type RN1/4	0410 1328
R3,7,8,22-24	Resistor,metal film,10KΩ,1%,1/4W, Type RN1/4	0410 1384
R4	Resistor,metal film,2.37KΩ,1%,1/4W, Type RN1/4	0410 1324
R5	Thermistor,10K @ 25degC,NL Industries 1D-101 or equiv.	17471
R6	Resistor,composition,6.8Ω,10%,1W,Allen-Bradley GB Series or equiv.	1009 690
R9,12	Resistor,metal film,4.99KΩ,1%,1/4W, Type RN1/4	0410 1355
R10,11,15-20,25	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R13,21	Resistor,metal film,121Ω,1%,1/4W, Type RN1/4	0410 1200
R14	Resistor,metal film,806Ω,1%,1/4W, Type RN1/4	0410 1279
R26	Resistor,metal film,3.01KΩ,1%,1/4W, Type RN1/4	0410 1334
R27	Resistor,metal film,499Ω,1%,1/4W, Type RN1/4	0410 1259
R28,33	Resistor,metal film,604Ω,1%,1/4W, Type RN1/4	0410 1267
R29	Resistor,metal film,17.8KΩ,1%,1/4W, Type RN1/4	0410 1408
R30	Resistor,variable,15-turn cermet,100KΩ,10%,3/4W,Beckman Helipot 89PHR100K or equiv.	47540
R32	Resistor,metal film,4.02KΩ,1%,1/4W, Type RN1/4	0410 1346
RZ1,2	Resistor network,nine 10KΩ 2% resistors,1.25W total,10-pin SIP, Bourns 4310R-101-103 or equiv.	32622
	SEMICONDUCTORS	
CR1,2	Diode,silicon,1N914B or 1N4448	26482
Q1	Transistor,NPN Darlington,60V,2A,Texas Instruments TIP110 or equiv.	41478
Q2	Transistor,NPN,40V,TO-92 case,2N4401	42574
U1	MOS quad differential line driver,16-pin DIP,National Semiconductor DS34C87N or equiv.	0615 395
U2	MOS quad 2-input multiplexer,16-pin DIP,National Semiconductor MM74HC157N or equiv.	0615 171
U3	MOS quad differential line receiver,16-pin DIP,National Semiconductor DS34C86N or equiv.	0615 394

<<table continues on next page>>

Table 14-1 continued. Replaceable parts, modem modules for RFL 9300 Charge Comparison System

Circuit Symbol (Figs. 14-3 & 14-4)	Description	Part Number
	SEMICONDUCTORS - continued.	
U4	MOS quad 2-input NAND gate,14-pin DIP,National Semiconductor MM74HC00N or equiv.	0615 159
U5	MOS 2-to-4 line decoder/demultiplexer,16-pin DIP,Signetics 74HC139N or equiv.	0615 269
U6	MOS quad 2-input Exclusive-OR gate,14-pin DIP,RCA CD74HCT86E or equiv.	0615 390
U7	MOS triple 3-input NOR gate,14-pin DIP,National Semiconductor MM74HC27N or equiv.	0615 250
U8	MOS triple 3-input OR gate,14-pin DIP,National Semiconductor MM74HC4075N or equiv.	0615 181
U9	MOS octal tri-state D-type latch,20-pin DIP,Texas Instruments SN74HC573N or equiv.	0615 308
U10,11	Linear adjustable precision shunt regulator,3-terminal TO-92 case,Motorola TL431ILP or equiv.	0620 320
U12	Linear operational amplifier,JFET input,8-pin DIP,Texas Instruments TL081IP or equiv.	0620 228
	MISCELLANEOUS COMPONENTS	
J1	Shorting bar,single,Molex 90059-0009 or equiv.	98306
J2	Resistor,zero-ohm,1/4-watt size,Corning OMA07 or equiv.	1510 2217
…	Modem card,CCITT V.29,full-duplex (4W)/half-duplex (2W), Rockwell R96DP TR96-D420-011 or equiv.	99450

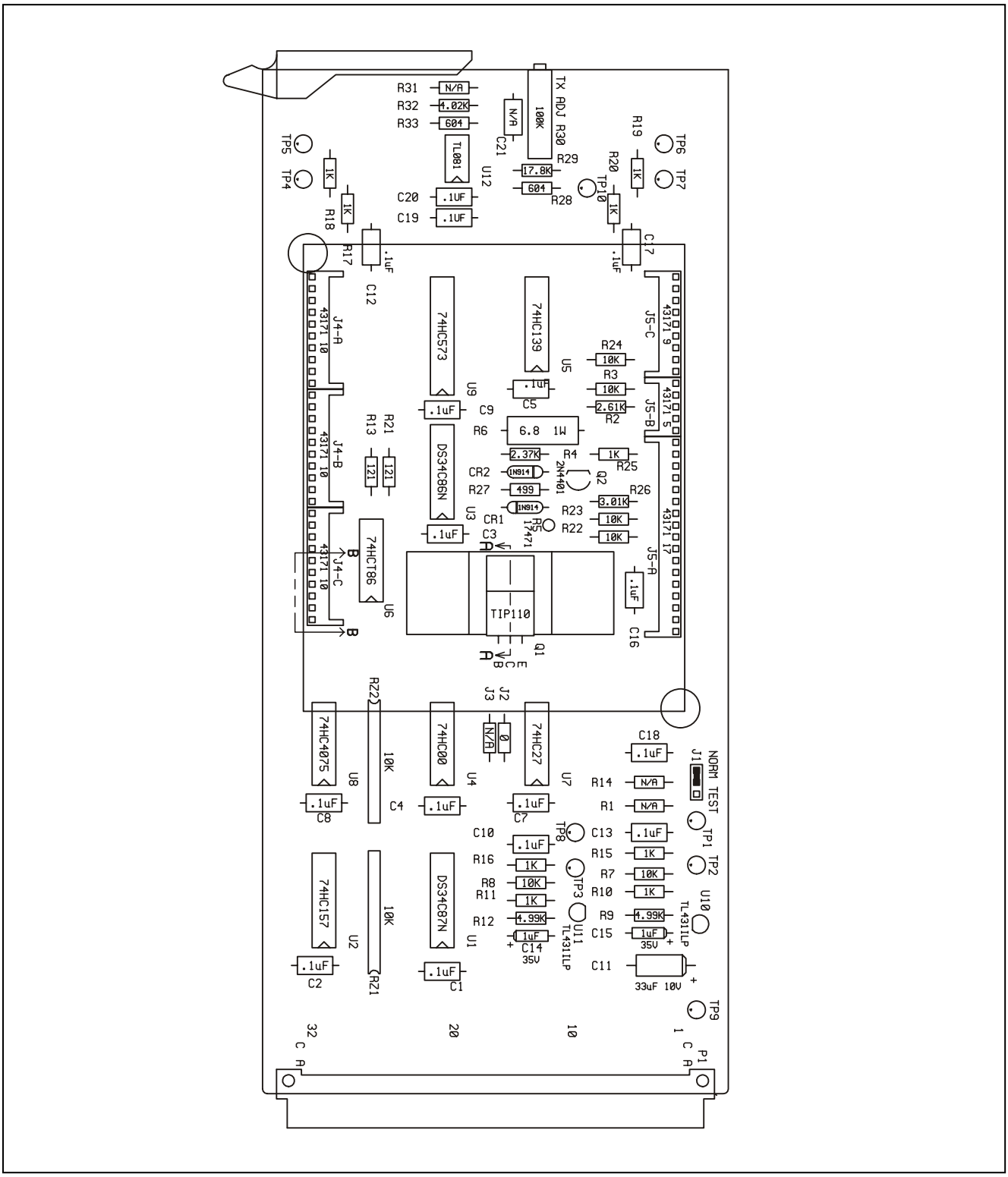


Figure 14-3. Component locator drawing, modem module for RFL 9300 Charge Comparison System

Figure 14-4. Modem module for RFL 9300 Charge Comparison System (Assembly No. 106355; Schematic No. D-103829, Rev. B)

Please see Figure 14-4 in Section 32: Schematics

This page intentionally left blank

SECTION 15: LINE COUPLER I/O MODULE

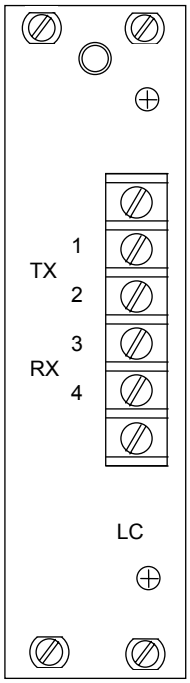


Figure 15-1. RFL 93 LC I/O Line Couple I/O Module

15.1 DESCRIPTION

The RFL 93 LC I/O Line Coupler I/O Module (Fig. 15-1) acts as a barrier between the telephone lines and the RFL 93B MO Modem Module. Its design incorporates isolation transformers (one for incoming signals and one for outgoing signals) which are designed for 600-ohm impedances, which are common in most telephone leased line circuits.

15.2 CONTROLS AND INDICATORS

The RFL 93 LC I/O has no controls or indicators; it is a passive module. There is a four-position terminal block on its rear panel which provides connections to a four-wire telephone line:

4W TX Connect to terminals 1 and 2.

4W RX Connect to terminals 3 and 4.

15.3 THEORY OF OPERATION

Isolation transformers T1 and T2 are specified for a high isolation voltage, so they block any common-mode voltages from reaching the inside of the RFL 9300. (Common-mode voltages are those where both inputs are high relative to ground.) If the potential applied to the inputs is differential, the voltage may appear on the secondary of the transformers and is limited by diodes CR1 through CR4. When a voltage with a fast rise-time is applied to the transformer inputs, the inter-winding capacitance will allow the voltage to appear on the secondary; capacitors C1 through C4 form a "capacitive divider" network which attenuates this voltage on the secondary. Resistor R1 and a resistor of equal value on the RFL 93B MO Modem Module combine to yield an impedance of 600 ohms. The resistance is split between the RFL 93 LC I/O and RFL 93B MO modules to provide some termination impedance even if the modem module is removed from the chassis.

In a field application, high voltages and currents could be induced or coupled onto the wires coming into the RFL 93 LC I/O. To reduce this possibility, the connection between the RFL 93 LC I/O and the telephone interface should be made with twisted pairs which are shielded within the cable. The shield ground must be connected to ground at the RFL 9300 **and** the telephone interface. A solid ground bus connection must be independently provided between the RFL 93 LC I/O card and the telephone interface, or the ground shield could melt from the high currents that could be induced during a fault.

Table 15-1. Replaceable parts, RFL 93 LC I/O Line Coupler I/O Module (Assembly No. 103835)

Circuit Symbol (Figs. 15-3 & 15-4)	Description	Part Number
C1-4	Capacitor,ceramic disc,0.005μF,20%,3kV,Centralab DD30-502 or equiv.	1007 1264
CR1-4	Transient suppressor,5-volt reverse standoff,5W,axial case, General Semiconductor 1N5908 or equiv.	49091
R1	Resistor,metal film,604Ω,1%,1/4W, Type RN1/4	0410 1267
T1,2	Transformer,audio coupling,600Ω impedance,Microtran TH5117 or equiv.	99440

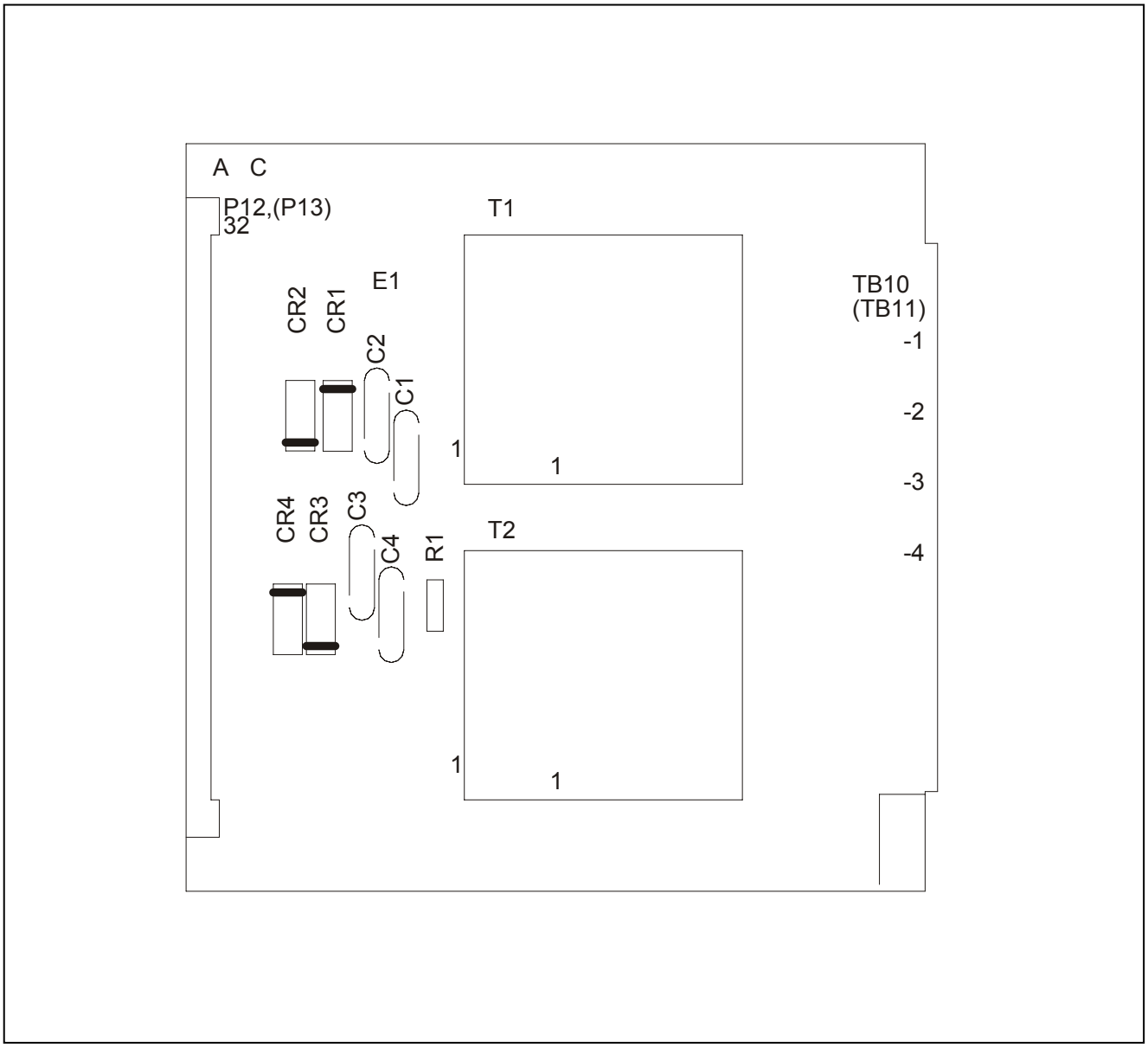


Figure 15-2. Component locator drawing, RFL 93 LC I/O Line Couple I/O Module (Assembly No. 103835; Drawing No. C-103838, Rev. A)

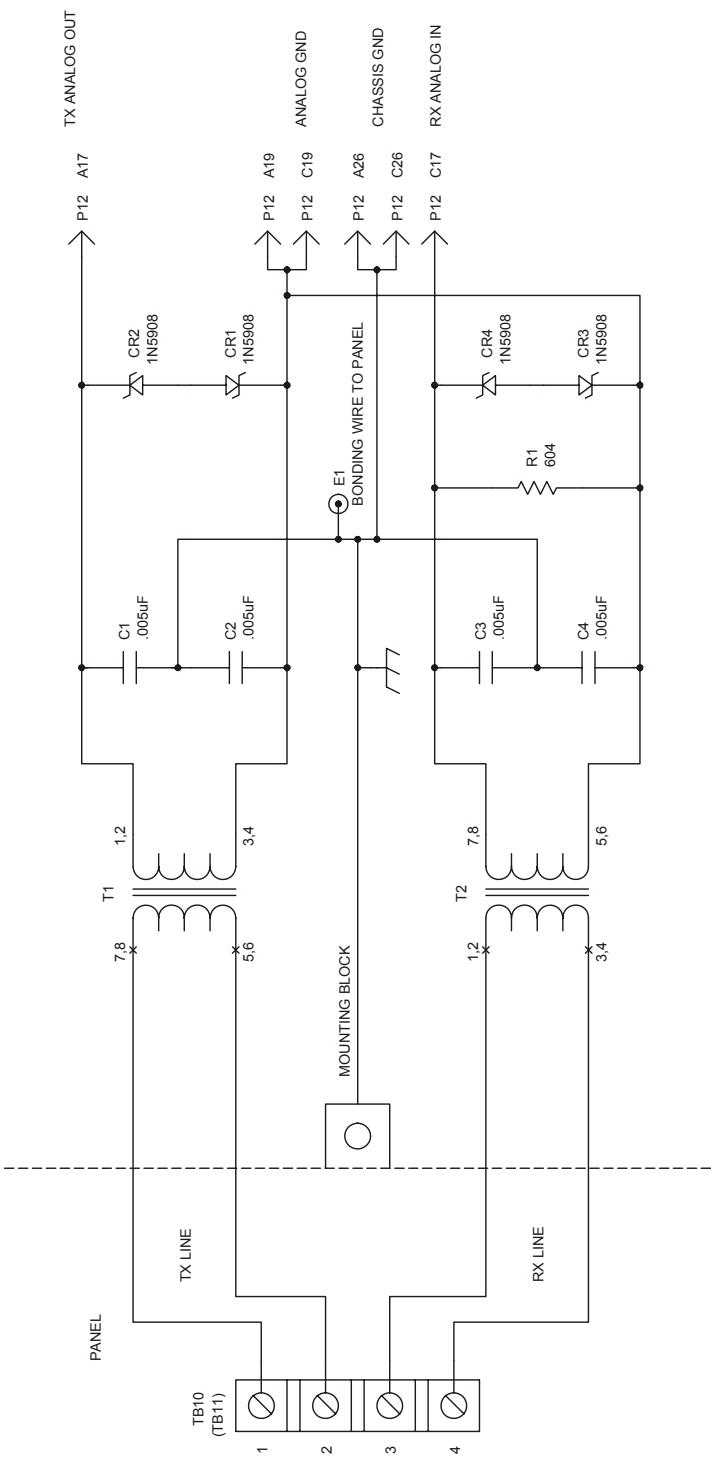


Figure 15-3. RFL 93 LC I/O Line Coupler I/O Module
(Assembly No. 103835; Schematic No. B-103839, Rev. B)

SECTION 16: DIRECT DIGITAL INTERFACE I/O MODULE

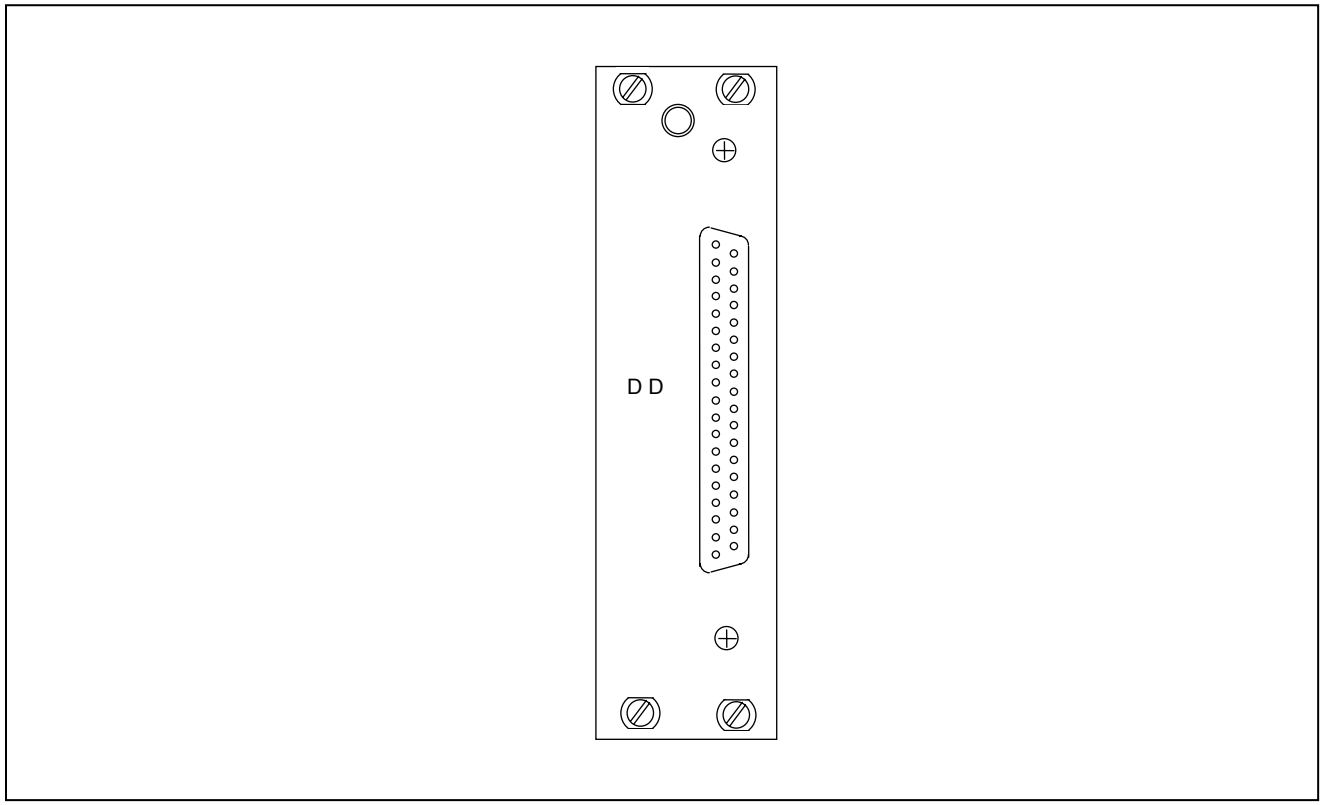


Figure 16-1. RFL 93 DD I/O Direct Digital Interface I/O Module

16.1 DESCRIPTION

The RFL 93 DD I/O Direct Digital Interface I/O Module (Fig. 16-1) allows digital communications equipment (DCE) to be connected directly to the RFL 9300. It serves as an interface between the RFL 9300's motherboard and a rear-panel connector that accepts RS-422 signals. The RFL 93 DD I/O acts only as a buffer, unless the system is configured for hot standby. Multiplex circuits on the RFL 93 DD I/O provide the alternate data paths used during hot standby.

16.2 CONTROLS AND INDICATORS

The RFL 93 DD I/O's circuit board contains two programmable jumpers that prepare it for use, and a rear-panel 37-pin D-subminiature connector. Figure 16-2 shows the jumper locations, and their functions are described below. The jumpers can only be accessed when the RFL 93 DD I/O is out of the chassis or is on a card extender.

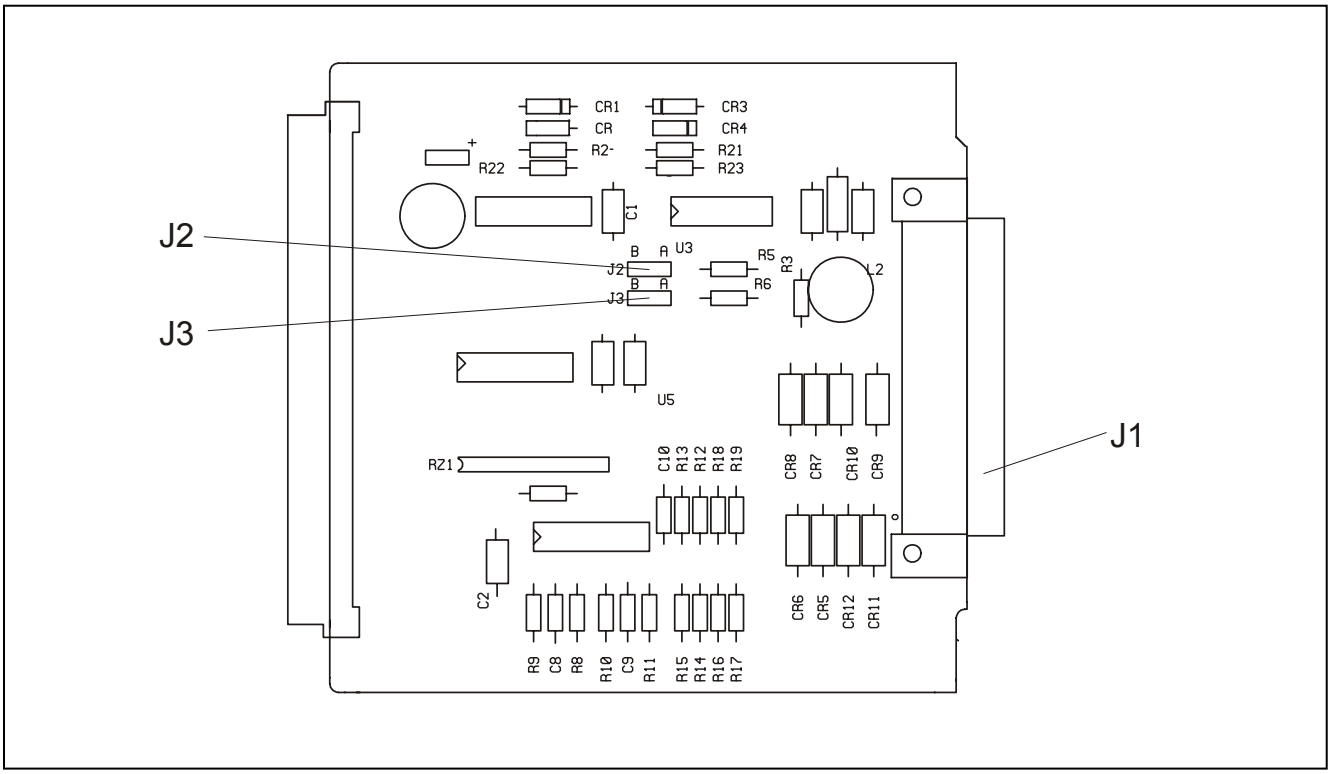


Figure 16-2. Controls and indicators, RFL 93 DD Direct Digital I/O Module

REAR-PANEL CONNECTOR

J1 Rear-panel RS-449 connector; accepts RS-422 signals. The following pins are supported; all other pins are not connected:

Pin No.	RS-449 Signal	CCITT X.21 Signal
5	ST +	Signal Timing A
23	ST -	Signal Timing B
8	RT +	Signal Timing A
26	RT -	Signal Timing B
6	RD +	Receive A
24	RD -	Receive B
7	RT +	Control B (+5V)
25	RT -	Control A (GND)
19	SG	Signal Ground
22	SD -	Transmit B
4	SD +	Transmit A

JUMPERS

J2 J2 sets the polarity of the SEND timing signal. Position A selects inverted polarity, and Position B selects normal polarity. J2's setting will depend on the DCE being connected to the RFL 9300. Try to use the RFL 9300 with J2 in Position B; if the SEND timing is not working properly, move J2 to Position A.

J3 J3 sets the polarity of the RECEIVE timing signal. Position A selects inverted polarity, and Position B selects normal polarity. J3's setting will depend on the DCE being connected to the RFL 9300. Try to use the RFL 9300 with J3 in Position B; if the RECEIVE timing is not working properly, move J3 to Position A.

16.3 THEORY OF OPERATION

RFL 93 DD I/O operation is regulated by two control lines: STANDBY (at edge connector terminal P1-A18) and TX CONTR (terminal P1-C18). When both control lines are low, the serial link paths go straight from the RFL 93B CC module, through the motherboard, and on to rear-panel connector J1. For example, SEND timing comes in on J1-5 and J1-23; if U4-1 is low, the timing pulses are passed to U4-7. The SEND timing signals can be inverted by placing jumper J2 in Position A; Position B selects normal polarity. U4-7 then feeds a logic level to pin 15 of RS-422 translator U1. The signals are again at RS-422 levels.

When the STANDBY line is high, the SEND timing enters the RFL 93 DD I/O as a logic level on edge connector terminal P1-C15. Multiplexer U4 provides a path between U4-6 and U4-7. The source of the logic-level timing signal would be the RFL 93 DD I/O module plugged into rear panel Slot 2. When the RFL 93B CC module decides to switch to Channel 2 in the hot standby configuration, it raises the STANDBY line.

The TX DATA path has a separate control line on edge connector terminal P1-C18, because the same data is transmitted over both channels at all times in hot standby systems.

Jumpers J2 and J3 are both placed in Position B for normal operation. The RFL 93B CC module expects that the received data is stable when the RECEIVE timing pulses are going from low to high (positive clock edge). If the edges are not correct and the data is changing when the positive clock edge is received, J3 must be changed to Position A. The RFL 93B CC module will produce stable TX DATA during the positive SEND timing clock edge; J2 should be in Position B to avoid confusion.

J1-33 is the external /ALARM input. If not connected, pull-up resistor RZ1 defaults the /ALARM to the ALARM OFF condition. The alarm is turned on by connecting J1-33 to J1-19 or J1-25 (signal ground).

Table 16-1. Replaceable parts, RFL 93 DD I/O Direct Digital Interface I/O Module (Assembly No. 103830-1)

Circuit Symbol (Figs. 16-3 & 16-4)	Description	Part Number
C1-4,6	Capacitor,X7R ceramic,0.1uF,10%,50V,AVX SA305C104KAA or equiv.	0130 51041
C5	Capacitor,tantalum,1uF,20%,35V,Kemet T322B105M035AS or equiv.	1007 496
C7	Capacitor,X7R ceramic,0.01uF,10%,50V,AVX SA105C103KAA or equiv.	0130 51031
C8-10	Capacitor, ceramic 220pF, 10%,100V	0125 12211
CR1-4	Diode, Shottky, 1A, 20V, 1N5817	30150
CR5-12	Suppressor, voltage, P6KE9.1CA	103340
J2,3	Shorting bar,single,Molex 90059-0009 or equiv.	98306
L1,2	Inductor,powerline,10mH,Renco RL-1283-10 or equiv.	30063
R1	Resistor,metal film,100Ω,1%,1/2W, Type RN1/2	0410 2192
R3	Resistor,metal film,1KΩ,1%,1/4W, Type RN1/4	0410 1288
R5,6	Resistor,metal film,4.99KΩ,1%,1/4W, Type RN1/4	0410 1355
R7	Resistor,metal film,121Ω,1%,1/4W, Type RN1/4	0410 1200
R8-13	Resistor, metal film, 499Ω, 1%,1/4W, Type RN 1/4	0410 1259
R20-23	Resistor, metal film, 15Ω, 1%, 1/4W	1510 1023
RZ1	Resistor network,nine 10KΩ 2% resistors,1.25W total,10-pin SIP,Bourns 4310R-101-103 or equiv.	32622
U1	MOS quad differential line driver,16-pin DIP,National Semiconductor DS34C87N or equiv.	0615 395
U2	MOS quad differential line receiver,16-pin DIP,National Semiconductor DS34C86N or equiv.	0615 394
U3	MOS quad 2-input NAND gate,14-pin DIP,National Semiconductor MM74HC00N or equiv.	0615 159
U4	MOS quad 2-input multiplexer,16-pin DIP,National Semiconductor MM74HC157N or equiv.	0615 171
U5	MOS quad 2-input Exclusive-OR gate,14-pin DIP,RCA CD74HCT86E or equiv.	0615 390

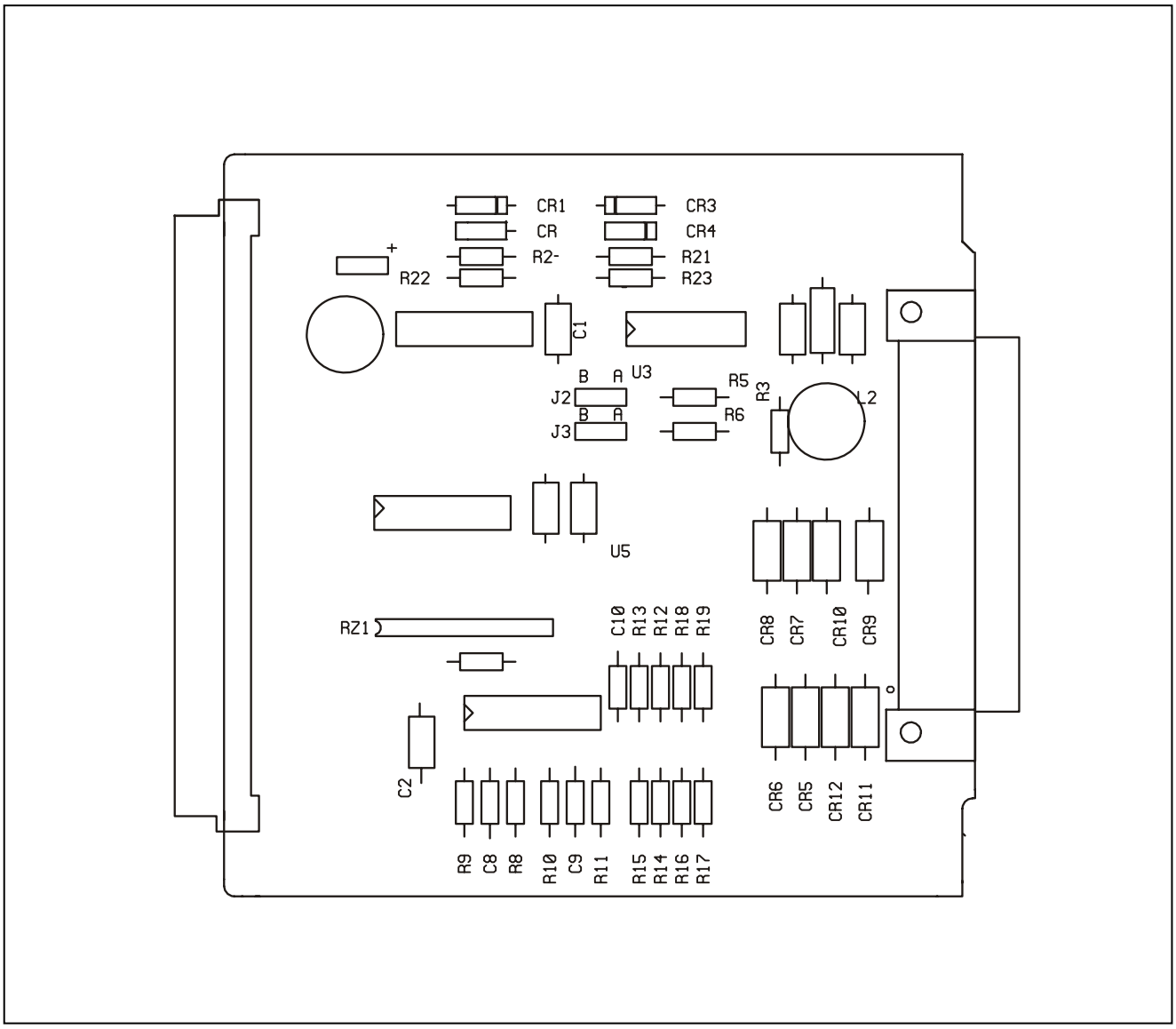


Figure 16-3. Component locator drawing, RFL 93 DD I/O Direct Digital I/O Module (Assembly No. 103830-1; Drawing No. C-103833-1, Rev. A)

Figure 16-4. RFL 93 DD I/O Direct Digital I/O Module (Assembly No. 103830-1; Schematic No. D-103834-1, Rev. A)

Please see Figure 16-4, in Section 32: Schematics

SECTION 17: SINGLE WIDTH FIBER OPTIC TRANSCEIVER MODULE

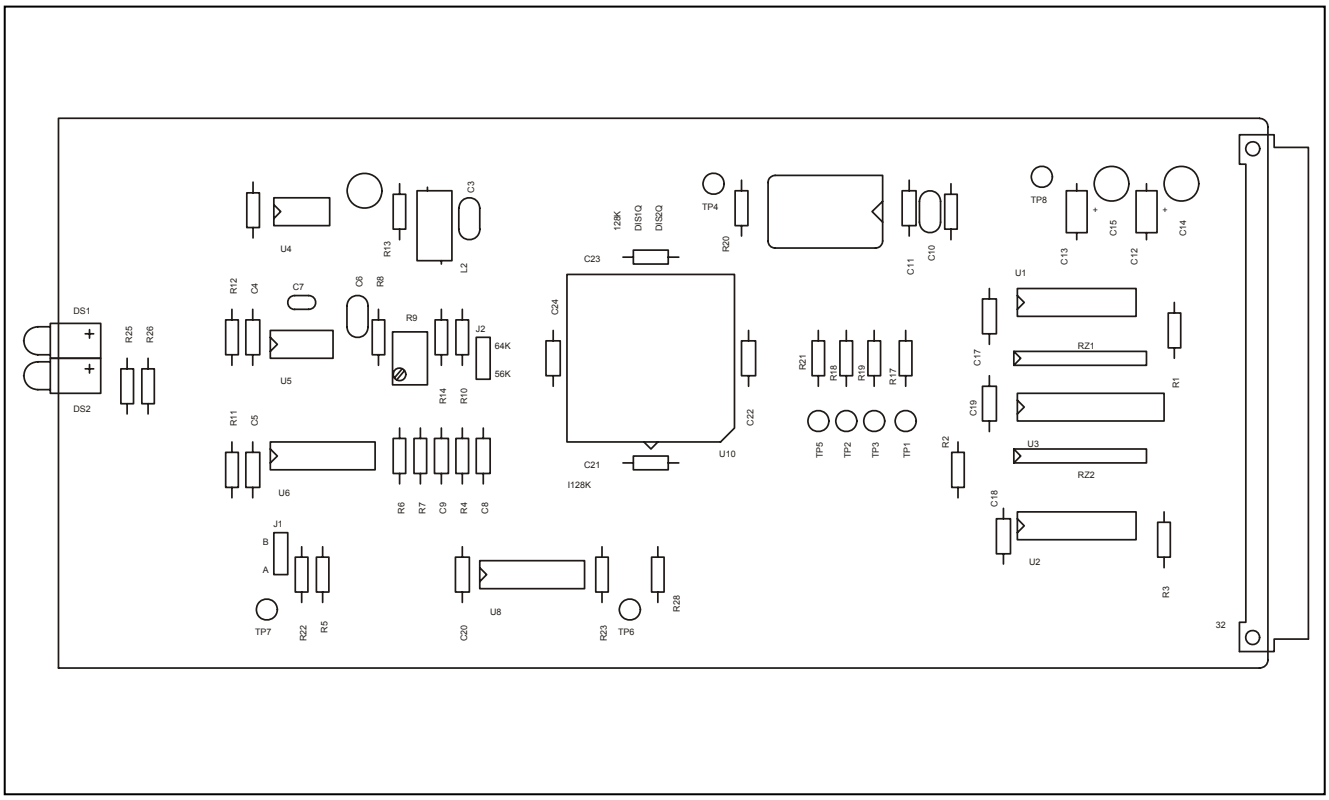


Figure 17-1. RFL 93 B FT/FR Single width fiber optic transceiver module

17.1 INTRODUCTION

The RFL 93B FT/FR single width fiber optic transceiver module (Figure 17-1) consists of a fiber optic transmitter and a fiber optic receiver housed in a single 1.4 inch wide module. For this reason it is referred to as a single width transceiver module.

The transmitter section accepts signals generated by the RFL 93B CC Communications Controller module (Section 13) and conditions them for optic transmission. A transmitter output monitor on the module will activate an alarm if transmitter power is lost.

The receiver section accepts inputs from a fiber optic I/O module (Section 18) and converts them back into RS-422 signals that can be processed by the RFL 93B CC Communications Controller module (Section 13).

17.2 DESCRIPTION

The RFL 93B FT/FR single width fiber optic transceiver module is shown in Figure 17-1. The module occupies one dedicated module space in the front of the RFL 9300 chassis, and is used with a fiber optic I/O module that is located at the rear of the chassis. The fiber optic I/O module selected for use with the RFL 93B FT/FR will determine the fiber optic cable interface characteristics, such as wavelength, output level, and mating connector type. All of the currently available single width fiber optic I/O modules are described in Section 18 of this manual.

17.3 SPECIFICATIONS

As of the date this manual was published, the following specifications apply to all RFL 93B FT/FR single width fiber optic transceiver modules, except where indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Power Requirements (from chassis supply):

+5-Volt Supply: 120 mA
+15-Volt Supply: 10 mA

Input Signals:

P1-C15	TXCONTR: 5V CMOS Controls one data selector inside the Actel. Logic 0 selects internal TX Data. Logic 1 selects external TX Data.
P1-A15	STANDBY: 5V CMOS Controls two data selectors inside the Actel. Logic 0 selects internal TX Clock and RX Data. Logic 1 selects external TX Clock and RX Data.
P1-C18	TXCLK_IN: 5V CMOS External TX Clock input.
P1-C21	RXD_IN: 5V CMOS External RX Data input.
P1-A22	TXD_IN: 5V CMOS External TX Data input.
P1-A10	TXDATA_A:
P1-C10	TXDATA_B: RS422 TX Data input.
P1-A28	RECEIVE_DATA: 5V CMOS Modulated RX Data from Fiber Head.
P1-A31	TX_ALARM: 5V CMOS Alarm signal from Fiber Head TX section. Logic 1 TX is OK. Logic 0, TX is malfunctioning

Output Signals:

P1-A18	TXCLKOUT: 5V CMOS Internal 56K or 64K TX Clock output.
P1-A21	RXD_OUT: 5V CMOS Internal modulated RX Data output.
P1-C22	TX_DATA: 5V CMOS Internal modulated TX Data output.
P1-C29	REC_CLOCK: 5V CMOS Logic 1, Receive clock is recovered and locked. Logic 0, Receive clock cannot be recovered.
P1-A12 P1-C12	RXDATA_A: RXDATA_B: RS422 Receive data output.
P1-C13 P1-A13	RXCLK_A: RXCLK_B: RS422 Receive clock output.
P1-C11 P1-A11	TXCLK_A: TXCLK_B: RS422 Transmit clock output.
P1-C24	SEND_DATA: 5V CMOS Modulated TX data output to fiber head

Temperature:

Storage: -40^{O}C to +75^{O}C (-40^{OF} to +167^{O}F).
Operating: -30^{O}C to +65^{O}C (-22^{O}F to +149^{O}F).

Relative Humidity: 95 percent, non-condensing.

Dimensions:

Width (including panel) 1.4 inches (3.6 cm)
Height (including panel) 5 inches (12.7 cm)
Depth (behind panel) 9 inches (22.9 cm)

17.4 CONTROLS AND INDICATORS

Figure 17-2 shows the location of all controls and indicators on the RFL 93B FT/FR single width fiber optic transceiver module. These controls and indicators are described below. Those described as front panel indicators are visible to the user with the RFL 93B FT/FR installed in the RFL 9300 chassis; all others are only accessible when the RFL 93B FT/FR is removed from the chassis or is on a card extender.

Front Panel LED Indicators

DS1 (Red LED)	TX ALARM when illuminated; Indicates that the Emitter on the FT/FR is damaged or not transmitting data.
DS2 (Green LED)	TX ON Indicates normal Emitter operation on the FT/FR I/O module.

Test Turrets

TP1	Monitoring point for TX_CLK
TP2	Monitoring point for RCVD_DAT
TP3	Monitoring point for RCVD_CLK
TP4	Monitoring point for 3.584 MHz clock
TP5	Monitoring point for VCO_2
TP6	Monitoring point for REC_LOCK
TP7	Monitoring point for PH_DET
TP8	Ground

Jumpers

J1	Phase detector select (used during factory alignment)
J2	56K/64K clock select

Controls

R9	Potentiometer (used to adjust phase detector during factory alignment)

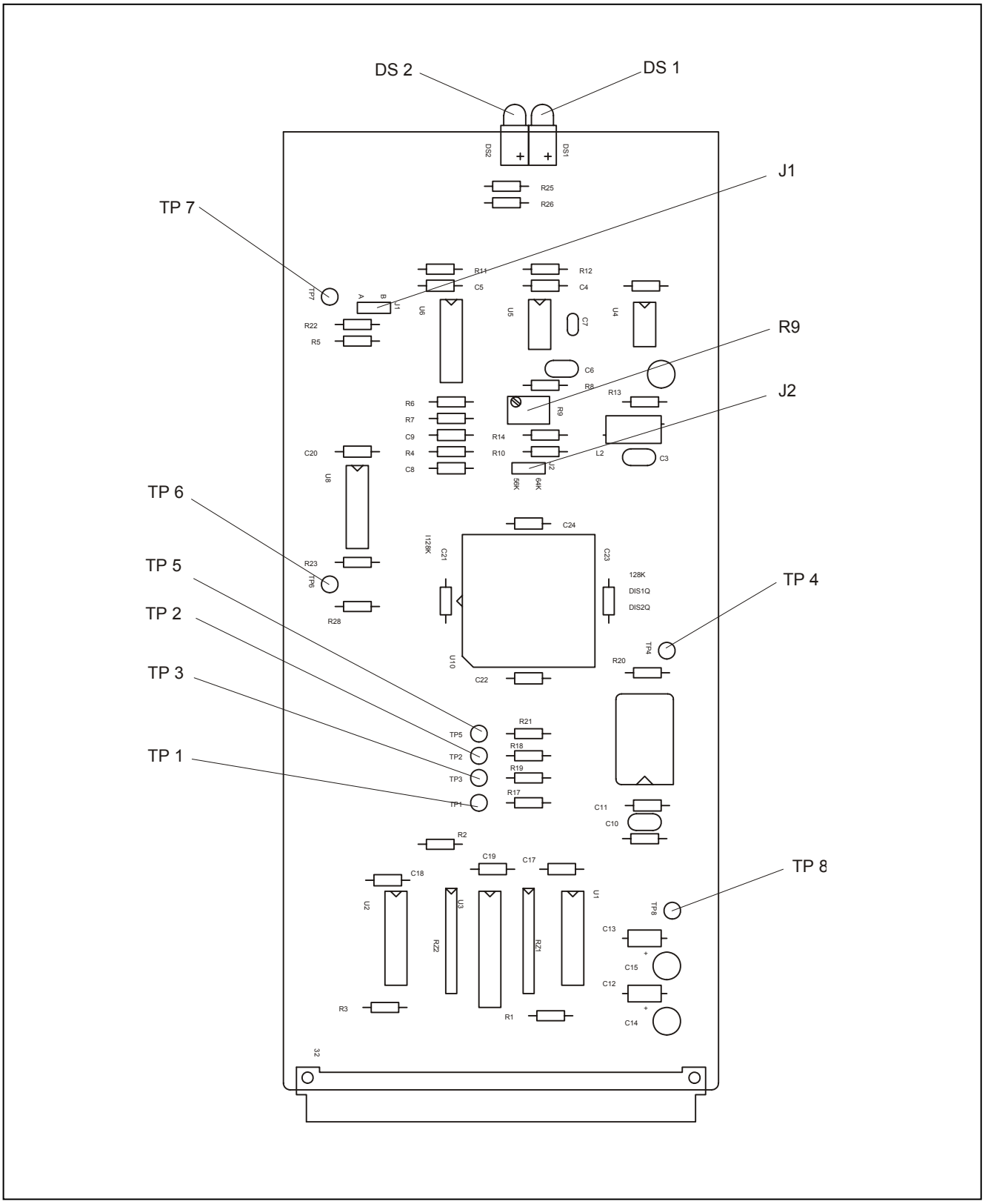


Figure 17-2. Controls and indicators, RFL 93B FT/FR single width fiber optic transceiver mode

17.5 THEORY OF OPERATION

17.5.1 OVERVIEW

The RFL 93B FT/FR Single Width Fiber Optic Transceiver module converts a single RS-422 data input into an FSK type signal, suitable for transmission over a fiber optic cable. The receive portion of the module accepts FSK signals from the fiber optic receiver and converts them back to RS-422 signals. The module consists of RS-422 drivers and receivers, buffers, a crystal oscillator, a voltage reference, a VF converter and an FPGA. A block diagram of the module is shown in Figure 17-3, and a schematic diagram is shown in Figure 17-4.

17.5.2 TRANSMIT DESCRIPTION

The crystal oscillator U7 provides a 3.584 mHz clock to pin 43 “OSC” input of the FPGA 1010B. The signal is divided down to 128 kHz for 64Kbit operation, and 112 kHz for 56Kbit operation. Jumper J2 enables the user to make the selection. Since the 64Kbit and 56Kbit operation is similar, only the 64Kbit operation will be discussed. The 128Khz signal becomes the clock input for a pair of D flip-flops connected to provide 64K and 32K timing signals. The 64K signal is brought out to become the TX_CLK on U1 pin 9, converted to RS-422, and will be the local clock source for TX_DATA originating from the 93B CC module.

The FPGA 64K and 128K signals are routed to an internal data selector that selects 64K when TX_DATA is a logic 1, and 128K when TX_DATA is a logic 0. A group of four internal D flip-flops are clocked by the 128K signal while the 32K inverted and 32K non-inverted signals control their PRESET inputs. The two signals created are DIS1Q and DIS2Q. These two signals control a group of four internal AND gates that route the output of the data selector to the “SEND_DAT” FPGA 1010B pin 36.

17.5.3 RECEIVE DESCRIPTION

The RECEIVE_DATA signal from the LIB (Light Interface Board) enters the board and is buffered by U3. This is a composite TTL signal containing modulated data an RX clock. The signal is demodulated and the clock is recovered by the following PLL (Phase Lock Loop) circuit. The circuit is composed of individual integrated circuits in order to achieve the stability required for this application.

Exclusive OR gate U6 section A is the phase detector, and R4, R6, R7, C8 and C9 filter the phase detector output. V/F converter and associated components form the VCO. A precision voltage reference U4 provides bias and VCC to the phase detector. Internal D flip-flops and logic are located in the FPGA U10. The demodulated data, RCVD_DAT and recovered clock, RCVD_CLK signals are routed from the FPGA U10 to the RS-422 transmitter U1.

17.5.4 RECEIVE CLOCK ERROR DETECTION

The FPGA, U10 contains logic to detect problems with the recovered clock signal. In the event the recovered clock signal is lost for more than 50 microseconds the CS_DET output will pulse high for 4 milliseconds. If the clock has returned prior to the end of the 4 millisecond period CS_DET will go low. If the clock is still inactive at the end of the 4 millisecond time period CS_DET will remain high until the clock returns. This circuit will also detect a slipped clock cycle by comparing the recovered clock to the local crystal generated Tx clock. Although they are asynchronous, the two clocks have alternating clock edges. If either clock has two rising edges without a rising transition of the other, CS_DET will go high for 4 milliseconds. The CS_DET signal is inverted and buffered by U8 and is routed to the Communication Controller module.

17.5.5 HOT STANDBY OPERATION

Hot Standby operation consists of one Communications Controller card and two Fiber Optic transceivers. This mode of operation provides for redundant fiber paths. The logic for switching between primary and secondary fiber paths is performed in the FPGA, U10. A control signal for switching the fiber paths originates from CC#1 and signals are routed via the backplane. See Figure 17-4 for the signal routing diagram.

RS-422 TX Data from CC#1 is routed to the primary FT/FR where it is converted to TTL. The TXCONTR signal is a logic one. This signal is pulled to a logic zero when CC#2 is installed. In hot standby mode CC#2 is not used. A logic one on TXCONTR steers TX_DATA in the primary FT/FR to the modulator and the primary FT/FR I/O. TX_DATA is routed via the backplane to the secondary FT/FR where the identical method is used to steer TX_DATA to the secondary FT/FR I/O. We now have redundant TX_DATA being transmitted over two separate cables.

On the receive side, when the secondary FT/FR module is installed, a grounded pin on the module will pull the TEST input on CC#1 low, signaling Hot Standby mode. In this mode the STANDBY control line will become active. When the line is low the primary FT/FR is selected and when it is high the secondary FT/FR is selected. The receive data from the secondary FT/FR is routed to the primary FT/FR via the backplane. The switching of receive data, primary or secondary, is done on the primary FT/FR. Refer to the Fiber Optic signal routing block diagram.

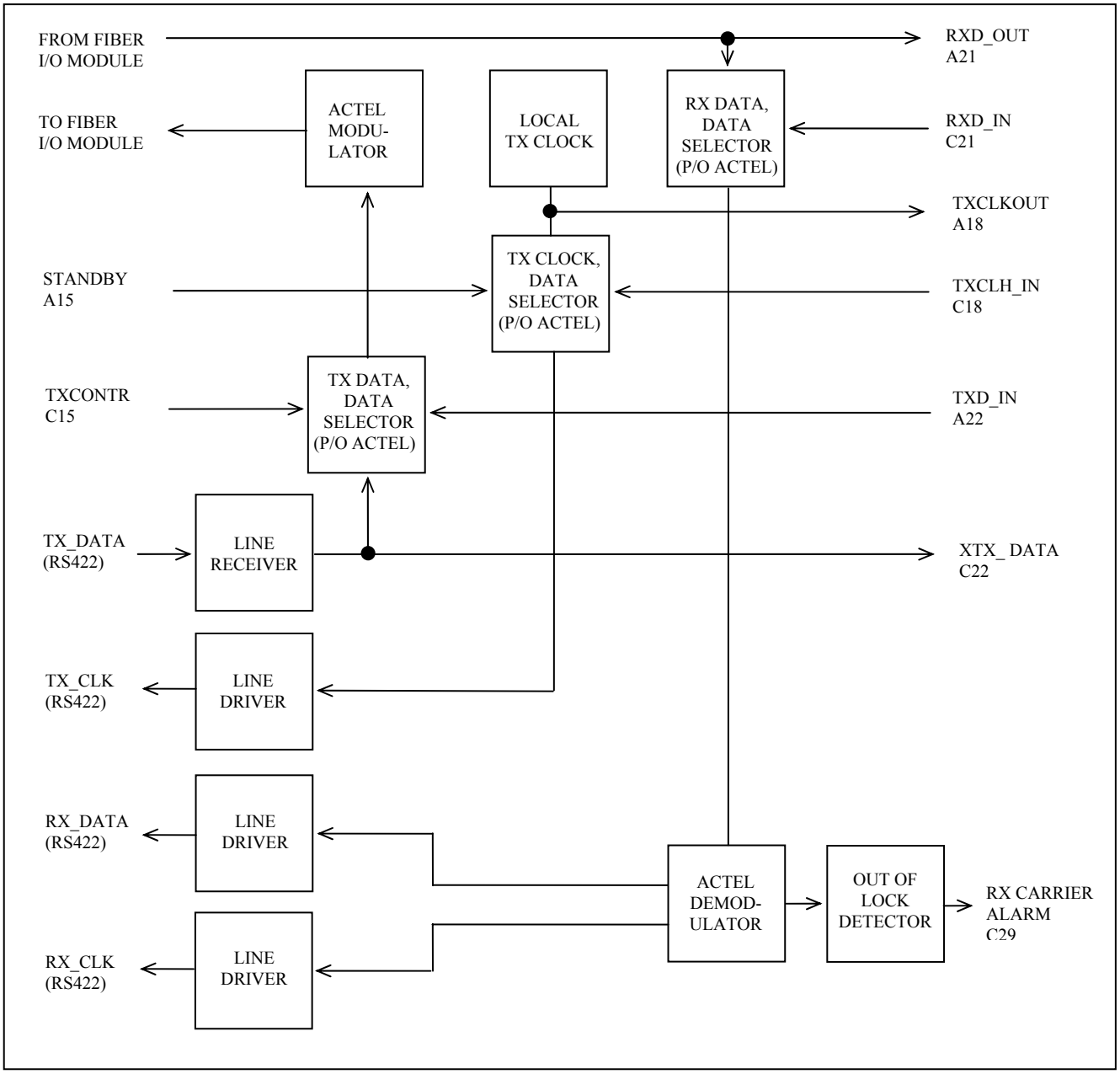


Figure 17-3. Block diagram, RFL 93B FT/FR single width fiber optic transceiver module

Figure 17-4. RFL 9300 Fiber Optics Hot Standby Signal Routing Diagram

Please see Figure 17-4, in Section 32: Schematics

Table 17-1. Replaceable parts, RFL 93B FT/FR single width fiber optic transceiver module. (Assembly No. 106360)

Circuit Symbol (Figs. 17-5 & 17-6)	Description	Part Number
	CAPACITORS	
C1, 4, 5, 11, 17-24	Capacitor, ceramic, 0.1μF, 10%, 50V	0130 51041
C2	Capacitor, tantalum, 10μF, 10%, 20V	1007 1465
C3, 6, 10	Capacitor, ceramic, dipped, 0.01μF, 5%, 100V	1007 1645
C7	Capacitor, ceramic, dipped, 330pF, 10%, 100V	1007 1672
C8	Capacitor, ceramic, 560pF, 5%, 100V	0125 15615
C9	Capacitor, ceramic, 0.0056μF, 5%, 100V	0125 15625
C12, 13	Capacitor, ceramic, 1μF, 20%, 50V	0135 51052
C14	Capacitor, electrolytic, 100μF, 20%, 10V	1007 1740
C15	Capacitor, electrolytic, 47μF, 20%, 35V	1007 1578
	RESISTORS	
R1, 3	Resistor, metal film, precision, 150Ω, 1%, 1/4W	0410 1209
R2, 10	Resistor, metal film, precision, 10K, 1%, 1/4W	0410 1384
R4	Resistor, metal film, precision, 8.45K, 1%, 1/4W	0410 1377
R5	Resistor, metal film, precision, 100K, 1%, 1/4W	0410 1480
R6	Resistor, metal film, precision, 78.7K, 1%, 1/4W	0410 1470
R7	Resistor, metal film, precision, 182K, 1%, 1/4W	0410 1505
R8	Resistor, metal film, precision, 4.02K, 1%, 1/4W	0410 1346
R9	Resistor, variable, metal film, 2K, 10%, 1/2W	90392
R11	Resistor, metal film, precision, 2K, 1%, 1/4W	0410 1317
R12	Resistor, metal film, precision, 10Ω, 1%, 1/4W	1510 1015
R13	Resistor, fixed carbon, 2.7Ω, 5%, 1/4W	1009 900
R14	Resistor, metal film, precision, 681Ω, 1%, 1/4W	0410 1272
R17-23	Resistor, metal film, precision, 1K, 1%, 1/4W	0410 1288
R25, 26	Resistor, metal film, precision, 499Ω, 1%, 1/4W	0410 1259
R28	Resistor, metal film, precision, 47.5K, 1%, 1/4W	0410 1449
RZ1,2	Resistor network, 10K, 8R/PKG, SIP	95571

Table 17-1 continued. Replaceable parts, RFL 93B FT/FR single width fiber optic transceiver module. (Assembly No. 106360)

Circuit Symbol (Figs. 17-5 & 17-6)	Description	Part Number
	SEMICONDUCTORS	
U1	Integrated circuit, MOS, quad differential line driver	0615 395
U2	Integrated circuit, MOS, quad differential line receiver	0615 394
U3	Integrated circuit, MOS, tri-state octal buffer	0615 176
U4	Integrated circuit, linear voltage reference, +5V	0620 308
U5	Integrated circuit, converter, voltage to frequency	0625 34
U6	Integrated circuit, MOS, quad, 2 input exclusive OR gate	0615 268
U8	Integrated circuit, MOS, quad, 2 input Schmitt Trigger NAND gate	0615 306
U10	Integrated Circuit, MOS, field programmable gate array	0615 422
	MISCELLANEOUS COMPONENTS	
DS1	Optoelectric device, LED, red	99294
DS2	Optoelectric device, LED, green	32567
J1, 2	Jumper, connector, programmable	98306
L1	Inductor, molded, RF, 100μH, 10%	32505 1
L2	Bead, ferrite, shield	103344
P1	Connector, JK male, 64 contact, DIN	98457
TP1-8	Test point, terminal, orange	98441 3
U7	Crystal, hybrid, clock oscillator, 3.584 MHz	103347

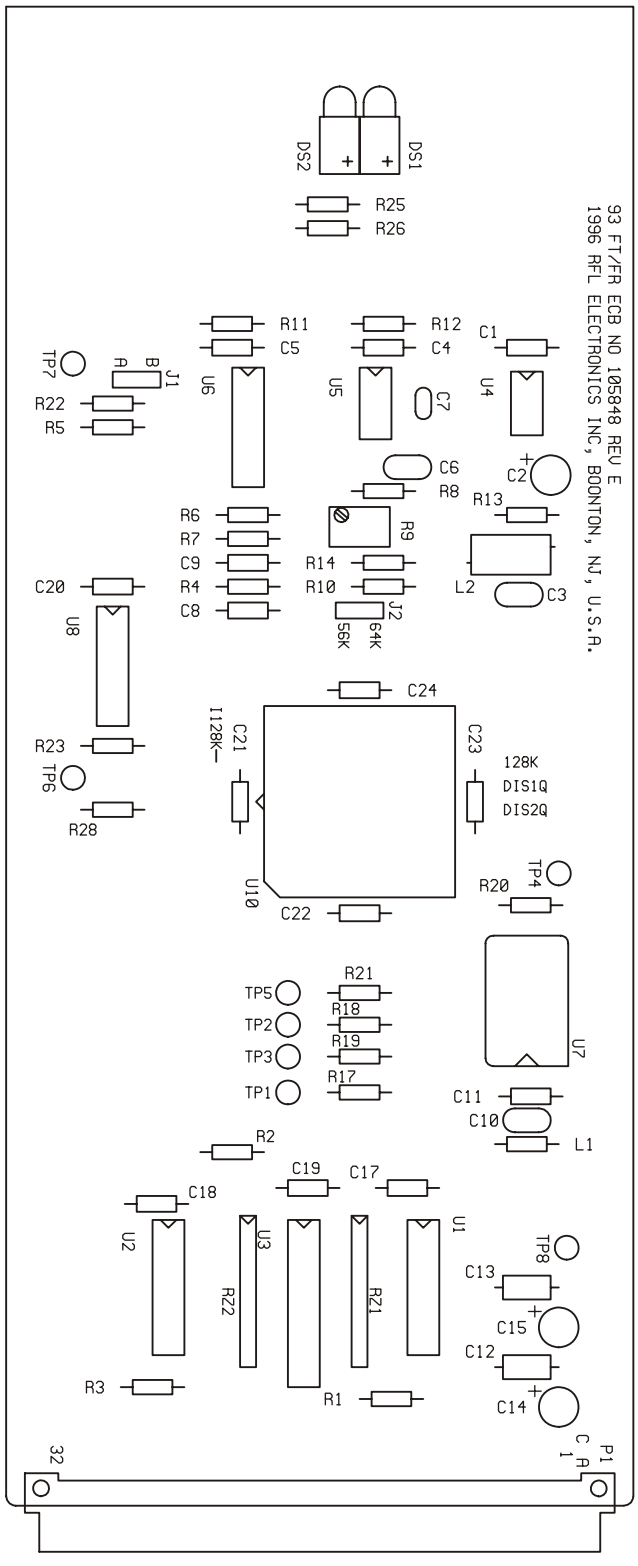


Figure 17-5. Component locator drawing, RFL 93B FT/FR single width fiber optic transceiver module (Assembly No. 106360)

Figure 17-6. RFL 93 FT/FR Singlewidth Fiber Optic Transceiver Module (Assembly No. 106360; Schematic No. D-105849, Rev. B)

Please see Figure 17-6, in Section 32: Schematics

SECTION 18: SINGLE WIDTH FIBER OPTIC I/O MODULE

WARNING

YOUR RFL 9300 TERMINAL MAY BE EQUIPPED WITH FIBER OPTIC INPUT/OUTPUT MODULES THAT HAVE FIBER OPTIC EMITTER HEADS. FIBER OPTIC EMITTER HEADS USE A LASER LIGHT SOURCE THAT PRODUCE INVISIBLE RADIATION. FIBER OPTIC COMMUNICATION SYSTEMS ARE INHERENTLY SAFE IN NORMAL OPERATION BECAUSE ALL RADIATION IS CONTAINED IN THE SYSTEM. IT IS POSSIBLE DURING MAINTENANCE TO EXPOSE THE RADIATION BY REMOVING OR BREAKING THE FIBER. STARING DIRECTLY INTO THE LIGHT BEAM MAY RESULT IN PERMANENT EYE DAMAGE AND/OR BLINDNESS. NEVER LOOK DIRECTLY INTO THE LIGHT BEAM AND BE CAREFUL NOT TO SHINE THE LIGHT AGAINST ANY REFLECTIVE SURFACE.

THE LASER SOURCE IS A CLASS I LASER PRODUCT WHICH COMPLIES WITH APPLICABLE FDA, OSHA AND ANSI STANDARDS.

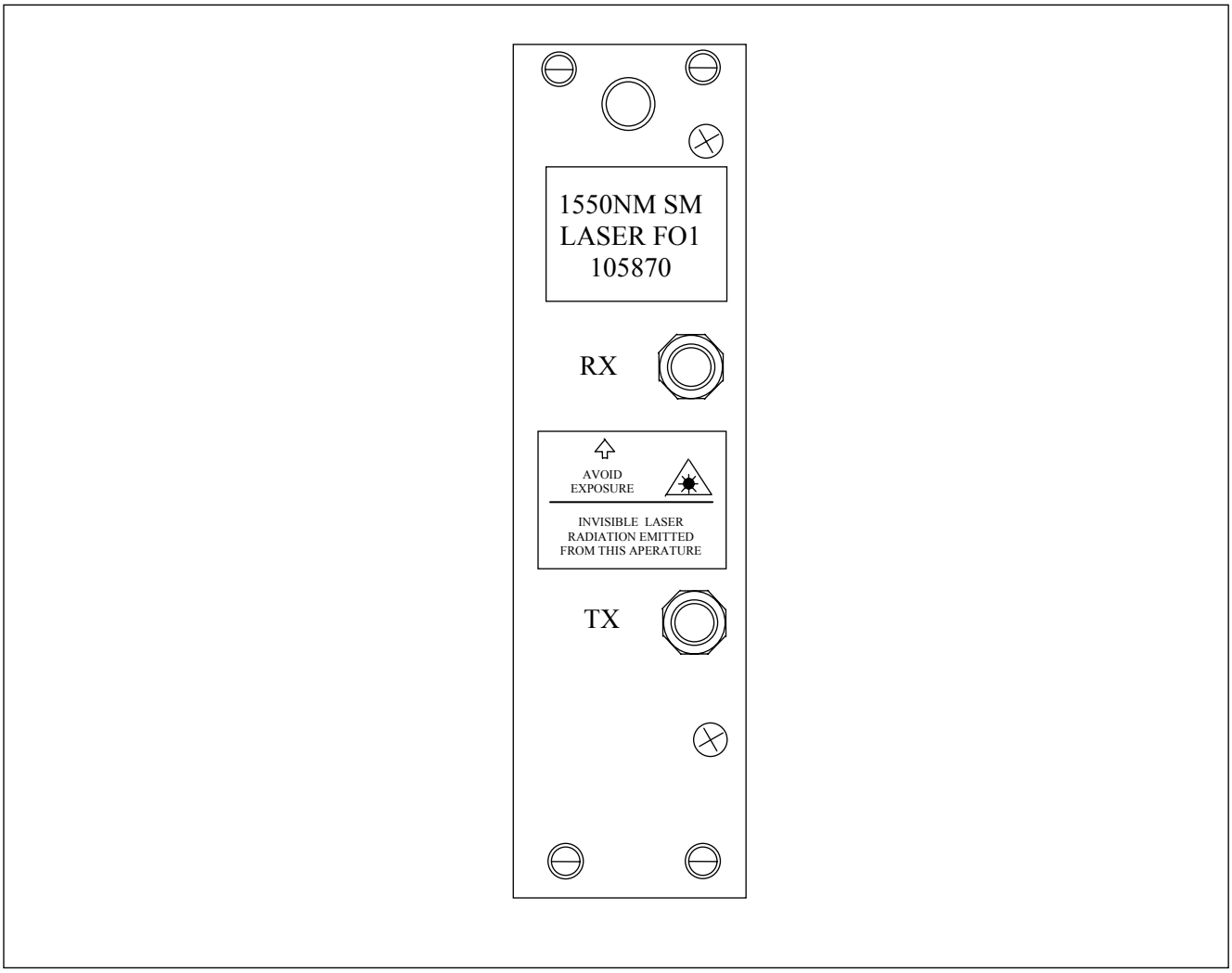


Figure 18-1. Typical RFL 93 FT/FR single width fiber optic I/O module

18.1 INTRODUCTION

The RFL 93 FT/FR single width fiber optic I/O module consists of an input section (detector) and an output section (emitter) housed in a single 1.4 inch wide module. For this reason it is referred to as a single width fiber optic I/O module. A typical single width fiber optic I/O module is shown in Figure 18-1.

Each 93 FT/FR single width fiber optic I/O module is mounted at the rear of the chassis and uses a single width fiber optic transceiver module (Section 17) mounted at the front of the chassis. Single width fiber optic I/O modules serve as the interface between the fiber optic transceiver module and the fiber optic cables. This allows the fiber optic modules to be removed from the chassis without having to draw the fiber through the chassis. A variety of single width fiber optic I/O modules are available, allowing the RFL 9300 to be used with many different types of fiber optic cables.

18.2 DESCRIPTION

Table 18-1 summarizes the differences between the various single width fiber optic I/O modules. A more detailed description of these modules can be found below.

Table 18-1. Differences between Single Width Fiber Optic I/O Modules

Model Number	Assembly Number	Type	Wavelength/Mode	Connector	Peak Light Level *	Average Light Level *
RFL 93FT/FR I/O-8M	105850	LED Emitter/Detector	850-nm Multimode	ST	-10dBm	-13dBm
RFL 93FT/FR I/O-13M	105855	LED Emitter/Detector	1300-nm Multimode	ST	-10dBm	-13dBm
RFL 93FT/FR I/O-13S	105860	LED Emitter/Detector	1300-nm Singlemode	ST	-14dBm	-17dBm
RFL 93FT/FR I/O-13SL	105865	LASER Emitter/Detector	1300-nm Singlemode	ST	+3dBm	0dBm
RFL 93FT/FR I/O-15SL	105870	LASER Emitter/Detector	1550-nm Singlemode	ST	+2dBm	-3dBm

* Light levels are emitter outputs for fiber optic I/O modules, and detector inputs for fiber optic I/O modules.

18.3 SPECIFICATIONS

As of the date this manual was published, the following specifications apply to all RFL 9300 single width fiber optic I/O modules, except where indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Input Power Requirements (from chassis supply):

RFL 93 FT/FR I/O-8M:
- +5-Volt Supply: 120 mA
- +15-Volt Supply: 80 mA
- -15-Volt Supply: 80 mA

RFL 93 FT/FR I/O-13M and RFL 93 FT/FR I/O-13S:
- +5-Volt Supply: 130 mA
- +15-Volt Supply: 50 mA
- -15-Volt Supply: 20 mA

RFL 93 FT/FR I/O-13SL and RFL 93 FT/FR I/O-15SL:
- +5-Volt Supply: 6 mA
- +15-Volt Supply: 50 mA
- -15-Volt Supply: 80 mA

Input Drive Signals: TTL logic-level, generated by RFL 93B FT/FR single width fiber optic transceiver module (Section 17).

Output Light Signal Characteristics: See Table 18-1.

Temperature:

Storage: -40^{O}C to +75^{O}C (-40^{O}F to +167^{O}F).
Operating: -30^{O}C to +65^{O}C (-22^{O}F to +149^{O}F).

Relative Humidity: 95 percent, non-condensing.

Dimensions:

Width (including panel) 1.4 inches (3.6 cm)
Height (including panel) 5 inches (12.7 cm)
Depth (behind panel) 4.7 inches (12.0 cm)

18.4 CONTROLS AND INDICATORS

Figures 18-2 through 18-4 show the locations of all controls and indicators on the RFL 93 FT/FR single width fiber optic I/O modules. These controls and indicators are described below.

Controls

R30	Potentiometer used at factory for adjusting Avalanch Photo Diode (CR9) bias current

Test Turrets

TP1	Monitoring point for LED emitter (U1) drive current
TP2	Monitoring point for high voltage supply
TP3	Monitoring point for REC_DATA signal
TP4	Monitoring point for Avalanch Photo Diode (CR9) bias current. 25mV is equivalent to about 0.5nA, and 150mV is equivalent to about 3.0nA.
TP5	Ground

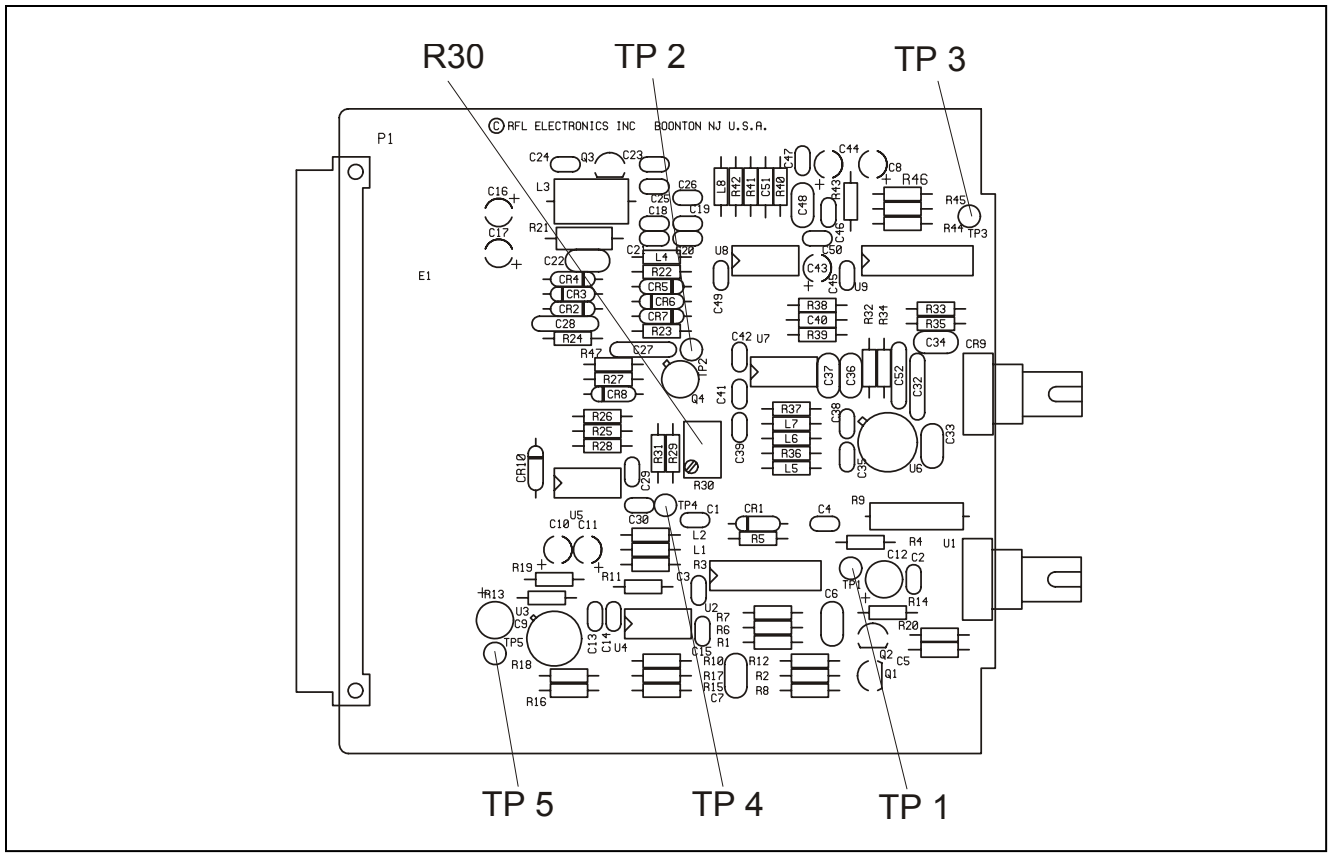


Figure 18-2. Controls and indicators, RFL 93 FT/FR I/O-8M single width fiber optic I/O module

Test Turrets

TP1	Monitoring point for LED emitter (U1) drive signal
TP2	Monitoring point for REC_DATA signal
TP3	Monitoring point for a voltage that is proportional to the light level into photo diode CR6. The voltage can vary from about 0 to 10Vdc.
TP4	Ground

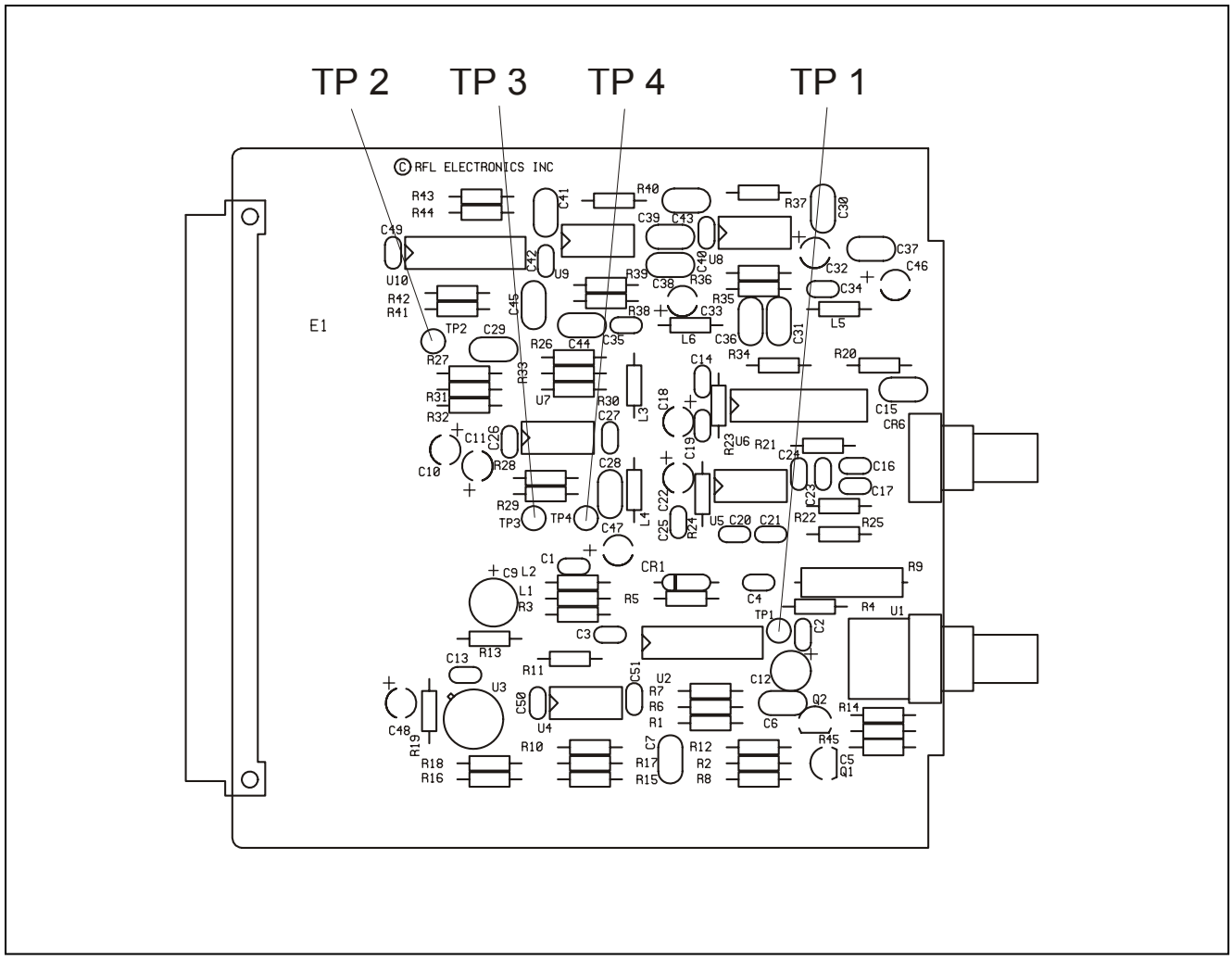


Figure 18-3. Controls and indicators, RFL 93 FT/FR I/O-13S and 13 M single width fiber optic I/O modules

Controls

R12	Potentiometer used at factory for adjusting Avalanch Photo Diode (U2) bias current

Test Turrets

TP2	Monitoring point for LASER emitter (U2) drive signal
TP3	Monitoring point for -11Vdc source
TP4	Monitoring point for REC_DATA signal
TP5	Monitoring point for a voltage that is proportional to the light level into photo diode CR2. The voltage can vary from about 0 to 10Vdc.
TP6	Ground

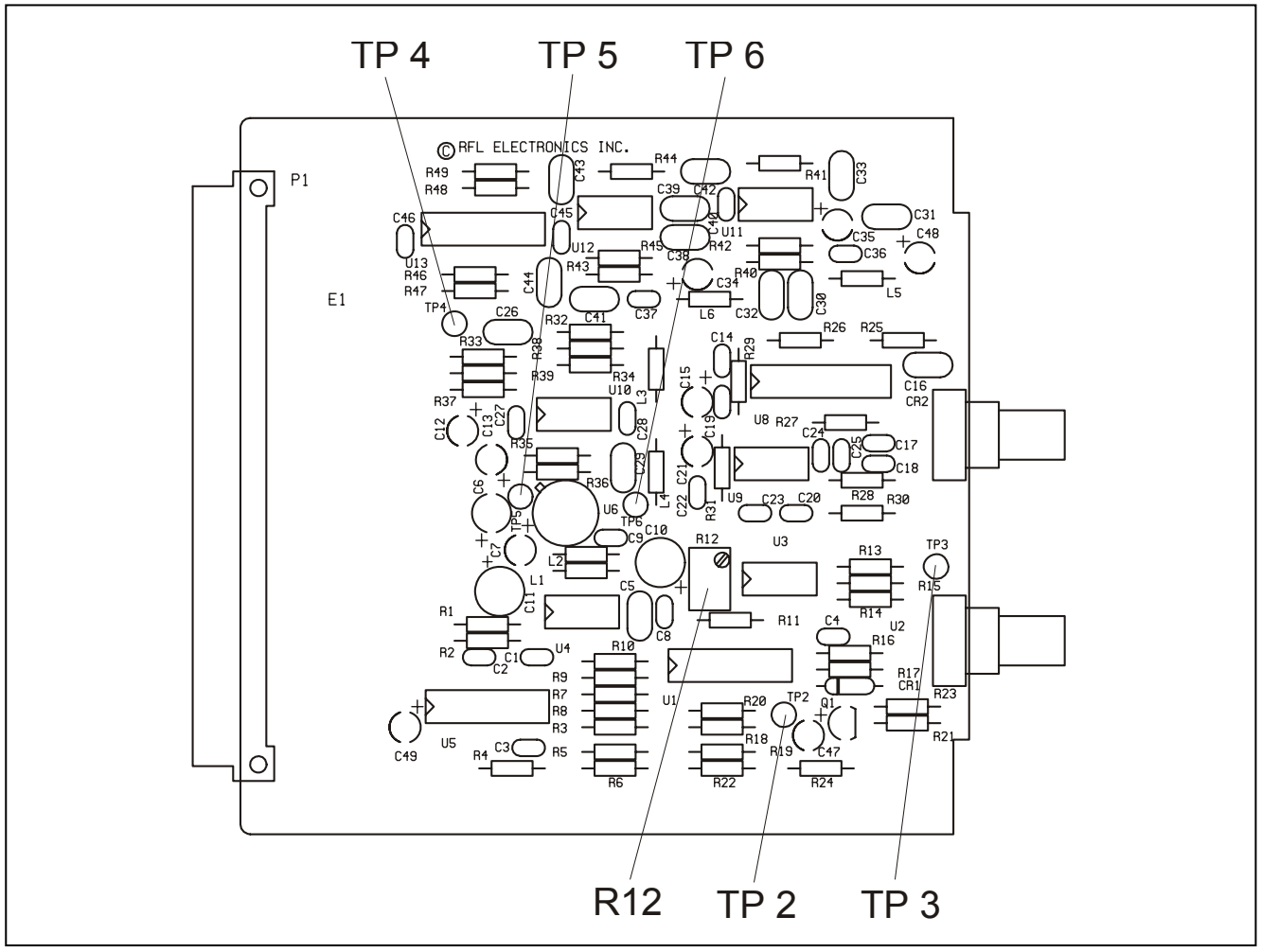


Figure 18-4. Controls and indicators, RFL 93 FT/FR I/O-13SL and 15SL single width fiber optic I/O modules

18.5 THEORY OF OPERATION

Single width fiber optic I/O modules contain both emitter and detector circuitry making them suitable for both transmission and reception of light signals over an optic fiber. Although all I/O modules perform the same function, each operates in a slightly different manner, so theories of operation are provided for each fiber optic I/O module which are described below.

18.5.1 RFL 93 FT/FR-8M

Overview

The RFL 93 FT/FR-8M single width fiber optic I/O module contains both LED emitter and photodiode detector circuitry. The transmit section consists of the LED, LED current driver, and alarm circuits to detect misoperation due to component failures. The receive section consists of the APD (Avalanch Photo Diode), high voltage tank circuit, shunt current regulator, several stages of amplification and a schmitt trigger output stage. A block diagram is shown in Figure 18-5, and a schematic diagram is shown in Figure 18-9.

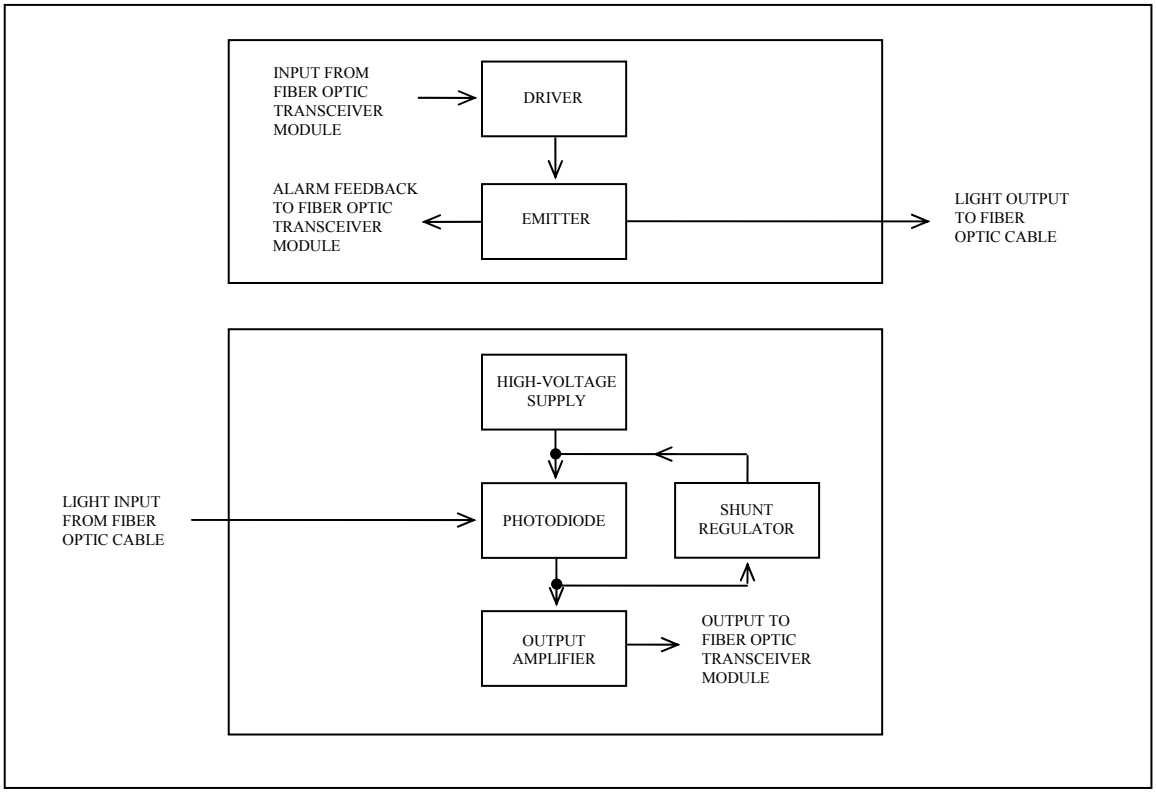


Figure 18-5. Block diagram, RFL 93 FT/FR I/O-8M 850 nm Multimode Fiber Optic I/O Module

Transmit Section

The fiber optic LED U1 is driven from a current source generated by Q1 and Q2. The unmodulated bias current through the LED is controlled by R2 and R20, which sets the bias voltage for emitter followers Q1 and Q2. The voltage across R9 produces a bias current which is essentially the same as the LED current. This causes the LED to emit, without modulation, a constant light output at approximately the average output power.

Modulation is accomplished by ac coupling the transmit data signal into the current driver circuit through C6. The signal switches the current in the LED between a maximum limited value and zero. The current is limited by U2, which compares the voltage across R9 (at pin 6) with a reference voltage (at pin 9) formed by CR1, R4 and R5, and limits the voltage at the base of Q1 by the current through pin 5. The maximum voltage across R9 is about 1.2 volts, which limits the LED current to about 100 mA.

An alarm output is generated at P2 pin 2 if the voltage across the LED deviates considerably from its nominal value due to component malfunctions. The LED voltage is filtered by R12 and C7, and then buffered by U4A. Voltage reference levels are generated by R10, R11, and R13. The upper reference voltage is also buffered by U4B. Buffering is required to keep the voltages being compared from being effected by the operation of the comparator circuitry. A window comparator is formed by dual comparator U3, whose open collector outputs are connected to pullup resistor R19 and the Tx alarm output. Resistors R16 and R18 provide hysterisis. The alarm output is an active low.

Receive Section

The avalanche photodiode (APD) CR9 is the detector for incoming light signals. CR9 is operated in the reverse breakdown region with its dc reverse current reguated to achieve maximum sensitivity. Current regulation yields a flat photomultplcation factor over the operating temperature range.

The high voltage for the reverse breakdown mode is generated from the LC tank circuit formed by L4 (180uH) and C18-21 (4 - 470 pF capacitors in series) and resonated by switching transistor Q3 and C25 and C26. R22 and C22 form a voltage doubler. The high voltage sine wave is rectified and filtered by CR2-CR7 and R23, 24 and C27, 28. The tank circuit oscillates at 1.1 Mhz.

A shunt current regulator is used to keep a constant dc reverse bias current through CR9. The regulator is formed by operational amplifier U5, transistor Q4, and their associated components. The dc voltage across R31 reflects the reverse bias current through CR9. This is compared to a reference voltage set by potentiometer R9 at the input to U5, which drives transistor Q4 (shunting element) that in turn steers excess current away from CR9 in order to maintain a constant dc reverse bias current in CR9. By adjusting R31 to vary the reverse bias current, the optimum point in the avalanche region can be located for each APD.

The signal from CR9 in response to the incident light signal is coupled by C33 to U6 (low noise amplifier). The output of U6 drives two differential amplifier sections consisting of U7 and U8. The stages are ac coupled by capacitors C35, C41 and C42, which act as high pass filters. High frequency gain is limited by capacitors C40 and C51. This reduces the noise bandwidth, allowing better receiver sensitivity. The gain is set by resistors R38, R39, R41 and R42. These amplifiers will limit symmetrically for large input signals. Both LC and RC filtering are again used on the power inputs to these amplifiers.

Capacitor C50 couples the signal at U8 pin 8 to U9F, which performs as a linear amplifier with a gain of 10 for small signals. This stage will also provide limiting for large signals. The signal then passes through a schmitt trigger circuit formed by two sections of U9 and resistors R45 and R46. The output of this stage is the digital Rx Data signal. The other three sections of U9 are not used.

18.5.2 RFL 93 FT/FR-13M and RFL 93 FT/FR-13S

Overview

The RFL 93 FT/FR-13M and RFL 93 FT/FR-13S single width fiber optic I/O modules contain both LED emitter and photodiode detector circuitry. The transmit section consists of the LED, LED current driver, and alarm circuits to detect misoperation due to component failures. The receive section consists of the fiber optic photodetector, a switched gain transimpedance amplifier, several stages of amplification and a schmitt trigger limiter. A block diagram is shown in Figure 18-6, and a schematic diagram is shown in Figure 18-11.

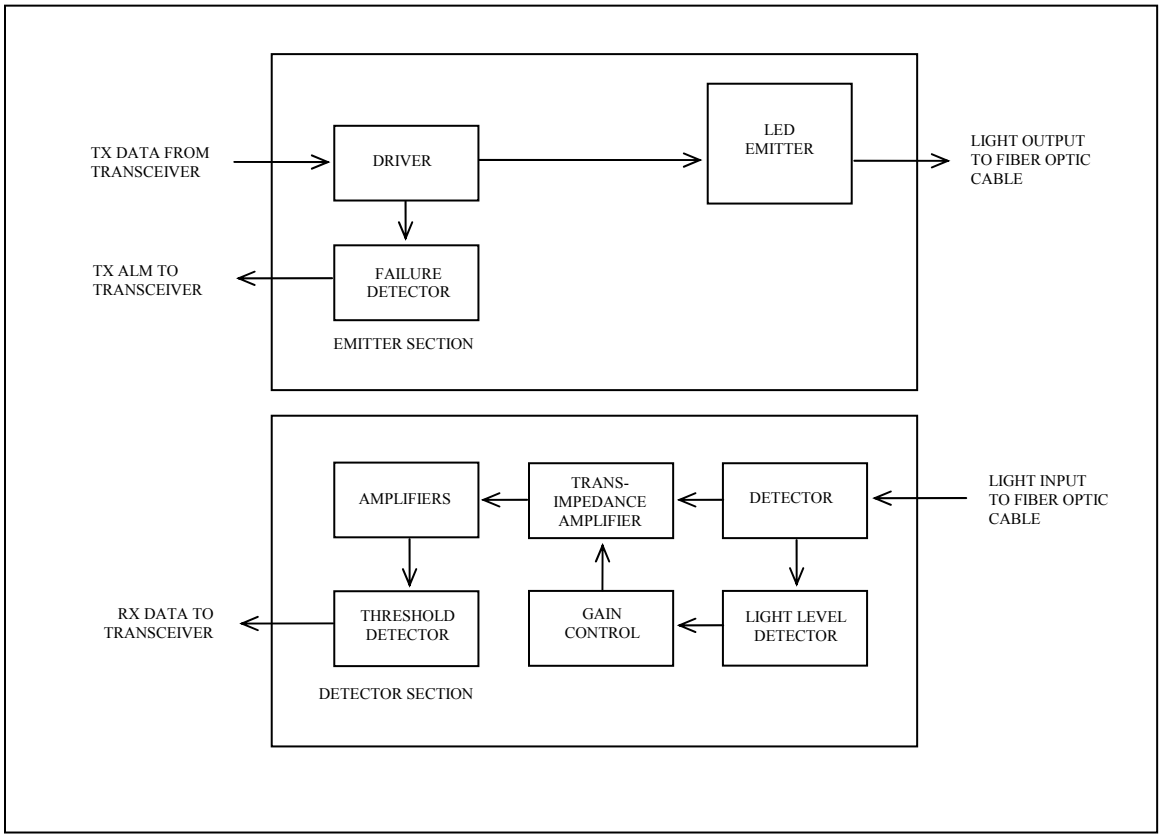


Figure 18-6. Block diagram, RFL 93 FT/FR-13M (Multimode) and RFL 93 FT/FR-S (Singlemode) 1300-nm Fiber Optic I/O Module

Transmit Section

The fiber optic LED U1 is driven from a current source generated by Q1 and Q2. The unmodulated bias current through the LED is controlled by R2 and R45, which sets the bias voltage for emitter followers Q1 and Q2. The voltage across R9 produces a bias current which is essentially the same as the LED current. This causes the LED to emit a constant light output at approximately the average output power, without modulation.

Modulation is accomplished by ac coupling the transmit data signal into the current driver circuit through C6. The signal switches the current in the LED between a maximum limited value and zero. The current is limited by U2, which compares the voltage across R9 (at pin 6) with a reference voltage (at pin 9) formed by CR1, R4 and R5, and limits the voltage at the base of Q1 by the current through pin 5. The maximum voltage across R9 is about 1.2 volts, which limits the LED current to about 100 mA.

An alarm output is generated at P2 pin 2 if the voltage across the LED deviates considerably from its nominal value due to component malfunctions. The LED voltage is filtered by R12 and C7, and is then buffered by U4A. Voltage reference levels are generated by R10, R11, and R13. The upper reference voltage is also buffered by U4B. Buffering is required to keep the voltages being compared from being effected by the operation of the comparator circuitry. A window comparator is formed by dual comparator U3, whose open collector outputs are connected to pullup resistor R19 and the Tx alarm output. Resistors R16 and R18 provide hysterisis. The alarm output is an active low.

Receive Section

The current output of photodiode detector CR6 is converted to a voltage using U5, which is configured as a switchable gain transimpedance amplifier. Amplifier U5 is a low noise, high speed operational amplifier. The normal gain is controlled by R22. For large input signals, the gain is reduced to avoid saturation of the amplifier output. This is accomplished by switching in shunt resistor R21 across the normal feedback resitor R22 using analog switch U6 (pins 14 - 15). The switch side of R21 (U6 pin 15) is shunted to ground when using the high gain configuration to reduce feedback signals resulting from the leakage capacitance across the open switch. Frequency compensation for the low gain setting is provided by C23 and switch U6 pins 10 - 11. Switch section U6 pins 6 - 7 is used as a logic inverter to generate complementary signals for the various switch settings. Both RC and LC filtering is used on the power supplies to the amplifier in order to reduce noise pickup.

Detector CR6 is connected to the +15 volt source through an RC filter formed by R20 and C15. The photodiode acts as a current source, where the current is proportional to the light input. This current causes a voltage drop across the filter resistor R20. The voltage at pin 2 of CR6 therefore decreases from +15 volts proportionally with the averge light input, reaching near 0 volts with an average light level of 0 dBm. Amplifier U7A and associated circuitry form a differential amplifier that produces an output of approximately 0 to +10 volts for input light levels ranging from no light to 0dBm respectively. The second section of U7 is configured as a comparator, where the output (pin 7) switches from negative to positive as the input light level increases past approximately -13 dBm. This output is used to control the switches that change the gain of U5. Resistor R33 provides hysteresis for the comparator.

The output of U5 drives two differential amplifier sections consisting of U8 and U9. The stages are ac coupled by capacitors C31, C38, and C39, which act as high pass filters. High frequency gain is limited by capacitors C40 and C42. This reduces the noise bandwidth, allowing better receiver sensitivity. The gain is set by resistors R36, R37, R39 and R40. These amplifiers will limit symmetrically for large input signals. Both LC and RC fitering are again used on the power inputs to these amplifiers.

Capacitor C45 couples the signal at U9 pin 1 to U10A, which performs as a linear amplifier with a gain of 10 for small signals. This stage will also provide limiting for large signals. The signal then passes through a schmitt trigger circuit formed by two sections of U10 and resistors R43 and R44. The output of this stage is the digital Rx Data signal. The other three sections of U10 are not used.

18.5.3 RFL 93 FT/FR-13SL and RFL 93 FT/FR-15SL

Overview

The RFL 93 FT/FR-13SL and RFL 93 FT/FR-15SL single width fiber optic I/O modules contain both the laser diode emitter and photodiode detector circuitry. The transmit section consists of the laser diode, laser diode control and current driver, and alarm circuits to detect misoperation due to component failures. The receive section consists of the fiber optic photodetector, a switched gain transimpedance amplifier, several stages of amplification and a schmitt trigger limiter. A block diagram is shown in Figure 18-7 and a schematic diagram is shown in Figure 18-13.

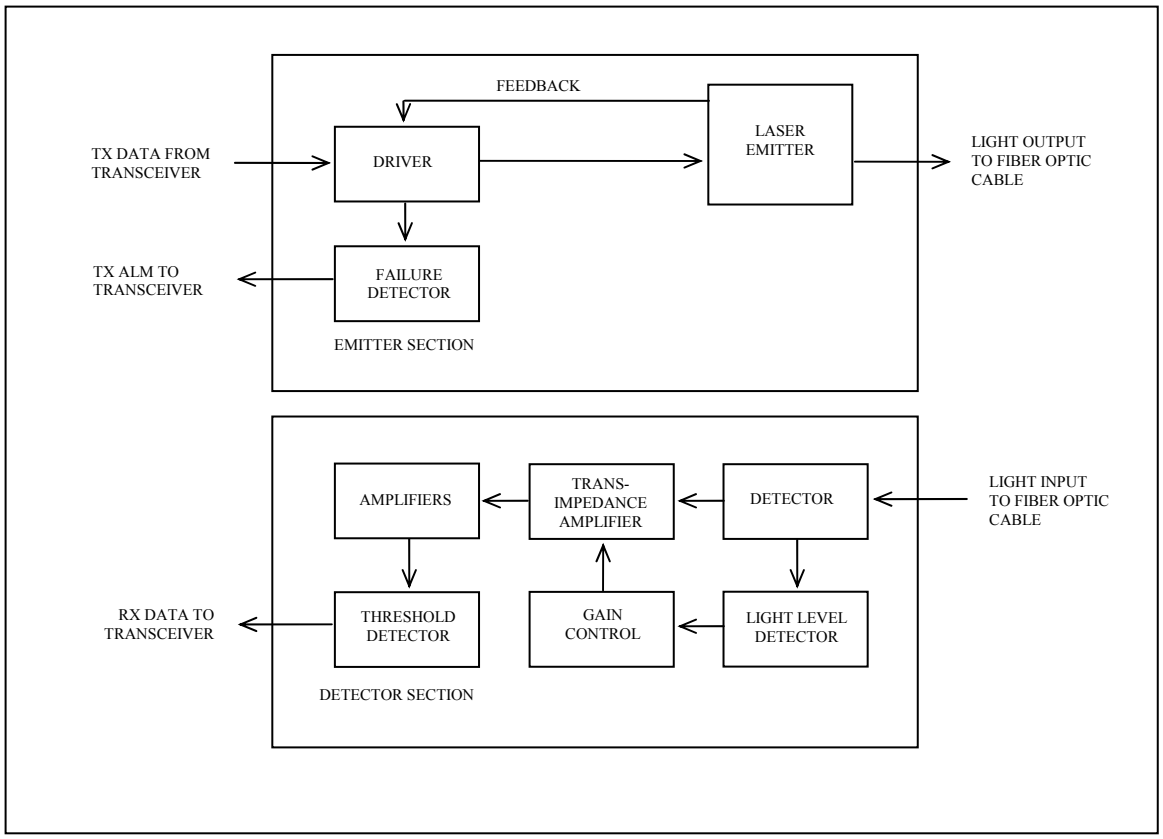


Figure 18-7. Block diagram, RFL 93 FT/FR 13SL (1300-nm Singlemode) and RFL 93 FT/FR 15SL (1550-nm Singlemode)

Transmit Section

The fiber optic laser diode U2 is driven from a current source generated by Q1. A photodiode inside U2 senses the light output of the laser diode and produces a current proportional to the output light level. This current produces a voltage across R12 and R13. The voltage level can be adjusted using R12. This voltage is then compared to a reference voltage by U3, which performs as an integrating comparator. The output of U3 controls the base of Q1 through R17 and one of the transistors in U1, which in turn will control the current through the laser diode. This feedback loop will control the average output level of the laser diode, independent of temperature or component variations.

The digital Tx data modulation signal is attenuated by R1 and R2, and coupled to the base of Q1 through C1 and one of the transistors in U1. This causes the laser diode current to vary from slightly above the laser threshold current to a current that will produce the rated output power under a 50% modulation current condition.

A voltage proportional to the current in the laser diode is sensed at pin 4 of U1. This voltage is compared to a reference voltage at pin 3 of U2, and will control Q1 to limit the maximum laser diode current to a safe level, if necessary.

An alarm circuit is used to sense the proper operation of the laser control loop. Under normal operation, the voltages at pins 2 and 3 of U3 should be nearly equal. These two voltages are buffered by the amplifiers in U4, and applied to a window comparator formed by U5 and its associated circuitry. The comparison voltages are generated by resistors R5, R6, R7 and R8. The open collector outputs of the comparators in U5 are connected to pull up resistor R4 and to the Tx alarm output on pin 2 of P2. The alarm output is active low.

Receive Section

The current output of photodiode detector CR2 is converted to a voltage using U9, which is configured as a switchable gain transimpedance amplifier. Amplifier U9 is a low noise, high speed operatonal amplifier. The normal gain is controlled by R28. For large input signals, the gain is reduced to avoid saturation of the amplifier output. This is accomplished by swiching in shunt resistor R27 across the normal feedback resistor R28 using analog switch U8 (pins 14 - 15). The switch side of R27 (U8 pin 15) is shunted to ground when using the high gain configuration to reduce feedback signals resulting from the leakage capacitance across the open switch. Frequency compensation for the low gain setting is provided by C25 and switch U8 pins 6 - 7. Switch section U8 pins 10 - 11 is used as a logic inverter to generate complementary signals for the various switch sections. Both LC and RC filtering is used on the power supplies of the amplifier in order to reduce noise pickup.

Detector CR2 is connected to the +15 volt source through an RC filter formed by R25 and C16. The photodiode acts as a current source, where the current is proportional to the light input. This current causes a voltage drop across the filter resistor R25. The voltage at pin 2 of CR2 therefore decreases from +15 volts proportionally with the average light input, reaching near 0 volts with an average light level of 0 dBm. Amplifier U10A and associated circuitry form a differential amplifier that produces an output of approximately 0 to +10 volts for input light levels of no light to 0 dBm respectively. The second section of U10 is configured as a comparator, where the output (pin 7) switches from negative to positive as the input light level increases past approximately -13 dBm. This output is used to control the switches that change the gain of U9. Resistor R38 provides hysteresis for the comparator.

The output of U9 drives two differential amplifier sections consisting of U11 and U12. The stages are AC coupled by capacitors C30, C38, and C39, which act as high pass filters. High frequency gain is limited by capacitors C40 and C45. This reduces the noise bandwidth, allowing better receiver sensitivity. The gain is set by resistors R41, R42, R44 and R45. These amplifiers provide limiting for large input signals. Both LC and RC filtering are again used on the power inputs of these amplifiers.

Capacitor C44 couples the signal at U12 pin 1 to U13A, which performs as a linear amplifier with a gain of 10 for small signals. This stage also provides limiting for large signals. The signal then passes through a Schmitt trigger circuit formed by two sections of U13 and resistors R46 and R47. The output of this stage is the digital Rx Data signal. The other three sections of U13 are not used.

Table 18-2. Replaceable parts, RFL 93 FT/FR I/O-8M Singlewidth fiber optic I/O module (Assembly No. 105850)

Circuit symbol (Figs 18-8 & 18-9)	Description	Part number
	CAPACITORS	
C1, 2, 3, 4, 13, 14, 15, 23, 24, 29, 30	Capacitor, ceramic, 0.1 μF, 20%, 50V	1007 1366
C5, 40	Capacitor, ceramic, 10 pF, 10%, 200V	0125 21001
C6	Capacitor, ceramic dipped, 0.47 μF, 20%, 50V	1007 1560
C7, 33, 34, 36, 37, 48	Capacitor, ceramic dipped, 0.01 μF, 5%, 100V	1007 1645
C8, 10, 11, 16, 17, 43, 44	Capacitor, tantalum, 1 μF, 10%, 35V	1007 1768
C9	Capacitor, electrolytic, 100 μF, 20%, 25V	1007 1630
C12	Capacitor, tantalum, 22 μF, 20%, 16V	1007 1569
C18, 19, 20, 21	Capacitor, ceramic dipped, 470 pF, 10%, 100V	1007 1392
C22	Capacitor, ceramic disc, 220 pF, 10%, 500V	1007 493
C25	Capacitor, ceramic dipped, 0.001 μF, 10%, 50V	1007 1666
C26	Capacitor, ceramic dipped, 0.0039 μF, 5%, 50V	1007 1657
C27, 28, 32, 52	Capacitor, ceramic disc, 0.01 μF, 20%, 500V	1007 83
C51	Capacitor, ceramic, 15 pF	0125 21505
	RESISTORS	
R1, 10	Resistor, metal film, precision, 449Ω, 1%, 1/4W	0410 1259
R2	Resistor, metal film, precision, 4.99K, 1%, 1/4W	0410 1355
R3, 29	Resistor, metal film, precision, 100Ω, 1%, 1/4W	0410 1192
R4, 5	Resistor, metal film, precision, 3.57K, 1%, 1/4W	0410 1341
R6, 8, 15, 17, 22, 32, 33, 36, 37	Resistor, metal film, precision, 1K, 1%, 1/4W	0410 1288
R7	Resistor, metal film, precision, 301K, 1%, 1/4W	0410 1526
R9	Resistor, metal film, precision, 12.1Ω, 1%, 1/2W	1510 2109
R11	Resistor, metal film, precision, 2.49K, 1%, 1/4W	0410 1326
R12, 16, 28	Resistor, metal film, precision, 100K, 1%, 1/4W	0410 1480
R13	Resistor, metal film, precision, 2K, 1%, 1/4W	0410 1317
R14	Resistor, metal film, precision, 20K, 1%, 1/4W	0410 1413
R18	Resistor, metal film, precision, 100K, 1%, 1/4W	0410 1480
R19	Resistor, metal film, precision, 3.01K, 1%, 1/4W	0410 1334
R20	Resistor, metal film, precision, 4.32K, 1%, 1/4W	0410 1349
R21	Resistor, metal film, precision, 511Ω, 1%, 1/2W	0410 2260
R23, 24, 25, 34	Resistor, metal film, precision, 499K, 1%, 1/4W	0410 1547

Table 18-2 continued. Replaceable parts, RFL 93 FT/FR I/O-8M Singlewidth fiber optic I/O module

Circuit symbol (Figs 18-8 & 18-9)	Description	Part number
	RESISTORS (continued)	
R26, 35, 44, 46	Resistor, metal film, precision, 10K, 1%, 1/4W	0410 1384
R27	Resistor, metal film, precision, 64.9K, 1%, 1/4W	0410 1462
R30	Resistor, variable, metal film, 1K, 10%, 1/2W	49995
R31	Resistor, metal film, precision, 49.9K, 1%, 1/4W	0410 1451
R38, 39, 40, 41, 42	Resistor, metal film, precision, 475Ω, 1%, 1/4W	0410 1257
	SEMICONDUCTORS	
CR1	Diode, zener, 2.4V, 500 mW, 1N5221B	40476
CR2, 3, 4, 5, 6, 7, 8	Diode, silcon, 1N914B/1N4448	26482
CR9	Opto device, fiber optic detector diode	30258
Q1	Transistor, silicon, NPN, 2N3903	21562
Q2	Transistor, silicon, NPN, 2N2222A	37445
Q3	Transistor, silicon, NPN, 2N5551	39484
Q4	Transistor, silicon, NPN, 2N6431	30504
U1	Opto device, fiber optic emitter, 850nm	101747
U2	Transistor array, NPN, CA3045F	0720 18
U3	Integrated circuit, linear dual comparator	0620 319
U4	Integrated circuit, linear, JFET, OP AMP	0620 227
U5	Integrated circuit, linear, JFET, OP AMP	0620 228
U6	Amplifier, hybrid	30505
U7, 8	Integrated circuit, linear, IF amplifier	0620 251
U9	Integrated circuit, MOS hex inverter, unbufferd	0615 304
	MISCELLANEOUS COMPONENTS	
L1, 2	Inductor, molded, 33 μH, 130mA	32868
L3	Choke, RF, 18mH, subminiature	21371
L4, 5	Inductor, Molded, RF, 180 μH, 10%	32505 2
L6, 7, 8	Inductor, Molded, RF, 100 μH, 10%	32505 1
P1	Connector, plug, female, 64 contacts, DIN	99134
TP1-5	Test point, terminal, orange	98441 3

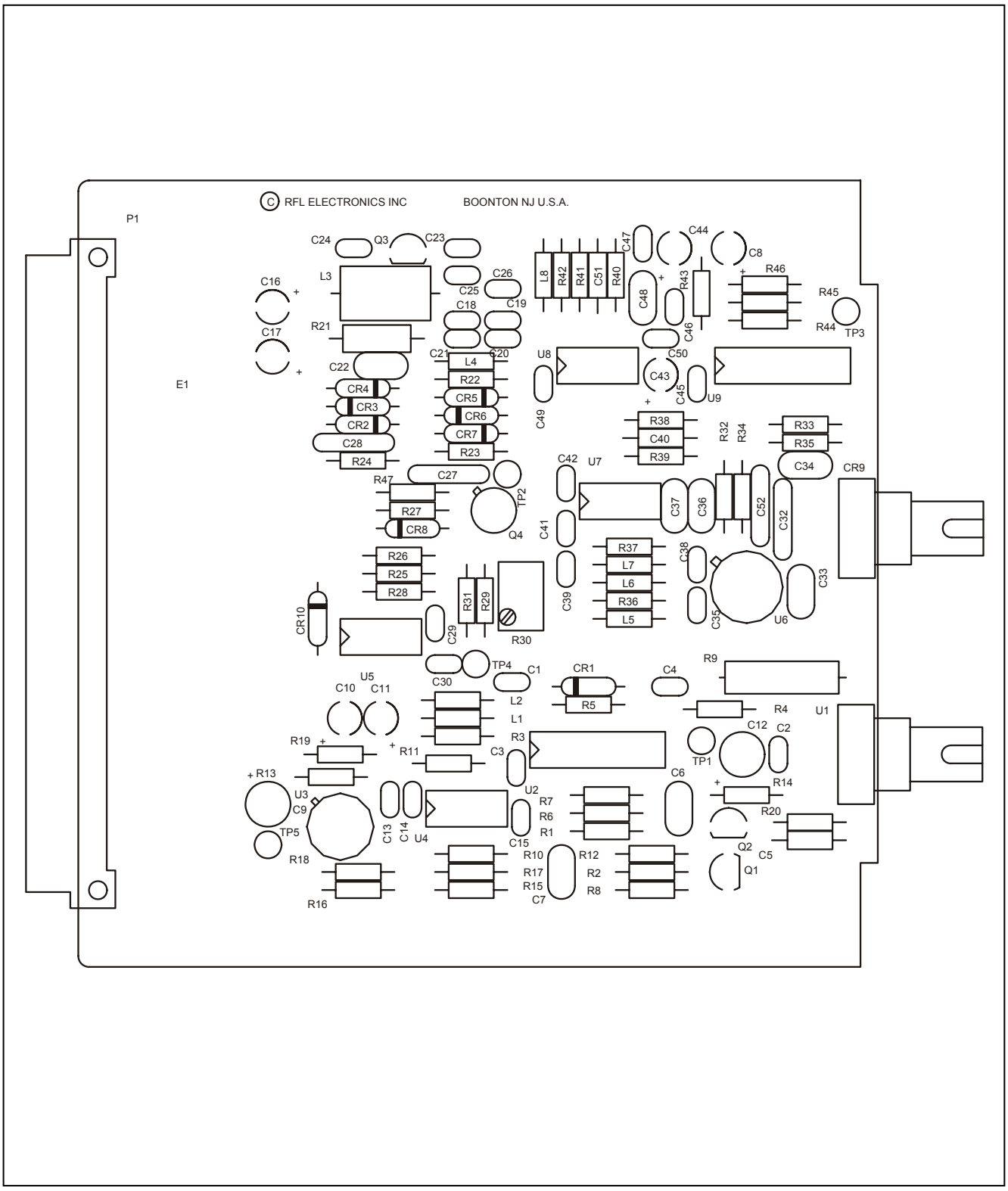


Figure 18-8. Component locator drawing, RFL 93 FT/FR I/O-8M 850-nm Multimode Singlewidth Fiber Optic I/O Module (Assembly No. 105850; Drawing No. 105853-A)

Figure 18-9. RFL 93 FT/FR Singlewidth Fiber Optic I/O Module -8M (Assembly No. 105850; Schematic No. D-105854, Rev. D)

Please see Figure 18-9, in Section 32: Schematics

Table 18-3. Replaceable parts, RFL 93 FT/FR I/O Singlewidth fiber optic I/O modules
RFL 93 FT/FR I/O-13M (Singlemode) (Assembly No. 105855)
RFL 93 FT/FR I/O-13S (Multimode) (Assembly No. 105860)

Circuit symbol (Figs 18-10 & 18-11)	Description	Part number
	CAPACITORS	
C1, 2, 13, 14, 19, 20, 21, 25, 26, 27, 34, 35, 49, 50, 51	Capacitor, ceramic, 0.1 μF, 20%, 50V	1007 1366
C7, 15, 28, 29, 30, 36, 37, 43, 44	Capacitor, ceramic, dipped, 0.01 μF, 5%, 100V	1007 1645
C9	Capacitor, electrolytic, 100 μF, 20%, 25V	1007 1630
C10, 11, 18, 22, 33, 32, 46, 47, 48	Capacitor, tantalum, 1 μF, 10%, 35V	1007 1768
C12	Capacitor, tantalum, 22 μF, 20%, 16V	1007 1569
C16	Capacitor, ceramic, 5 pF +1 -0.5 pF, 200V	0125 25R04
C23	Capacitor, ceramic, dipped, 10 pF, 10%, 200V	1007 1462
C31, 38, 39, 41, 45	Capacitor, ceramic, dipped, 0.1 μF, 10%, 50V	1007 1769
C40, 42	Capacitor, ceramic, dipped, 100 pF, 10%, 100V	1007 1671
	RESISTORS	
R1, 10	Resistor, metal film, precision, 499Ω, 1%, 1/4W	0410 1259
R15, 17, 41, 43	Resistor, metal film, precision, 1K, 1%, 1/4W	0410 1288
R9	Resistor, metal film, precision, 23.7Ω, 1%, 1/2W	1510 2132
R11	Resistor, metal film, precision, 11.87K, 1%, 1/2W	0410 1314
R12, 18, 16	Resistor, metal film, precision, 100K, 1%, 1/4W	0410 1480
R13	Resistor, metal film, precision, 3.09K, 1%, 1/4W	0410 1335
R14	Resistor, metal film, precision, 20K, 1%, 1/4W	0410 1413
R19	Resistor, metal film, precision, 3.01K, 1%, 1/4W	0410 1334
R20	Resistor, metal film, precision, 16.9K, 1%, 1/4W	0410 1406
R22, 25	Resistor, metal film, precision, 24.9K, 1%, 1/4W	0410 1422
R23, 24, 35, 38	Resistor, metal film, precision, 182Ω, 1%, 1/4W	0410 1217
R26	Resistor, metal film, precision, 133K, 1%, 1/4W	0410 1492
R27, 29	Resistor, metal film, precision, 110K, 1%, 1/4W	0410 1484

Table 18-3 (continued). Replaceable parts, Singlewidth fiber optic I/O modules
RFL 93 FT/FR I/O-13M (Singlemode) (Assembly No. 105855)
RFL 93 FT/FR I/O-13S (Multimode) (Assembly No. 105860)

Circuit symbol (Figs 18-10 & 18-11)	Description	Part number
	RESISTORS (continued)	
R28	Resistor, metal film, precision, 150K, 1%, 1/4W	0410 1497
R30, 32	Resistor, metal film, precision, 301Ω, 1%, 1/4W	0410 1238
R31	Resistor, metal film, precision, 14.7K, 1%, 1/4W	0410 1400
R33	Resistor, metal film, precision, 60.4K, 1%, 1/4W	0410 1459
R34, 42, 44	Resistor, metal film, precision, 10K, 1%, 1/4W	0410 1384
R36, 37, 39, 40	Resistor, metal film, precision, 475Ω, 1%, 1/4W	0410 1257
R45	Resistor, metal film, precision, 4.32K, 1%, 1/4W	0410 1349
	SEMICONDUCTORS	
CR6	Opto device, fiber optic detector, 1300/1550-nm	101733
Q2	Transistor, VMOS, FET, VN10KM	0715 13
U1	Opto device, fiber optic emitter, 1300nm	
	For multimode module (Assembly No. 105855)	101731
	For singlemode module (Assembly No. 105860)	101727
U3	IC, linear, dual comparator	0620 319
U4, 7	IC, linear, JFET, OP AMP	0620 227
U5	IC, low noise, video OP AMP	0620 354
U6	IC, analog switch, quad, SPST, CMOS	0605 17
U8, 9	IC, linear, IF amplifier	0620 251
U10	IC, MOS, hex inverter, unbufferd	0615 304
	MISCELLANEOUS COMPONENTS	
L1, 2	Inductor, molded, 33 μH, 130MA	32868
L3, 4, 5, 6	Inductor, molded, RF, 100 μH, 10%	32505 1
P1	Connector, plug, female, 64 contact, DIN	99134
TP1-4	Test point, terminal, orange	98441 3

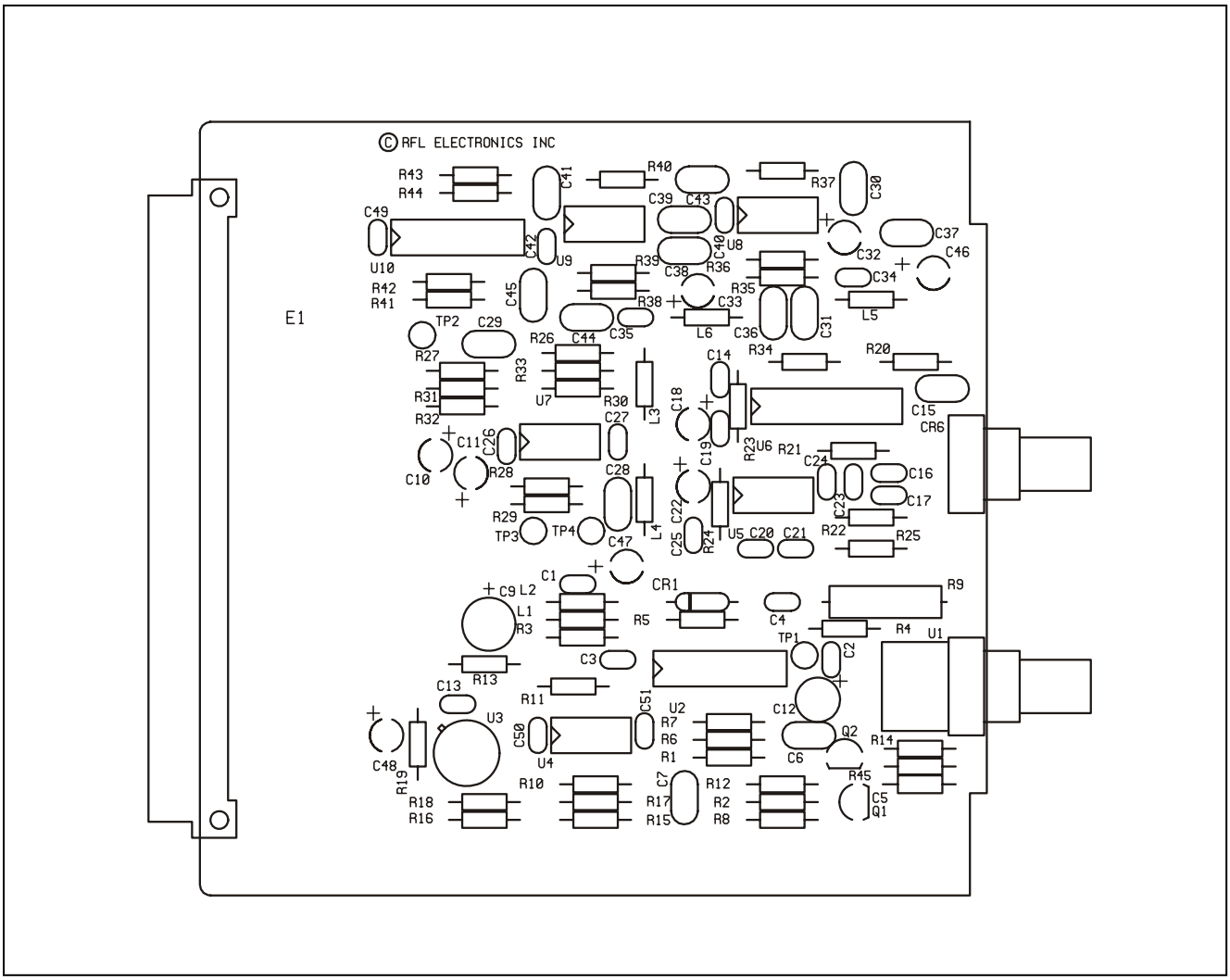


Figure 18-10. Component locator drawing, RFL 93 FT/FR I/O-13M and RFL 93 FT/FR I/O-13S

Figure 18-11. RFL 93 FT/FR Singlewidth Fiber Optic I/O Modules, -13M (Assembly No. 105855; Schematic No. D-105864, Rev. A), -13S (Assembly No. 105860; Schematic No. D-105864, Rev. A)

Please see Figure 18-11, in Section 32: Schematics

Table 18-4. Replaceable parts, Singlewidth fiber optic I/O modules
RFL 93 FT/FR I/O-13SL (single mode, LASER) (Assembly No. 105865)
RFL 93 FT/FR I/O-15SL (single mode, LASER) (Assembly No. 105870)

Circuit symbol (Figs. 18-12 & 18-13)	Description	Part number
	CAPACITORS	
C1, 4, 14, 19, 20, 22, 23, 27, 28, 36, 37	Capacitor, ceramic, 0.1 μF, 20%, 50V	1007 1366
C5, 16, 26, 29, 31, 32 33, 41, 42	Capacitor, ceramic dipped, .01 μF, 5%, 100V	1007 1645
C6	Capacitor, tantalum, 2.2 μF, 10%, 35V	1007 1681
C7, 12, 13, 15, 21, 34, 35, 47, 48, 49	Capacitor, tantalum, 1μ F, 10%, 35V	1007 1768
C10, 11	Capacitor, electrolytic, 100 μF, 20%, 25V	1007 1630
C17	Capacitor, ceramic, 5 pF +1 - 0.5pF, 200V	0125 25R04
C25	Capacitor, ceramic dipped, 10 pF, 10%, 200V	1007 1462
C30, 38, 39, 43, 44	Capacitor, ceramic dipped, 0.1μF, 10%, 50V	1007 1769
C40, 45	Capacitor, ceramic dipped, 100pF, 10%, 100V	1007 1671
	RESISTORS	
R1	Resistor, metal film, precision, 1.5K, 1%, 1/4W	0410 1305
R2, R20	Resistor, metal film, precision, 499 Ω, 1%, 1/4W	0410 1259
R3, 9	Resistor, metal film, precision, 49.9K, 1%, 1/4W	0410 1451
R4, 27	Resistor, metal film, precision, 3.01K, 1%, 1/4W	0410 1334
R5	Resistor, metal film, precision, 21K, 1%, 1/4W	0410 1415
R6, 10, 16, 21, 47, 49	Resistor, metal film, precision, 1K, 1%, 1/4W	0410 1288
R7, R8	Resistor, metal film, precision, 11K, 1%, 1/4W	0410 1388
R11, 14	Resistor, metal film, precision, 100K, 1%, 1/4W	0410 1480
R12	Resistor, variable, metal film, 50K, 10%, 1/2W	93667
R13	Resistor, metal film, precision, 6.65Ω, 1%, 1/4W	0410 1367
R15	Resistor, metal film, precision, 75K, 1%, 1/4W	0410 1468
R17, 26, 46, 48	Resistor, metal film, precision, 10K, 1%, 1/4W	0410 1384
R18	Resistor, metal film, precision, 681 Ω, 1%, 1/4W	0410 1272
R19	Resistor, metal film, precision, 100 Ω, 1%, 1/4W	0410 1192
R22	Resistor, metal film, precision, 10 Ω, 1%, 1/4W	1510 1015
R23	Resistor, metal film, precision, 10 Ω, 1%, 1/8W	1510 1092
R24	Resistor, metal film, precision, 49.9 Ω, 1%, 1/4W	0410 1163
R25	Resistor, metal film, precision, 16.9K, 1%, 1/4W	0410 1406
R28, 30	Resistor, metal film, precision, 24.9K, 1%, 1/4W	0410 1422
R29, 31, 40, 43	Resistor, metal film, precision, 182 Ω, 1%, 1/4W	0410 1217

Table 18-4 continued. Replaceable parts, Singlewidth fiber optic I/O modules
RFL 93 FT/FR I/O-13SL (single mode, LASER) (Assembly No. 105865)
RFL 93 FT/FR I/O-15SL (single mode, LASER) (Assembly No. 105870)

Circuit symbol (Figs. 18-12 & 18-13)	Description	Part number
	RESISTORS (continued)	
R32	Resistor, metal film, precision, 133K, 1%, 1/4W	0410 1492
R33, 36	Resistor, metal film, precision, 110K, 1%, 1/4W	0410 1484
R34, 37	Resistor, metal film, precision, 301Ω, 1%, 1/4W	0410 1238
R35	Resistor, metal film, precision, 150K, 1%, 1/4W	0410 1497
R38	Resistor, metal film, precision, 60.4K, 1%, 1/4W	0410 1459
R39	Resistor, metal film, precision, 14.7K, 1%, 1/4W	0410 1400
R41, 42, 44, 45	Resistor, metal film, precision, 475Ω, 1%, 1/4W	0410 1257
	SEMICONDUCTORS	
CR1	Diode, silicon, 1N914B / 1N4448	26482
CR2	Opto device, fiber optic detector, 1300/1550NM	101733
Q1	Transistor, silicon, NPN 2N2222A	37445
U1	Transistor Array, NPN, CA3045F	0720 18
U2	Opto device, fiber optic emitter	
	For 1300-nm module (Assembly No. 105865)	101729
	For 1550-nm module (Assembly No. 105870)	101728
U3	Integrated circuit, linear, JFET, OP AMP	0620 228
U4, 10	Integrated circuit, linear, JFET, OP AMP	0620 227
U5	Integrated circuit, linear, dual differential comparator	0620 290
U6	Integrated circuit, linear, 3-terminal, negative voltage regulator	0620 353
U8	Integrated circuit, analog switch, quad, SPST CMOS	0605 17
U9	Integrated circuit, low noise, video OP AMP	0620 354
U11, 12	Integrated circuit, linear IF Amplifier	0620 251
U13	Integrated circuit, MOS, hex inverter, unbuffered	0615 304
	MISCELLANEOUS COMPONENTS	
L1, 2	Inductor, molded, 33 μH, 130 mA	32868
L3, 4, 5, 6	Inductor, molded, 100 μH, 10%	32505 1
P1	Connector, plug, female, 64 contacts, DIN	102061
TP2-6	Test point, terminal, orange	98441 3

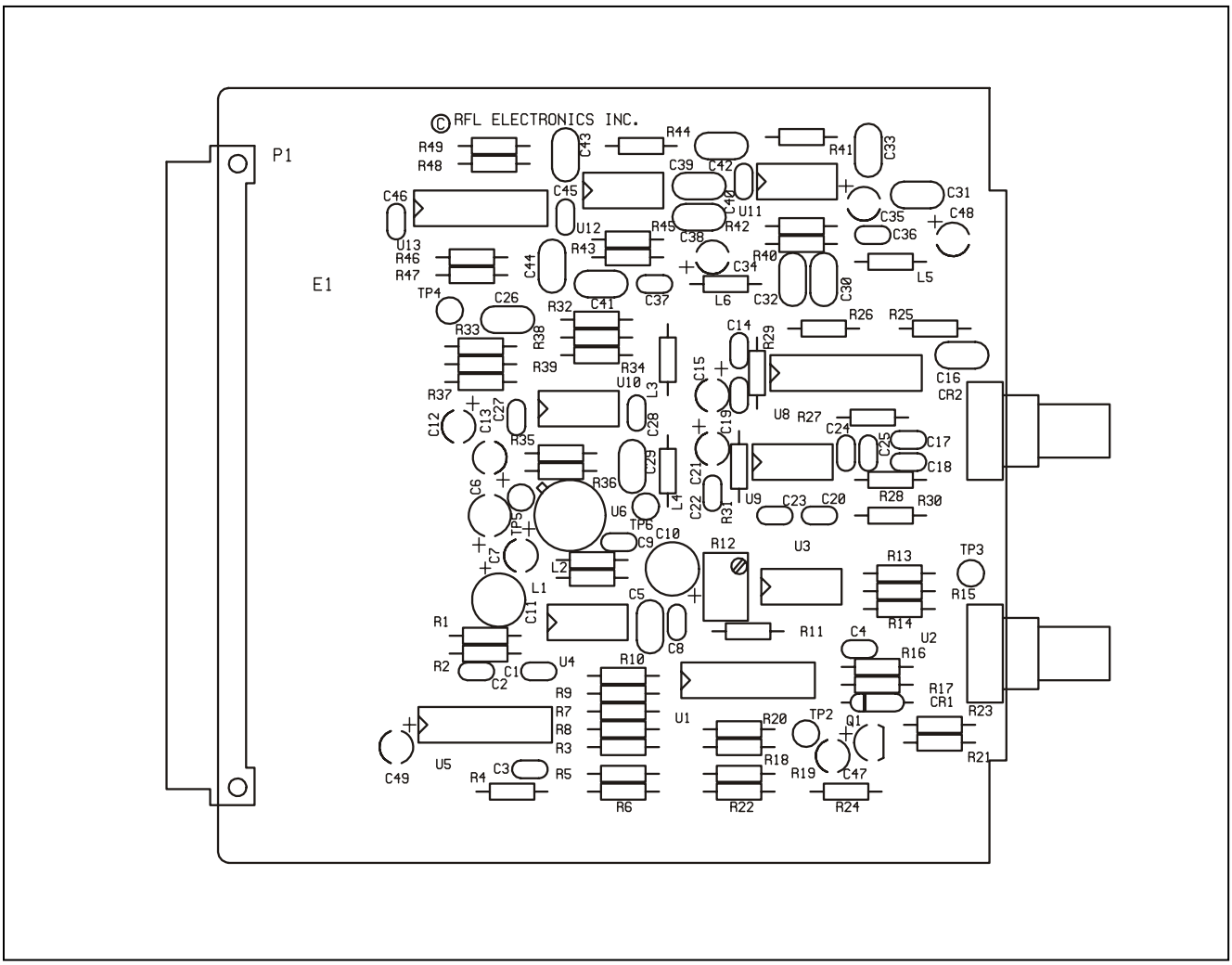


Figure 18-12. Component locator drawing, RFL 93 FT/FR I/O-13SL and RFL 93 FT/FR I/O-15SL

Figure 18-13. RFL 93 FT/FR Singlewidth Fiber Optic I/O Modules, -13SL (Assembly No. 105865; Schematic No. D-105869, Rev. A), -15SL (Assembly No. 105870; Schematic No. D-105869, Rev. A)

Please see Figure 18-13, in Section 32: Schematics

SECTION 19: POWER SUPPLY MODULE

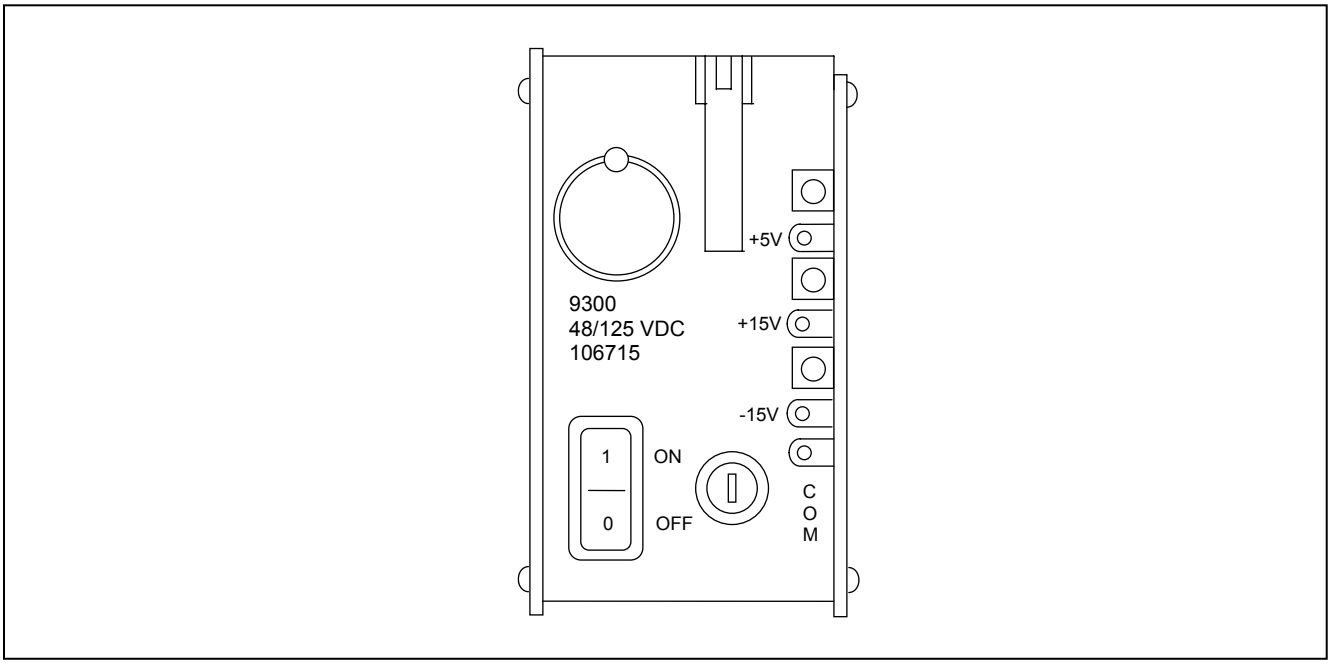


Figure 19-1. Typical RFL 9300 power supply module

19.1 DESCRIPTION

The wide range, 50 Watt power supply shown in Figure 19-1 is a multiple output, forward, dc to dc converter, which is used to supply regulated dc power to the RFL 9300 Charge Comparison System. The power supply operates from a 38 to 150 Vdc input and provides three regulated dc outputs: +5 Vdc at 2.5 Amps, + 15 Vdc at 1.3 Amps, and -15 Vdc at -0.6 Amps. All outputs have overvoltage protection and short circuit protection, and the entire power supply will shut down if the ambient temperature exceeds a pre-established limit. All outputs are constantly monitored and are connected to a common ground. Should any output exceed lower limits power fault monitor (U9), will generate an under voltage signal.

19.2 SPECIFICATIONS

As of the date this manual was published, the specifications shown in Table 19-1 apply to the RFL 9300 power supply module, except where indicated. Because RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

Table 19-1. 9300 Power Supply Specifications

Power Supply→ **Specifications** ↓	**9300 PS 48/125 DC**
RFL Part No.	106715-1
Input Voltage Range	38-150 Vdc
Maximum Output Current	+5Volts @ 2.3Amps +15Volts @ 1.3 Amps -15Volts @ 0.6 Amps
Adjustments	R114: +5 Volt output adjust R116: +15 Volt output adjust R120: -15 Volt output adjust
Test Points	TP101: Output circuit common TP102: +5 Volt output TP103: +15 Volt output TP104: -15 Volt output
Indicators	DS101: +15 Volt indicator (green) DS102: -15 Volt indicator (green) DS103: +5 Volt indicator (green)
Switches	SW1: power supply ON/OFF switch
Operating Temperature	-20°C to +55°C
Humidity	95% @ +40°C
Isolation	In accordance with ANSI/IEEE C37.90

19.3 THEORY OF OPERATION

Input power is fed through terminals A23-25, C23-25 and A15-17, C15-17. The first circuits provide fusing and EMI suppression.

Diode CR1 protects the power supply form reversal of input voltage. Under such conditions, a fuse on the power supply clears. Inrush limiter TH1 allows charging of capacitor C5 from a stiff dc source without excessive input currents.

The forward converter is designed around PWM integrated circuit U1. The device has an internal clock set by resistor R12 and capacitor C11. Power for the device is initially provided by a series regulator consisting of MOSFET Q3, resistors R2 and R8, and diode CR5. With power applied and internal clock set, pin 11 of U1 goes high causing MOSFET's Q1, Q2, and Q5 to conduct. This causes the dc bus voltage to be applied across windings 1 and 2 of transformer T1 and conduction of output diodes CR9, CR11, and CR14. Upon conduction of these diodes, power flows from the input to the output of the power supply. The dc bus current, which flows through MOSFET's Q1 and Q2 is detected across resistors R5 and R6 and is monitored at pins 3 and 4 of U1. When the peak increases to a level set at pin 7 of U1, pin 11 of U1 is set low causing transistor Q4 to conduct. This drives MOSFET's Q1 and Q2 to an off state. Transformer T1 voltage reverses and diodes CR21, CR9 (opposite device), CR11 (opposite device) conduct and circulate current stored in inductor L3. Inductor L3 and capacitors C24, C26, and C34 form a low pass filter producing a dc that is the half cycle average voltage produced by transformer T1. Inductor L3 is a multi-winding inductor that is matched to transformer T1.

The auxiliary winding of transformer T1, terminals 5 and 4, provides a source of power for the supply's control circuit. After the first few cycles, the voltage at capacitor C17 increase rendering MOSFET Q3 non-conductive.

The secondary auxiliary winding of transformer T1, terminals 3 and 4, capacitor C6, and diode CR2, is a clamp to limit voltage transients across MOSFET's Q1 and Q2.

The 5 Vdc output is unique because its level is monitored across diode CR102, resistors R113 and R115, and potentiometer R114.The wiper arm of potentiometer R114 is fed to pin 6 of dual error amplifier U3 and is compared against an internal reference set at pin 7 of U3. If the 5Vdc output is greater than the reference, pin 14 of U3 goes high causing optical isolator U2 to conduct. This reduces the voltage applied to pin 5 of integrated circuit U1, reduces the peak current through transformer T1, and lowers the output voltage. The negative feedback path is compensated with resistor R110 and C104.

To protect the 5 Vdc output from excessive output currents, the voltage across shunt R122 is monitored between pins 2 and 3 of U3. Like the voltage feedback path, exceeding limits, established by resistors R102 and R103, causes pin 14 to go high and reduces the output voltage.

Integrated circuits U102 and U103 are series regulators which provide post regulation for the secondary outputs. Post regulation is required to meet the voltage regulation requirements of the supply. Feedback for regulator U102 is provided by resistors R117, R118, potentiometer R116, and CR103. Feedback paths for the other regulators are similarly structured.

NOTE

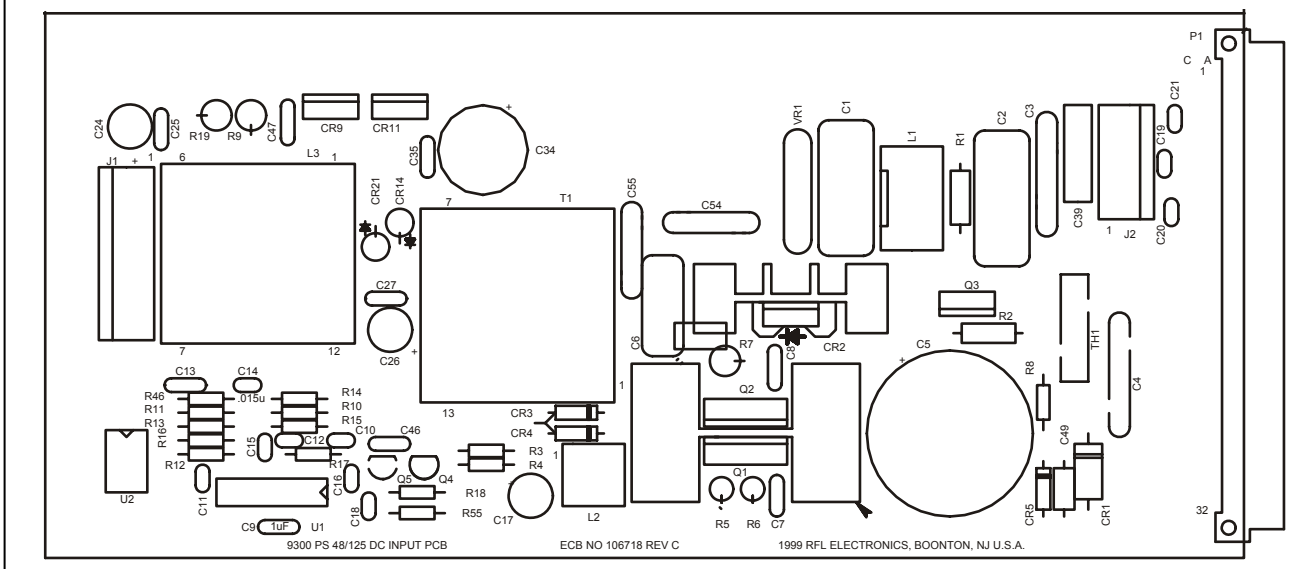
RFL 9300 power supply modules are equipped with several protection circuits. These circuits will cause the module to shut down if its voltage, current, or temperature limits are exceeded. If the power supply has shut down, it can be reset by placing power switch S1 to the OFF position, and then placing it back to the ON position. If it shuts down again, troubleshoot the RFL 9300's chassis to make sure that nothing external to the power supply is causing it to shut down. If nothing is found in the rest of the chassis and the power supply is still shutting down, the power supply may be defective, and should be serviced.

Table 19-2. Replaceable parts, 50-watt power supply module for RFL 9300 Charge Comparison System RFL 48/125 Vdc (Assembly No. 106715-1)

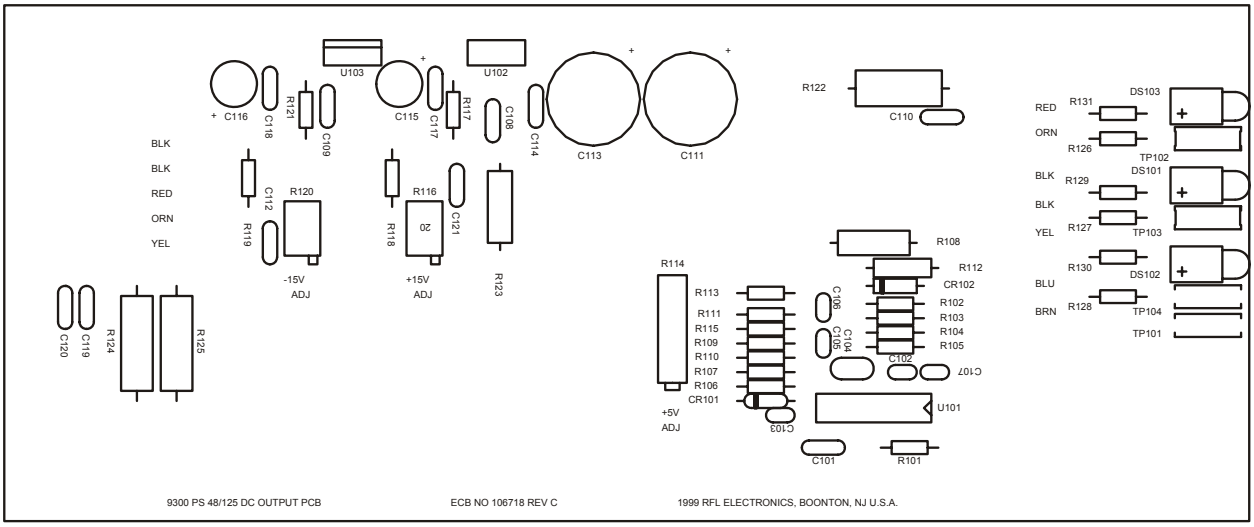
Circuit Symbol (Figs. 19-3 & 19-4)	Description	Part Number
	CAPACITORS	
C1, 2	Capacitor, film, polypropylene, 0.22μF, 20%, 275V	1007 1808
C3, 4	Capacitor, ceramic disc, 0.01μF	1007 1788
C5	Capacitor, electrolytic, 680μF, 20%, 200V	1007 1813
C6	Capacitor, metalized polyester, 1.0μF, 10%, 250V	1007 1809
C7, 9, 25, 27, 35, 13, 46, 101, 108, 109, 110, 112, 114, 117-121	Capacitor, ceramic, 1.0μF, 10%, 50V	0110 6
C8, 47	Capacitor, ceramic disc, 470pF, 10%, 1000V	1007 378
C11	Capacitor, ceramic, 0.0047μF, 10%, 50V	1007 1843
C12	Capacitor, ceramic, 0.022μF, 10%, 100V	1007 1840
C14	Capacitor, ceramic, 0.015μF, 10%, 100V	1007 1839
C15	Capacitor, ceramic, 0.047μF, 10%, 100V	1007 1842
C16, 103, 107, 10, 19, 20, 21	Capacitor, ceramic dip, 0.1μF, 10%, 50V	1007 1667
C18	Capacitor, ceramic dip, 0.033μF, 10%, 50V	1007 1453
C24, 26, 115, 116, 17	Capacitor, electrolytic, 220μF, 20%, 35V	1007 1817
C34, 111, 113	Capacitor, electrolytic, 2200μF, 20%, 10V	1007 1815
C39	Capacitor, suppressor, X2, 0.01μF, 20%, 250VAC	1007 1810
C49	Capacitor, ceramic, 0.1μF, 10%, 100V	0130 11041
C54, 55	Capacitor, ceramic disc, 470pF, 20%, 3KV	1007 1849
C102, 105, 106	Capacitor, ceramic dip, 0.01μF, 10%, 100V	1007 1390
C104	Capacitor, ceramic, 0.47μF, 10%, 50V	1007 1833
	RESISTORS	
R1	Resistor, carbon film, 330K, 5%, 1/2W	0500 6
R2	Resistor, metal film, axial, 1K, 1%, 1/2W	0410 2288
R3, 4	Resistor, fixed composition, 10Ω, 5%, 1/4W	1009 823
R5, 6	Resistor, wirewound, 0.10Ω,1%, 1W	1100 801
R7	Resistor, metal oxide, 10Ω, 5%, 2W	1510 2363
R8	Resistor, metal film, axial, 221K, 1%, 1/4W	0410 1513
R9, 19	Resistor, metal oxide, 100Ω, 5%, 2W	1510 2365
R10	Resistor, metal film, axial, 681Ω, 1%, 1/4W	0410 1272
R11, 13, 14, 16	Resistor, metal film, axial, 10K, 1%, 1/4W	0410 1384
R12	Resistor, metal film, axial, 4.22K, 1%, 1/4W	0410 1348
R15, 46, 104, 105, 106, 115, 126, 127, 128, 129, 130	Resistor, metal film, axial, 1K, 1%, 1/4W	0410 1288
R17, 107	Resistor, metal film, axial, 100Ω, 1%, 1/4W	0410 1192
R18	Resistor, metal film, axial, 82.5Ω, 1%, 1/4W	0410 1184
R55	Resistor, fixed composition, 22Ω, 5%, 1/4W	1009 613
R101, 111	Resistor, metal film, axial, 274Ω, 1%, 1/4W	0410 1234
R102	Resistor, metal film, axial, 33.2Ω, 1%, 1/4W	0410 1146
R103	Resistor, metal film, axial, 3.65K, 1%, 1/4W	0410 1342
R108, 123	Resistor, metal oxide, 56Ω, 5%, 1W	1510 2371
R109	Resistor, metal film, axial, 475Ω, 1%, 1/4W	0410 1257
R110	Resistor, metal film, axial, 4.75K, 1%, 1/4W	0410 1353
R112	Resistor, metal film, axial, 100Ω, 1%, 1/2W	0410 2192

Table 19-2 continued. Replaceable parts, 50-watt power supply module for RFL 9300 Charge Comparison System

Circuit Symbol (Figs. 19-3 & 19-4)	Description	Part Number
	RESISTORS – continued.	
R113	Resistor, metal film, axial, 953Ω, 1%, 1/4W	0410 1286
R114	Resistor, metal film, variable, 100Ω, 10%, 3/4W	46901
R116, 120	Resistor, metal film, variable, 20Ω, 20%, 1/2W	97032
R117, 121	Resistor, metal film, axial, 118Ω, 1%, 1/4W	0410 1199
R118, 119	Resistor, metal film, axial, 1.4K, 1%, 1/4W	0410 1302
R122	Resistor, wirewound, 0.01Ω,1%, 3W	1100 840
R124, 125	Resistor, metal oxide, 1K, 5%, 2W	1510 2368
R131	Resistor, metal film, axial, 221Ω, 1%, 1/4W	0410 1225
	SEMICONDUCTORS	
CR1	Diode, rectifier, silicon, 3A, 1N5406	101716
CR2	Diode, rectifier, ultrafast, MUR8100E	105011
CR3, 4	Diode, fast recovery, 1A, 400V	103484
CR5	Diode, Zener, 15V, 1.5W, 1N5929A	30053
CR9	Diode, rectifier, ultrafast	105416
CR11	Diode, rectifier, Schottky, 20A, 100V	105422
CR14, 21	Diode, rectifier, ultrafast, 4A, 600V	105424
CR101	Diode, general purpose, 1N4148	101778
CR102	Diode, Schottky, 1A, 40V, 1N5819	103382
Q1, 2	Transistor, MOSFET, N-CH, IRFP360	0715 38
Q3	Transistor, FET, N-CH, IRF610	0715 39
Q4	Transistor, silicon, PNP, medium power	103384
Q5	Transistor, silicon, NPN, medium power	105421
U1	Integrated circuit, linear, current mode, PWM	0620 32
U2	Optocoupler, HCNW136	105041
U101	Integrated circuit, linear, mag amp controller	0620 370
U102	Integrated circuit, linear, voltage regulator, positive, 3-terminal	0620 207
U103	Integrated circuit, linear, voltage regulator, negative, 3-terminal	0620 333
VR1	Suppressor, varistor, V130LC20B	41079
	MISCELLANEOUS COMPONENTS	
DS101, 102, 103	Opto device, LED, green	101780
F1	Fuse, 4A, 250V, SLO-BLO	301122
J1	Connector, wafer assembly, 8-circuit	45142 8
J2	Connector, wafer assembly, 5-circuit	45142 5
L1	Choke, C-mode, 3mH, 1.8Adc	105426
L2	Choke, bias, 20mH, 50mAdc	105428
L3	Choke, multi output, 38-150V	103887
P1	Connector, JK male, 64 contact, DIN	98457
SW1	Switch, rocker, SPST	30441 1
TH1	Thermistor, NTC, 2.5 Ohm @ 25 Deg C	103370
TP101	Test point, black, PC mount	38116 3
TP102	Test point, green, PC mount	38116 5
TP103	Test point, red, PC mount	38116 2
TP104	Test point, yellow, PC mount	38116 8



a. Input board



b. Output board

Figure 19-2. Component locator drawings, 50-watt power supply module (ECB Drawing No. 106718-C)

Figure 19-3. 9300 PS 48/125 DC power supply module for RFL 9300 Charge Comparison System, (Assembly No. 106715-1; Schematic No. 106719-E)

Please see Figure 19-3, in Section 32: Schematics

This page intentionally left blank

SECTION 20: RELAY I/O MODULE

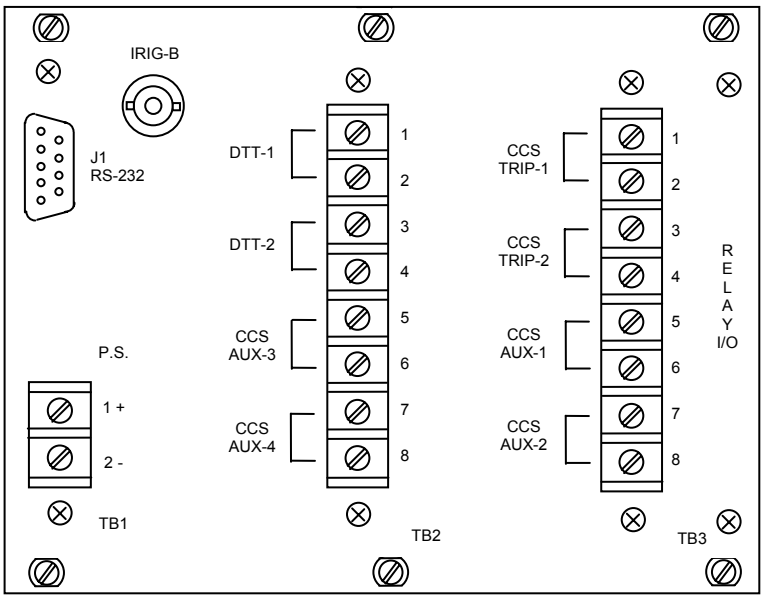


Figure 20-1. RFL 93B Relay I/O Module, rear panel

20.1 DESCRIPTION

The RFL 93B Relay I/O Module provides customer connections for the DTT and CCS trip output functions. Each output is the normally-open contact sets of a high-speed relay that is internally energized with station battery voltage. The RFL 93B Relay I/O Module consists of a rear panel assembly (Figure 20-1) and three subassembly boards which are described below:

1.	Power/RS-232 board.	(series 100 components)	Assy. No. 106388-1
2.	Current Sense board.	(series 200 components)	Assy. No. 106388-2
3.	Relay Output board.	(series 1-99 components)	Assy. No. 106388-3

20.2 CONTROLS AND INDICATORS

Figure 20-2 shows the location of all rear-panel connectors and terminal blocks on the RFL 93B Relay I/O module. All of these connectors and terminal blocks are accessible with the Relay I/O Module installed in the chassis. Figure 20-3 shows the location of all controls and indicators on the Power/RS-232 board. These controls and indicators are only accessible when the Relay I/O Module is removed from the chassis, or is placed on a card extender. The Current Sense board and the Relay Output board do not have controls and indicators and therefore are not included under this heading.

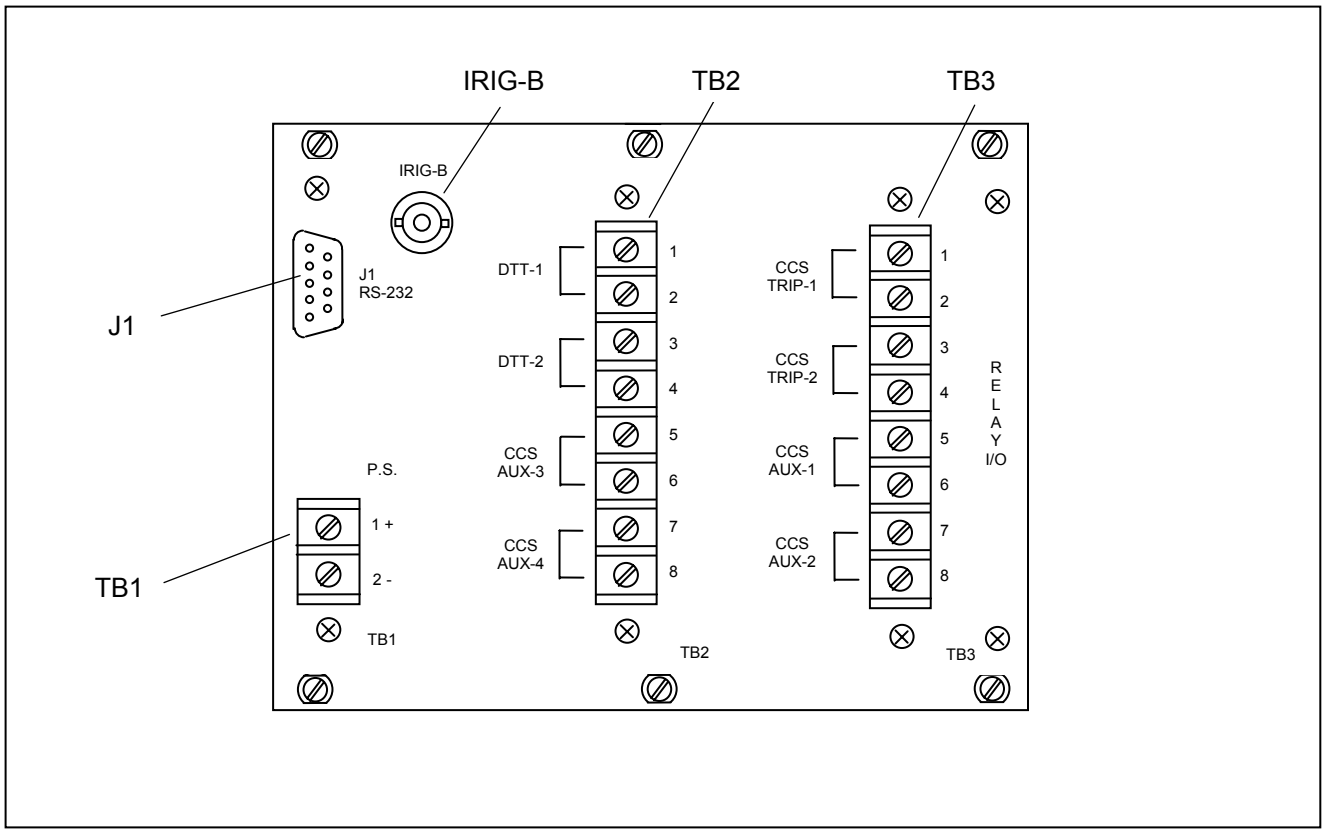


Figure 20-2. Rear panel connectors and terminal blocks, RFL 93B Relay I/O Module

20.2.1 REAR PANEL CONNECTORS AND TERMINAL BLOCKS (See Figure 20-2)

J1 9-pin D-subminiature (DE-9) connector for RS-232 interface (future enhancement).

IRIG-B BNC connector for IRIG-B input.

TB1 Input Power:

TB1-1	Station Battery +
TB1-2	Station Battery -

TB2 DTT Output Connections:

TB2-1 and TB2-2	DTT-1
TB2-3 and TB2-4	DTT-2

CCS Output Connections:

TB2-5 and TB2-6	CCS AUX-3
TB2-7 and TB2-8	CCS AUX-4

TB3 CCS Output Connections:

TB2-1 and TB2-2	CCS TRIP-1
TB2-3 and TB2-4	CCS TRIP-2
TB2-5 and TB2-6	CCS AUX-1
TB2-7 and TB2-8	CCS AUX-2

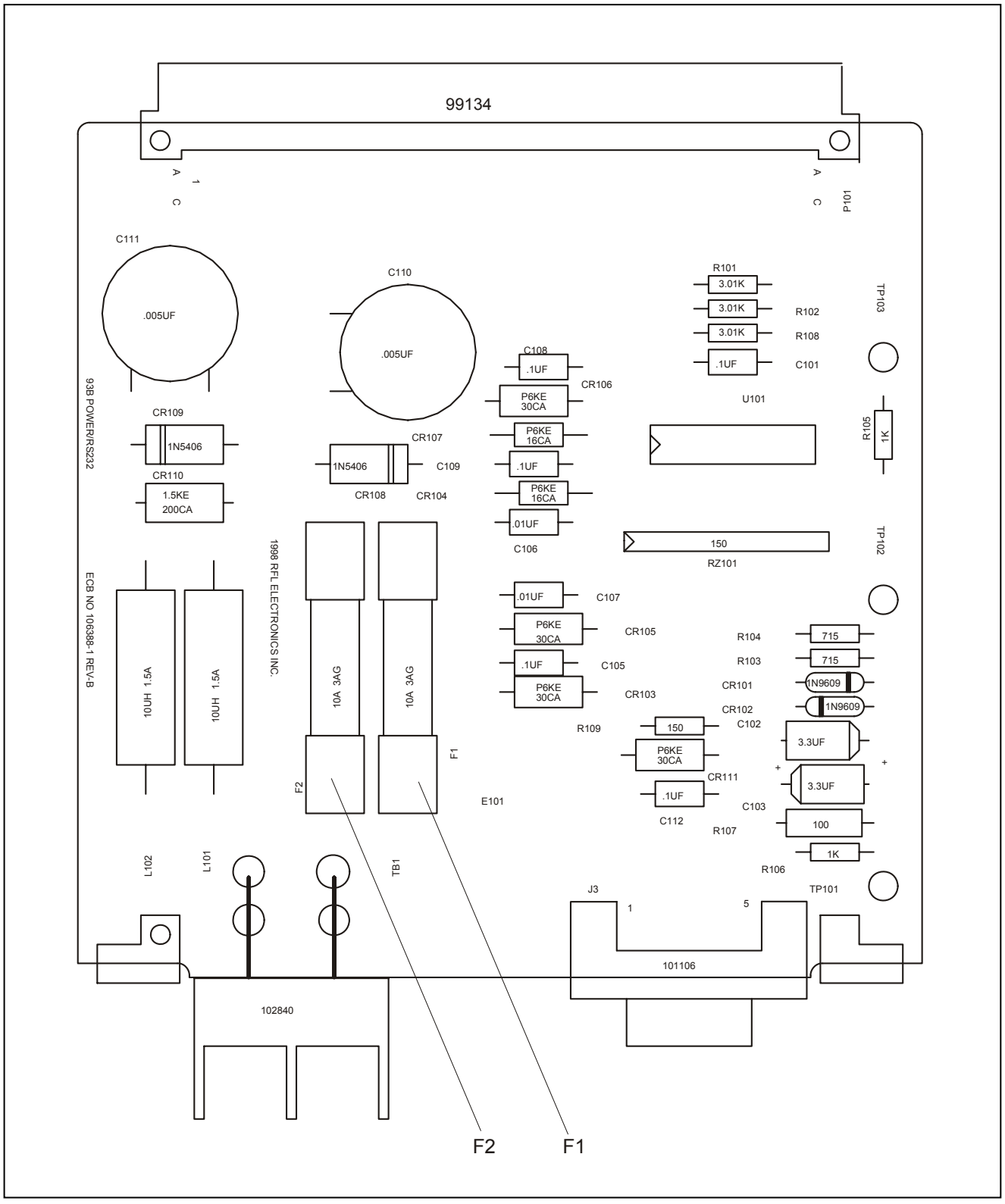


Figure 20-3. Controls and indicators, power/RF-232 board for RFL 93B Relay I/O Module

20.2.2 POWER/RS-232 BOARD (See Figure 20-3)

F1, F2 Input fuses; See Table 20-2 for replacement part numbers.

TP101 Monitoring point for RS-232 port +V supply.

TP102 Monitoring point for RS-232 port -V supply.

TP103 Ground reference.

20.3 THEORY OF OPERATION

The DTT outputs on terminal block TB2 are activated when a DTT input appears at the remote terminal. The DTT RX trip command is issued by the RFL 93B SV Supervisor Controller to the Relay I/O as the DTT TRIP signal.

The CCS outputs on terminal block TB3 are the result of a trip decision based on the currents applied to the relays. This trip function originates in each individual phase controller module as an X_3PT signal sent to the test board in the display module. These signals are combined to form the TRIP signal.

When a low TRIP RELAY ENABLE signal is received from the display module's oscillography board, the RFL 9300's trip output circuits are enabled. A low trip command signal will energize the coil of the corresponding high-speed relays. A trip confirmation signal (TRIP LATCH or DTT LATCH) derived directly from the voltage applied to the coil is fed back to the oscillography board. On the oscillography board, a logic circuit creates a latch condition for which the relay remains energized after the trip command signal ceases. This performs the "make" operation of the trip function. The contact circuits are not required to "break" the trip coil (52TC) current, because this is done by the breaker's 52a contacts. The relay will not release until it is detected that the breaker coil current has stopped.

The current sense board detects and generates a status signal of the 52TC current. The current sense feature exists on only two of the contact sets available in each output, so there are two sense signals per trip function. When current is detected through the contact set, the corresponding "sense" signal goes low and is latched on the oscillography board to be read by the Display Controller. To release the relay, the Display Controller issues a TRIP LATCH DISABLE or DTT LATCH DISABLE signal. This squelches the latch feedback, and opens the loop.

The customer connections for station battery are also located on the Relay I/O (TB1). It is first fused and then distributed to the system power supply module (Section 19) and trip circuits. An RS-232 port is provided by 9-pin D-subminiature (DB-9) connector J3 for remote programming and monitoring,

20.3.1 POWER/RS-232 BOARD

The power/RS-232 board provides connections for station battery input to the RFL 9300. It also provides a connector for an RS-232 port. The components on the power/RS-232 board have circuit reference numbers between 101 and 199.

20.3.1.1 STATION BATTERY INPUT

One of the functions of the power/RS-232 board is to provide connections for station battery input. Station battery voltage is used for the tripping circuits and the power supply input. Fuses F1 and F2 disable the entire system, not just the trip circuits, should a severe component malfunction occur. Transient filtering of the station battery voltage is provided by LC filters formed from inductors L101 and L102, and capacitors C110 and C111. CR110 provides transient overvoltage protection, and reverse polarity protection is provided by CR108 and CR109. After filtering, this voltage is supplied to the motherboard through connector P101.

20.3.1.2 RS-232 COMMUNICATION PORT

There are provisions for an RS-232 port at 9-pin D-subminiature (DB-9) connector J3. U101 converts input signals from 12-volt to 5-volt logic, and output signals from 5-volt to 12-volt logic. The 12-volt supplies required by U101 are generated by Zener-regulated supplies formed by resistors R103 through R106, capacitors C102 and C103, and Zener diodes CR101 and CR102. The communication lines are protected by RC filters formed from resistor network RZ101, resistor R109, and capacitors C105 through C109 and C112. Transorbs CR103 through CR107 and CR111 provide transient overvoltage protection.

20.3.2 CURRENT SENSE BOARD

The current sense board translates logic-level signals into relay drive signals. It also routes many signal lines between the current sense board and the relay output board, and provides other interface functions. The components on the current sense board have circuit reference numbers between 201 and 299. Interfacing to the relay output board is through connectors P202 and P203.

20.3.2.1 TRIP ENABLE FUNCTION

During power-up sequences and system test modes, the RFL 9300's trip outputs must be disabled. The TRIP RELAY ENABLE signal from the oscillography board in the display module controls this function. When this line is high, the outputs of U203 tri-state. Tripping is further inhibited during power-up by the normally-open contacts of relay K201 that opens the 15V supply of the high-speed relays. A low enable signal, and system power, must be present to turn on K201. The normally-closed contacts of K201 generate a confirmation signal (TRIP DISABLE LED). Current from the 15V supply is limited by R220 and is used to activate the LED in optocoupler U207. U207's output phototransistor pulls the line low and lights the PROTECTION DISABLED indicator on the display controller in the display module. When TRIP RELAY ENABLE is low, the same output of U203 is enabled to turn on PNP transistor Q201. This supplies base current to transistor Q202, which is normally reverse-biased. Q202 turns on conducting current from the -15-volt supply to energize K201. The normally-open relay contacts will close, and providing a +15V supply for the coil circuits of both the TRIP and DTT relays.

20.3.2.2 TRIP AND DTT FUNCTION

With the TRIP RELAY ENABLE signal low U203 is transparent to circuit operation other than for buffering and edge shaping. When the AUX_TRIP line goes low the signal goes through U202 where it is inverted and then routed into U204. U204 is a darlington transistor relay driver. Two identical circuits in U204 are paralleled for increased reliability. The output from U204 provides a return path for the relay drive current supplied through K201. Relays K203 through 206 on the current sense board are activated, as are relays K1 and K2 on the relay output board. The DTT output is similar with only relays K7 and K8 on the relay output board being activated.

20.3.2.3 TRIP LATCH AND DTT LATCH FUNCTION

The current flowing through TRIP COIL1 and DTT COIL 1 goes through Optoisolators U206 and U205 respectively. The output of these isolators goes high when current is flowing. These signals go into AND gates inside U202. Assuming the latch disable signals are high, the output signals of these gates are fed back to the oscillography board to latch the trip or DTT signal.

20.3.2.4 TRIP LATCH AND DTT LATCH DISABLE FUNCTION

In order to terminate a trip condition, the display controller issues a 10 ms active low TRIP LATCH DISABLE or DTT LATCH DISABLE signal. These signals force the latch signals from U202 to go high. As long as there is no trip command, the relay is released.

20.3.2.5 CURRENT SENSE FUNCTION

The relay output board has 4 current sense relays on it. The relay coils are in series with the output contacts. When the contact is closed and current is in the range of 150 to 250 ma, the sense relay contacts will close. One side of all four contacts is tied to +5V. The 5V current sense signals flow to the current sense board. The signals are filtered to remove noise and the edges are squared using U201 Schmitt trigger inverter. These sense signals are used by the display controller to light the indicators and maintain the trip relay output until the contact current drops below the set point.

20.3.3 RELAY OUTPUT BOARD

The RELAY OUTPUT BOARD contains 4 trip relays and 4 current sense relays. Along with 4 more trip relays on the CURRENT SENSE BOARD, they provide for 6 form A, CCS Trip contacts and 2 form A, DTT Trip contacts. The outputs of the relays are protected with surge withstanding capacitors. The relay board also provides a BNC connector for IRIG-B input. Surge withstanding components allow this input to survive 8 KV ESD discharges.

Table 20-1. Replaceable parts, RFL 93B Relay I/O, Power/RS-232 board (Assembly No. 106388-1)

Circuit Symbol (Figs. 20-4 & 20-7)	Description	Part Number
	CAPACITORS	
C101,105,108,109,112	Capacitor,ceramic,0.1uf,10%,100V	0130 11041
C102,103	Capacitor,tantalum,3.3uf,20%,35V	1007 1260
C106,107	Capacitor,ceramic,0.01uf,10%,100V	0130 11031
C110,111	Capacitor,ceramic disc,0.005uf,20%,3KV	1007 1264
	RESISTORS	
R101,102,108	Resistor,metal film,axial,3.01K,1%,1/4W	0410 1334
R103,104	Resistor,metal film,axial,715Ω,1%,1/4W	0410 1274
R105,106	Resistor,metal film,axial,1K,1%,1/4W	0410 1288
R107	Resistor,metal film,axial,100Ω,1%,1/2W	0410 2192
R109	Resistor,metal film,axial, 150Ω,1%,1/4W	0410 1209
RZ101	Resistor,network,150Ω,5R/PKG,SIP	100571
	SEMICONDUCTORS	
CR101,102	Diode,Zener,silicon,9.1V,1N960B	41014
CR103,105,106,111	Suppressor,transient,voltage,P6KE30CA	100567
CR104,107	Suppressor,transient,voltage,P6KE16CA	100572
CR108,109	Diode,rectifier,silicon,3A,1N5406	101716
CR110	Suppressor,transient,voltage,1.5KE200CA	30266
	MISCELLANEOUS COMPONENTS	
F1,2	Fuse,10A,3AG,250V,normal-blow	44395 010
J3	Connector, JK male,9P,RT angle	101106
L101,102	Inductor,10μH,5%,1.5A max	30285
P101	Connector,plug,female,64 cont,DIN	99134
TP101,102,103	Test point,terminal,orange	98441

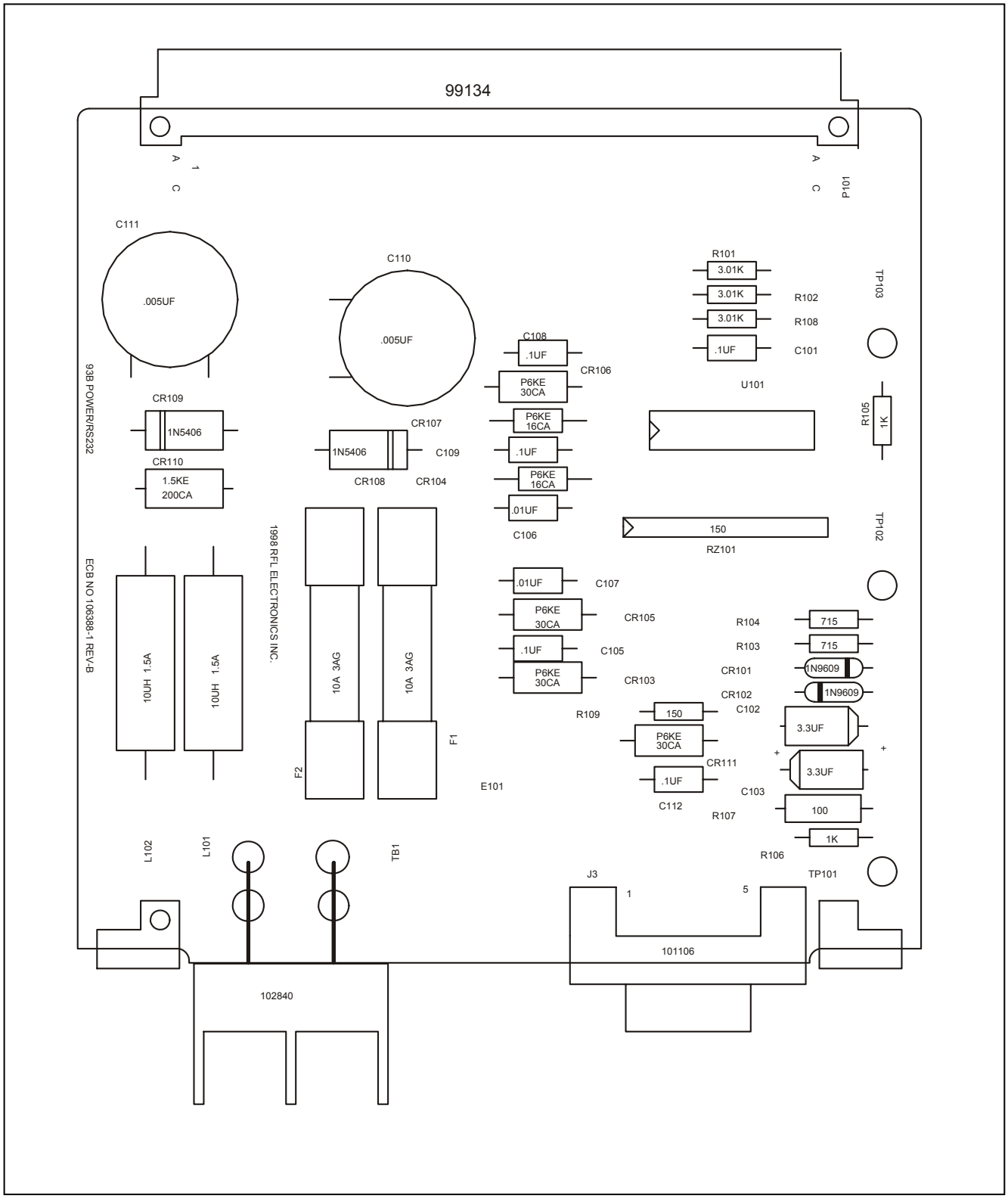


Figure 20-4. Component locator drawing, RFL 93B Relay I/O module, Power/RS-232 board

Table 20-2. Replaceable parts, RFL 93 Relay I/O module, Current Sense board (Assembly No. 106388-2)

Circuit Symbol (Figs. 20-5 & 20-7)	Description	Part Number
	CAPACITORS	
C201-204	Capacitor,ceramic,0.1μF,10%,50V	0120 38
C205	Capacitor,tantalum,10μF,20%,25V	1007 1563
C206,208,210	Capacitor,ceramic,0.1μF,10%,100V	0130 11041
C207	Capacitor,electrolytic,200μF,-10+75%,25V	1007 900
C209	Capacitor,electrolytic,47μF,20%,35V	1007 1578
	RESISTORS	
R201-208	Resistor,metal film,axial,5.11KΩ,1%,1/4W	0410 1356
R209,218	Resistor,metal film,axial,10K,1%,1/4W	0410 1384
R210,211,212,213	Resistor,metal film,axial,69.8Ω,1%,1/4W	0410 1177
R214	Resistor,metal film,axial,6.81K,1%,1/4W	0410 1368
R215	Resistor,metal film,axial,3.16K,1%,1/4W	0410 1336
R216	Resistor,metal film,axial,3.01K,1%,1/4W	0410 1334
R217,219	Resistor,metal film,axial,5.11K,1%,1/4W	0410 1362
R220	Resistor,metal film,axial,1K,1%,1/4W	0410 1288
RZ201	Resistor network,10K,9R/PKG,SIP	32200
	SEMICONDUCTORS	
CR201,203,204	Diode,silicon,rectifier,1 Amp,1N4003	30769
Q201	Transistor,silicon,PNP,2N3906	21565
Q202	Transistor,NPN,40V,2N4401	42574
U201	Integrated circuit,MOS,Hex inverter,Schmitt trigger	0615 242
U202	Integrated circuit,MOS,QUAD 2-input NAND gate	0615 159
U203	Integrated circuit,MOS,Octal D-latch	0615 308
U204	Transistor array,ULN2803A	0720 7
U205,206,207	Opto device,photo,ISO,4N35	47104
	MISCELLANEOUS COMPONENTS	
K201	Relay,SPDT,12V,PCB,sealed	101236
K203,204,205,206	Relay,SPDT,12VDC,37.5MA,SPCL	102860
L1	Inductor,axial,47μH,15%,1.6A	105411
P201	Connector,plug,female,64cont,DIN	99134
P202	Connector, wafer assembly,12 CKT	42082 12
P203	Connector, JK male,16P,vertical	30202

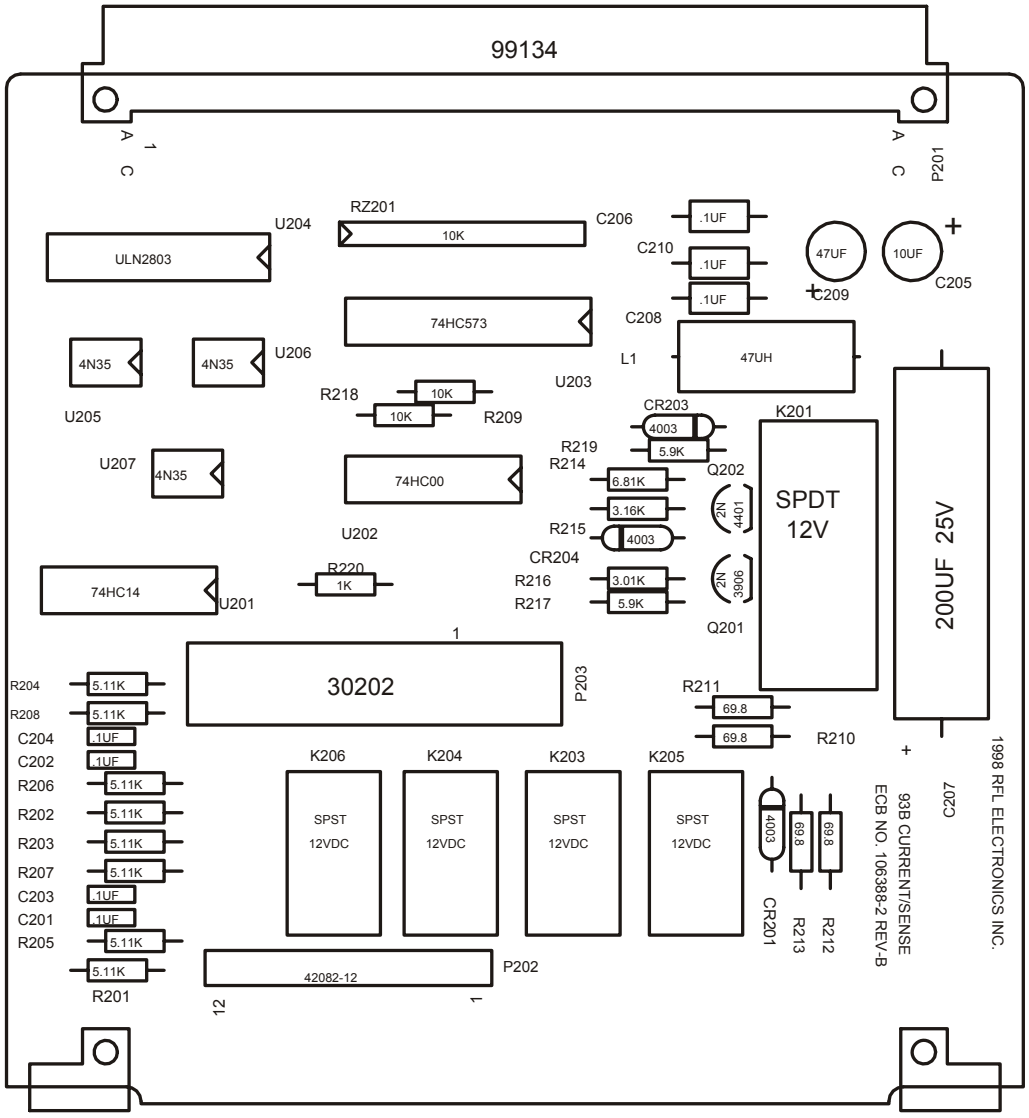


Figure 20-5. Component locator drawing, RFL 93B Relay I/O module, Current Sense Board

Table 20-3. Replaceable parts, RFL 93 Relay I/O module, Relay Output board (Assembly No. 106388-3)

Circuit Symbol (Figs. 20-6 & 20-7)	Description	Part Number
	CAPACITORS	
C1-16	Capacitor, ceramic disc,0.005μF,20%,3KV	1007 1264
C17,18,19	Capacitor, 0.01μF,10%,100V	0130 11031
	RESISTORS	
R1,3	Resistor, metal film,axial,23.7Ω,1%,1/4W	0410 1132
R2,4	Resistor, metal film,axial,69.8Ω,1%,1/4W	0410 1177
	SEMICONDUCTORS	
CR1,2,3,4	Diode, silicon, rectifier,1 Amp,1N4003	30769
CR5,6	Suppressor, transient,voltage,P6KE16CA	100572
CR7,8	Suppressor, transient,voltage,1.5KE400CA	30442
	MISCELLANEOUS COMPONENTS	
J1	Connector assembly, C board,12 circuit, right angle	43173 12
J2	Connector,S.H.E.,16-pin	90223
K1,2,7,8	Relay, SPST, 12VDC, 37.5 MA	102860
K9,10,11,12	Realy, reed, SPST, 100V, 250MA	102859
T1	Transformer, modem matching	95595
TB2,3	Block terminal, 8 terminal, 7/16 center	102839

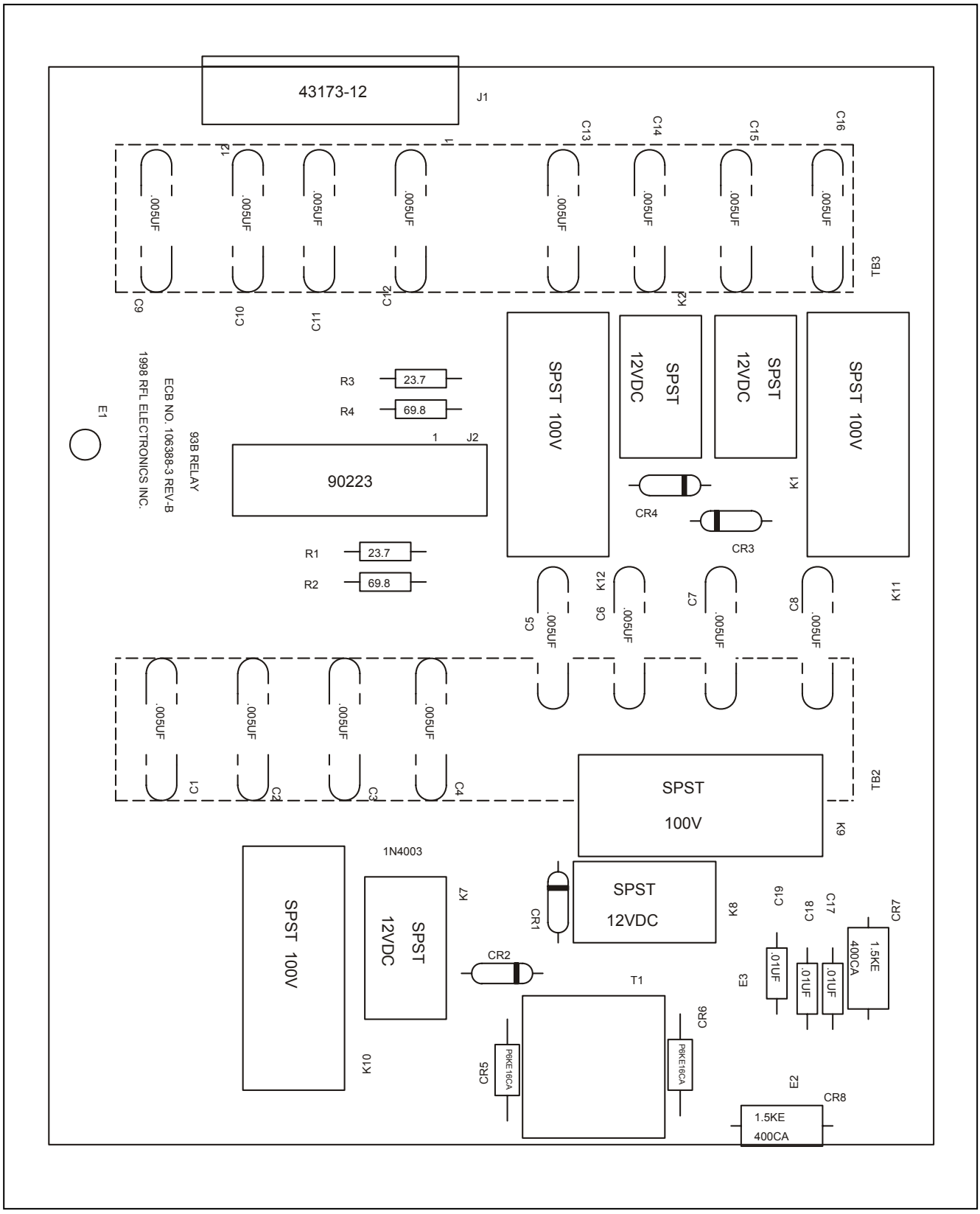


Figure 20-6. Component locator drawing, RFL 93B Relay I/O module, Relay Output board

Figure 20-7. RFL 93B RELAY I/O module, Power/RS-232 board (Assembly No. 106388-1; Schematic No. D-106389, Rev. D) Sheets 1 of 3 through 3 of 3

Please see Figure 20-7, Sheets 1 of 3 through 3 of 3, in Section 32: Schematics

This page intentionally left blank

SECTION 21. ALARM I/O MODULE

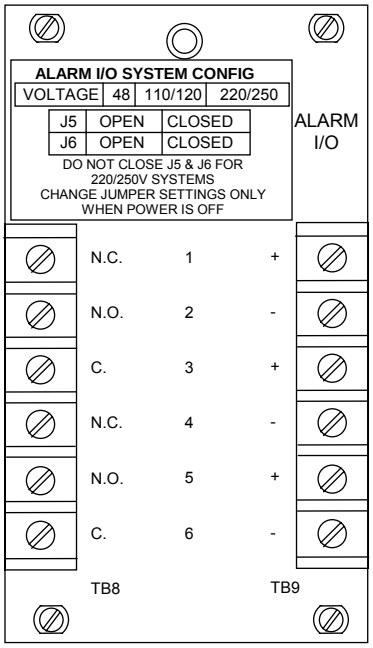


Figure 21-1. RFL 93 Alarm I/O Module

21.1 DESCRIPTION

The RFL 93 Alarm I/O Module (Fig. 21-1) is an interface module mounted at the rear of all RFL 9300 units. It provides connections for DTT input, 89B disconnect switch input, reclose block output, and alarm relay outputs. There are three types of RFL 93 Alarm I/O modules as follows:

Assembly No.	Nomenclature	Application
104775-5	93 Alarm I/O	Operates on 48V, 125V or 250V
104775-6	93 Alarm I/O (24V)	Operates on 24V only
104775-7	93 Alarm I/O (48/110/220)	Operates on 48V, 110V or 220V

21.2 CONTROLS AND INDICATORS

The controls and indicators on the 104775-5 and 104775-7 modules consist of two terminal blocks (TB8 and TB9) and six jumpers (J1 to J6). The controls and indicators on the 104775-6 module consist of two terminal blocks (TB8 and TB9) and two jumpers (J5 and J6). These controls and indicators are described below. The terminal blocks are mounted on the rear panel, and are accessible with the RFL 93 Alarm I/O installed in the RFL 9300 chassis. The jumpers can only be accessed with the Alarm I/O module removed from the chassis. The location of the terminal blocks and jumpers is shown in Figure 21-2.

>> text continues on page 21-3 <<

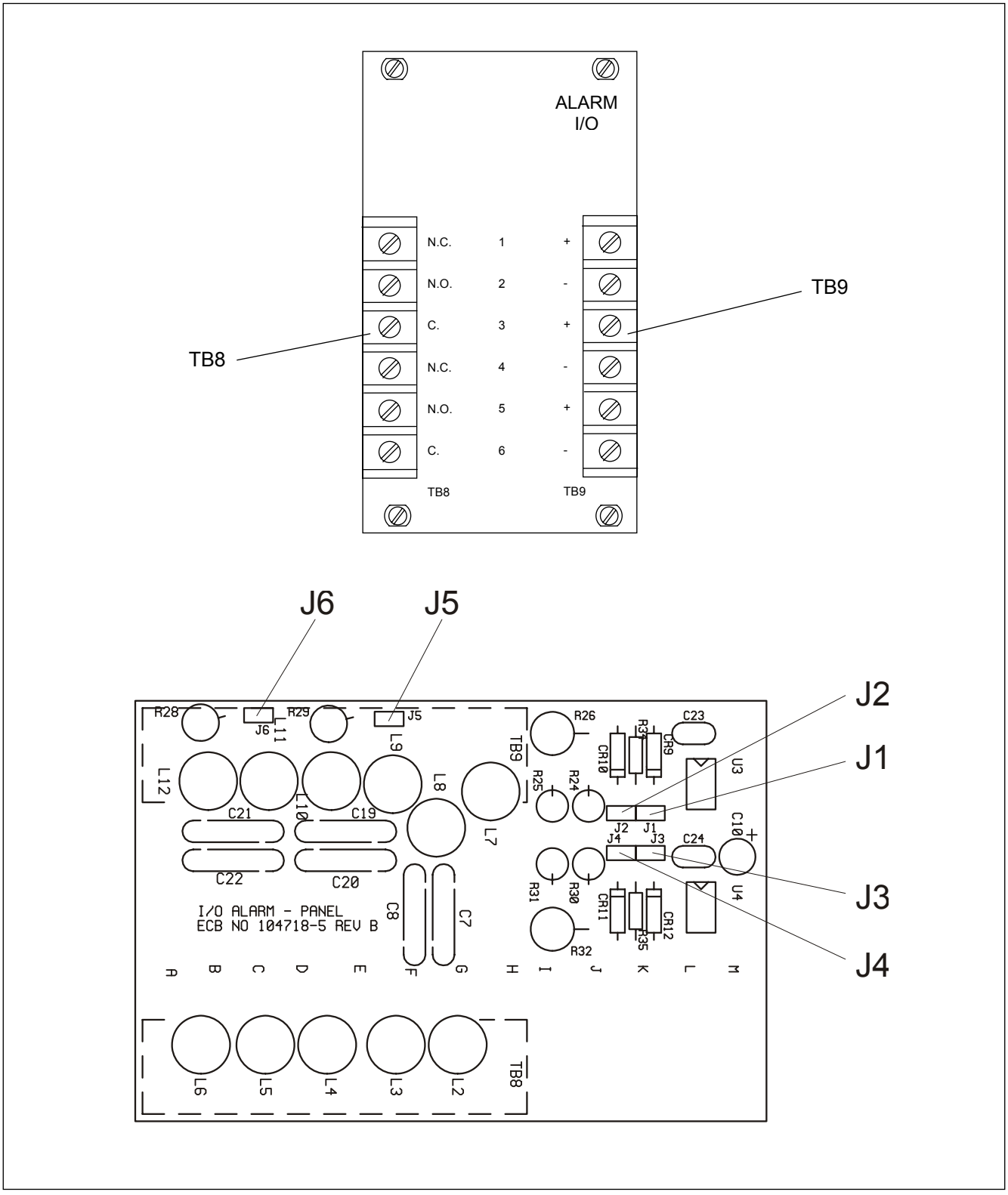


Figure 21-2. Controls and indicators, RFL 93 Alarm I/O Module

TERMINAL BLOCK OUTPUT CONNECTIONS:

ALARM OUTPUTS:

TB8-1 LOCAL ALARM N.C.
TB8-2 LOCAL ALARM N.O.
TB8-3 LOCAL ALARM COM
TB8-4 COMM ALARM N.C.
TB8-5 COMM ALARM N.O.
TB8-6 COMM ALARM COM

RECLOSE BLOCK OUTPUTS:

TB9-1 RECLOSE BLOCK +
TB9-2 RECLOSE BLOCK -

TERMINAL BLOCK INPUT CONNECTIONS:

DTT INPUTS:

TB9-3 DTT +
TB9-4 DTT –

89B INPUTS:

TB9-5 89B +
TB9-6 89B –

JUMPERS: J1, J2, J3, J4 (104775-5 only)

With J1 and J3 installed, and with J2 and J4 removed, the module will operate at 48 Volts.

With J2 and J4 installed, and with J1 and J3 removed, the module will operate at 125 Volts.

With J1, J2, J3 and J4 removed, the module will operate at 250 Volts.

JUMPERS: J1, J2, J3, J4 (104775-7 only)

With J1 and J3 installed, and with J2 and J4 removed, the module will operate at 48 Volts.

With J2 and J4 installed, and with J1 and J3 removed, the module will operate at 110 Volts.

With J1, J2, J3 and J4 removed, the module will operate at 220 Volts.

JUMPERS: J5 and J6 (104775-5, 104775-6 and 104775-7)

Used to wet the contacts of circuits that activate the module inputs. These jumpers should not be inserted with station battery voltages in excess of 125 Volts.

21.3 THEORY OF OPERATION

The RFL 93 Alarm I/O Alarm I/O Module provides connections for DTT input, 89B disconnect switch input, reclose block output, and alarm relay outputs.

21.3.1 JUMPERS

The 104775-5 93 Alarm I/O replaces four previous versions of the module. The 93 Alarm I/O contains jumpers that allow programming for the different station voltages that could be present at the DTT and 89B inputs. The jumpers select resistors, which set input thresholds. If J1 and J3 are inserted with the other jumpers removed, the module will operate with a 48V station battery. If J2 and J4 are inserted with the other jumpers removed, the module will operate with a 125V station battery. If jumpers J1, J2, J3 and J4 are removed, the module will operate with a 250V station battery. The module inputs will not turn the module on at 50% of the station voltage, and the module will be on at 80% of the station voltage. When the input voltage is greater than 80% of the station battery U3 or U4 will turn on. This creates a low signal out of U1 on pin 5 or 7.

Additional jumpers are located at the input terminals, J5 and J6. Some end users want to wet the contacts of circuits that activate the module inputs. These jumpers should not be inserted with station battery voltages in excess of 125 Volts.

21.3.2 RECLOSE BLOCK OUTPUT

The reclose block output is closed when /reclose on P9 A2 goes low. This biases Q3 on which turns on the optical FET switch U2. Pins 6 and 4 are shorted to pin 5 of U2 when pin 2 is low. The optical isolated FET U2 then in turn biases Q4 on and the reclose block output presents a low impedance. Q4 requires current from the external load to fully turn on. If the load is very small, the primary current path will be through R18, U2 and the base to emitter junction of Q4. As the load increases and more current flows through the circuit, Q4 is biased on. The maximum voltage between TB9 1 and 2 while the circuit is active should be 1.5 volts or less. The circuit can work with up to 1 ampere of load current when turned on and can block an external voltage of 350 volts when turned off. This allows one module to work with a 48, 125 or 250 Volt station battery. No jumper changes are required.

21.3.3 ALARM RELAY OUTPUT

Two alarm relays are also present in the 93 Alarm I/O. If the local alarm or the com alarm connections at P9 A5 or A4 go low, Q5 or Q6 is biased on. This turns on Q1 or Q2 which actives the alarm relay.

Table 21-1. Replaceable parts, RFL 93 Alarm I/O Module.
Assembly No. 104775-5

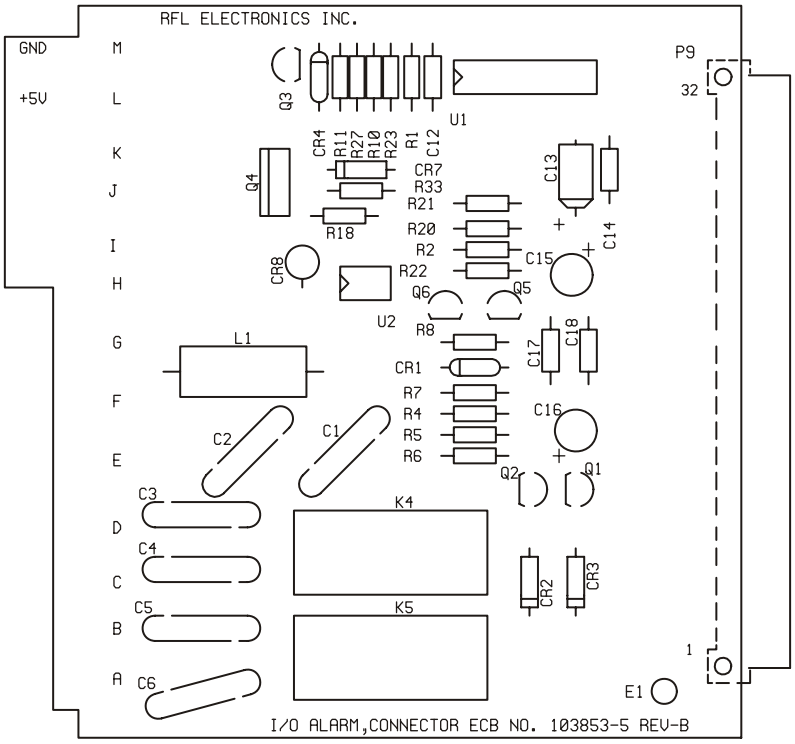
Circuit Symbol (Figs. 21-3 & 21-4)	Description	Part Number
	CAPACITORS	
C1-6	Capacitor, ceramic disc, 0.005μF, 20%, 3kV	1007 1264
C7, 8, 19-22	Capacitor, ceramic disc, 0.005μF, 20%, 3kV	1007 1264
C10	Capacitor, tantalum, 1μF, 20%, 35V	1007 496
C12, 14, 17, 18	Capacitor, ceramic, 0.1μF, 10%, 50V	0130 51041
C13	Capacitor, tantalum, 33μF, 10%, 10V, axial	1007 1142
C15, 16	Capacitor, electrolytic, 47μF, 20%, 35V	1007 1578
C23, 24	Capacitor, ceramic dip, 0.01μF, 5%, 100V	1007 1645
	RESISTORS	
R1, 2, 4, 8, 11	Resistor, metal film, axial, 1K, 1%, 1/4W	0410 1288
R5	Resistor, metal film, axial, 2.61K, 1%, 1/4W	0410 1328
R6, 7	Resistor, metal film, axial, 3.16K, 1%, 1/4W	0410 1336
R10	Resistor, metal film, axial, 10K, 1%, 1/4W	0410 1384
R18	Resistor, metal film, axial, 619Ω, 1%, 1/4W	0410 1268
R20, 22	Resistor, metal film, axial, 3.01K, 1%, 1/4W	0410 1334
R21, 23	Resistor, metal film, axial, 5.9K, 1%, 1/4W	0410 1362
R24, 30	Resistor, metal film, 43K, 2%, 2W	1510 2374
R25, 31	Resistor, metal film, 27K, 2%, 2W	1510 2373
R26, 32	Resistor, wirewound, 5K, 5%, 3.25W	1100 460
R27	Resistor, metal film, axial, 332Ω, 1%, 1/4W	0410 1242
R28, 29	Resistor, wirewound, 25K, 5%, 3W	1100 833
R33	Resistor, metal film, axial, 31.6K, 1%, 1/4W	0410 1432
R34, 35	Resistor, metal film, axial, 12.1K, 1%, 1/4W	0410 1392
	SEMICONDUCTORS	
CR1, 4	Diode, silicon, 1N914B/1N4448	26482
CR2, 3	Diode, silicon, rectifier, 1Amp, 1N4003	30769
CR7	Rectifier, avalanch, 600V, 1A, 1N4005	26935
CR8	Suppressor, transient voltage, 1.5KE350CA	101722
CR9, CR11	Diode, Zener, 20V, 5%, 1W, 1N4747A	20794
CR10, 12	Diode, silicon, rectifier, 1Amp, 1N4003	30769
Q1-3	Transistor, NPN, 40V, 2N4401	42574
Q4	Transistor, silicon, NPN, 700V, 5A	102870
Q5, 6	Transistor, silicon, PNP, 2N3906	21565
U1	Integrated Circuit, MOS, tri-state buffer	0615 290
U2	Switch, solid state	102842
U3, 4	Opto device, iso-coupler, MOC8021	90271
	MISCELLANEOUS COMPONENTS	
J1-6	Connector, header, single, 2 ckt	32802 2
K4, 5	Relay, SPDT, 12V, PCB, sealed	101236
L1	Inductor, 10μH, 5%, 1.5A max	30285
L2-12	Inductor, 10μH, 5%, 1.5A max	102698
TB8, 9	Terminal block, 6 terminal	101233

Table 21-2. Replaceable parts, RFL 93 Alarm I/O Module.
Assembly No. 104775-6 and 104775-7

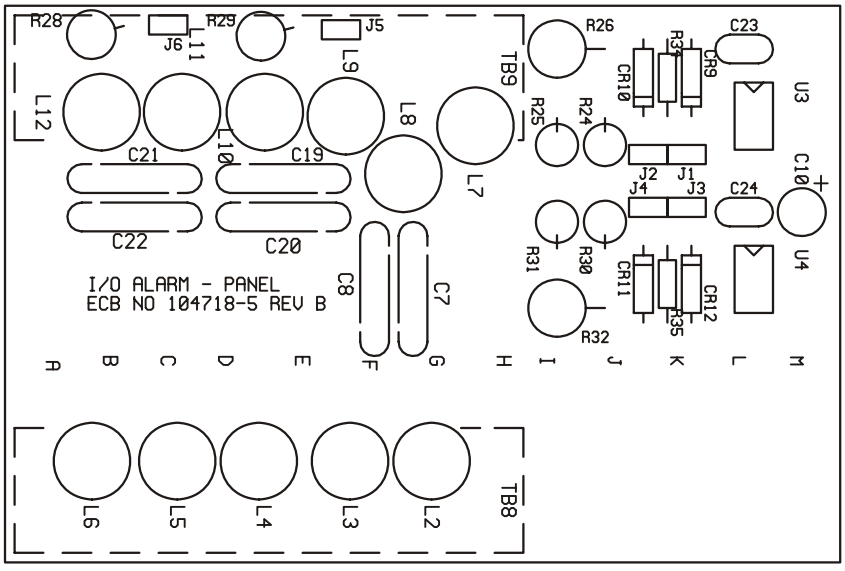
Circuit Symbol (Figs. 21-3 & 21-4)	Description	Part Number
	CAPACITORS	
C1-6	Capacitor, ceramic disc, 0.005μF, 20%, 3kV	1007 1264
C7, 8, 19-22	Capacitor, ceramic disc, 0.005μF, 20%, 3kV	1007 1264
C10	Capacitor, tantalum, 1μF, 20%, 35V	1007 496
C12, 14, 17, 18	Capacitor, ceramic, 0.1μF, 10%, 50V	0130 51041
C13	Capacitor, tantalum, 33μF, 10%, 10V, axial	1007 1142
C15, 16	Capacitor, electrolytic, 47μF, 20%, 35V	1007 1578
C23, 24	Capacitor, ceramic dip, 0.01μF, 5%, 100V	1007 1645
	RESISTORS	
R1, 2, 4, 8, 11	Resistor, metal film, axial, 1K, 1%, 1/4W	0410 1288
R5	Resistor, metal film, axial, 2.61K, 1%, 1/4W	0410 1328
R6, 7	Resistor, metal film, axial, 3.16K, 1%, 1/4W	0410 1336
R10	Resistor, metal film, axial, 10K, 1%, 1/4W	0410 1384
R18	Resistor, metal film, axial, 619Ω, 1%, 1/4W	0410 1268
R20, 22	Resistor, metal film, axial, 3.01K, 1%, 1/4W	0410 1334
R21, 23	Resistor, metal film, axial, 5.9K, 1%, 1/4W	0410 1362
R24, 30	Resistor, metal film, axial	
	104775-6 = not used	NA
	104775-7 = 43K, 2%, 2W	1510-2374
R25, 31	Resistor, metal film, axial	
	104775-6 = not used	NA
	104775-7 = 27K, 2%, 2W	1510-2373
R26, 32	Resistor, wirewound	
	104775-6 = 2.5K, 5%, 3.25W	1100-329
	104775-7 = 5K, 5%, 3.25W	1100-460
R27	Resistor, metal film, axial, 332Ω, 1%, 1/4W	0410 1242
R28, 29	Resistor, wirewound, 25K, 5%, 3W	1100 833
R33	Resistor, metal film, axial, 31.6K, 1%, 1/4W	0410 1432
R34, 35	Resistor, metal film, axial	
	104775-6 = 6.65K, 1%, 1/4W	0410-1367
	104775-7 = 18.2K, 1%, 1/4W	0410-1409
	SEMICONDUCTORS	
CR1, 4	Diode, silicon, 1N914B/1N4448	26482
CR2, 3	Diode, silicon, rectifier, 1Amp, 1N4003	30769
CR7	Rectifier, avalanch, 600V, 1A, 1N4005	26935
CR8	Suppressor, transient voltage, 1.5KE350CA	101722
CR9, CR11	Diode, Zener, 10V, 5%, 1W, 1N4740A	33342
CR10, 12	Diode, silicon, rectifier, 1Amp, 1N4003	30769

Table 21-2. Replaceable parts, RFL 93 Alarm I/O module – continued
Assembly No. 104775-6 and 104775-7

Circuit Symbol (Figs. 21-3 & 21-4)	Description	Part Number
	SEMICONDUCTORS - continued	
Q1-3	Transistor, NPN, 40V, 2N4401	42574
Q4	Transistor, silicon, NPN, 700V, 5A	102870
Q5, 6	Transistor, silicon, PNP, 2N3906	21565
U1	Integrated Circuit, MOS, tri-state buffer	0615 290
U2	Switch, solid state	102842
U3, 4	Opto device, iso-coupler, MOC8021	90271
	MISCELLANEOUS COMPONENTS	
J1-6	Connector, header, single, 2 ckt	32802 2
K4, 5	Relay, SPDT, 12V, PCB, sealed	101236
L1	Inductor, 10μH, 5%, 1.5A max	30285
L2-12	Inductor, 10μH, 5%, 1.5A max	102698
TB8, 9	Terminal block, 6 terminal	101233



Connector ECB Assy.
Drawing No. C-103853



Panel ECB Assy.
Drawing No. C-104718

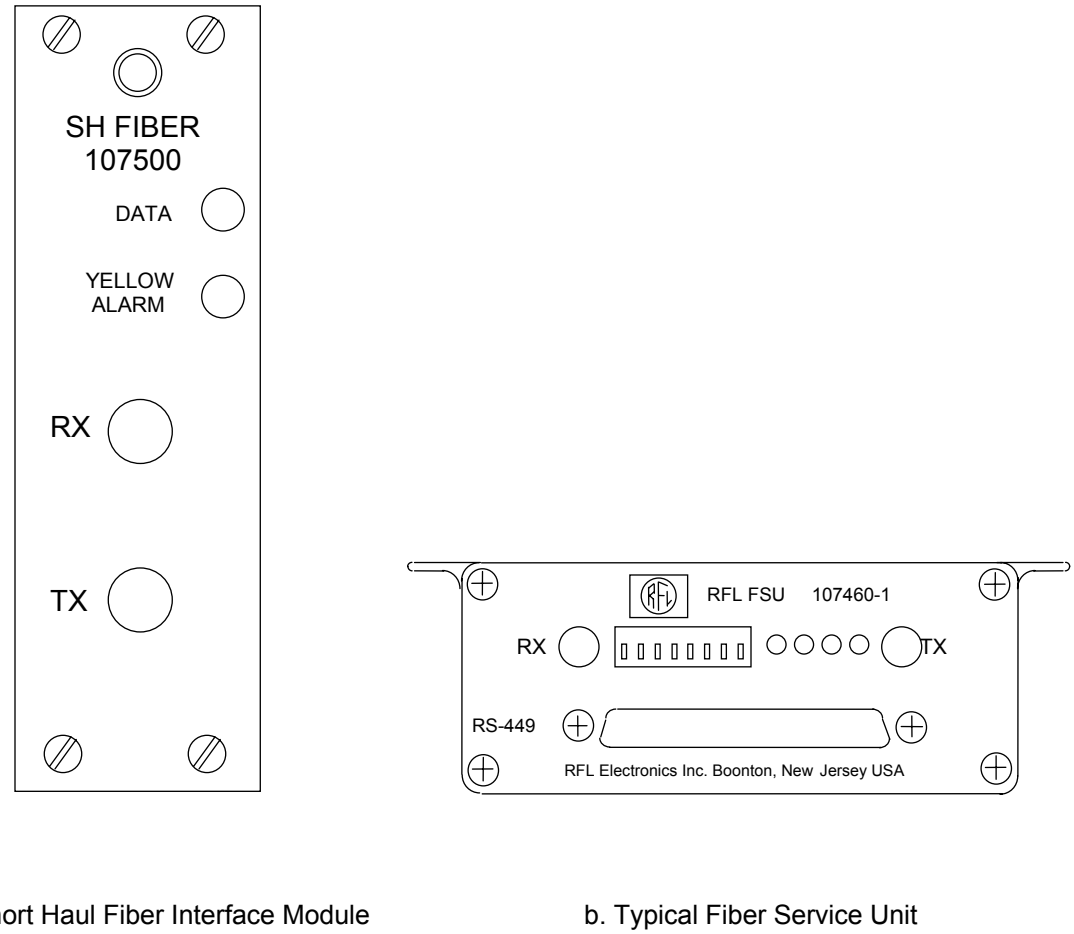
Figure 21-3. Component locator drawing, RFL 93 Alarm I/O Module, Assembly No. 104775-5

SECTION 22. SHORT HAUL FIBER INTERFACE MODULE AND FIBER SERVICE UNIT

WARNING

YOUR RFL 9300 TERMINAL MAY BE EQUIPPED WITH FIBER OPTIC INPUT/OUTPUT MODULES THAT HAVE FIBER OPTIC EMITTER HEADS. FIBER OPTIC EMITTER HEADS USE A LASER LIGHT SOURCE THAT PRODUCE INVISIBLE RADIATION. FIBER OPTIC COMMUNICATION SYSTEMS ARE INHERENTLY SAFE IN NORMAL OPERATION BECAUSE ALL RADIATION IS CONTAINED IN THE SYSTEM. IT IS POSSIBLE DURING MAINTENANCE TO EXPOSE THE RADIATION BY REMOVING OR BREAKING THE FIBER. STARING DIRECTLY INTO THE LIGHT BEAM MAY RESULT IN PERMANENT EYE DAMAGE AND/OR BLINDNESS. NEVER LOOK DIRECTLY INTO THE LIGHT BEAM AND BE CAREFUL NOT TO SHINE THE LIGHT AGAINST ANY REFLECTIVE SURFACE.

THE LASER SOURCE IS A CLASS I LASER PRODUCT WHICH COMPLIES WITH APPLICABLE FDA, OSHA AND ANSI STANDARDS.



a. Short Haul Fiber Interface Module

b. Typical Fiber Service Unit

Figure 22-1. Front panel view of RFL 93 SH FIBER short haul interface module and RFL FSU fiber service unit

22.1 INTRODUCTION

The RFL SH FIBER, Short Haul Fiber Interface module (Figure 22-1a) and the RFL FSU Fiber Service Unit (Figure 22-1b), are used in applications where the communications equipment is remotely located from the RFL 9300 relay. Data cables routed through cable troughs in a substation environment can be subjected to induced voltages from adjacent cables, producing intermittent loss of communications. To eliminate this problem the RFL SHF module provides immunity by using a fiber optic communication path between the RFL 9300 and the digital channel equipment. Refer to paragraph 22.2 for more information on the RFL 93 SHF short haul fiber module. Refer to paragraph 22.3 for more information on the FSU module.

22.2 SHORT HAUL FIBER INTERFACE MODULE

22.2.1 DESCRIPTION

The RFL 93 Short Haul Fiber Interface module (Figure 22-1a) is housed in a single 1.4 inch wide module, and can be installed in either one of the two right-most slots at the rear of the 9300 chassis. The module consists of an input section (detector) and an output section (emitter). Table 22-1 contains general information related to the RFL 93 Short Haul Fiber Interface module.

Table 22-1. General Information, Short Haul Fiber Interface Module

Assembly Number	Type	Wavelength/Mode	Connector Type	Receiver Sensivity	Tx Level (Min)	Typical Distance
107500	LED Emitter/Detector	830 (+/-40 nm) multimode	ST	-32dBm to-11dBm	-19dBm (62.5μm)	Up to 2km (1.2mi) using 50μm or 62.5μm core diameter optical fiber

22.2.2 SPECIFICATIONS

As of the date this manual was published, the following specifications apply to the RFL SHF Short Haul Fiber Interface module, except where indicated. Because all RFL products undergo constant refinement and improvement, these specifications are subject to change without notice.

IEEE Standard: C37.94 for N times 64 kilobit per second Optical Fiber Interfaces between teleprotection and multiplexer equipment.

Input Power Requirements (from chassis supply):
+5-Volt Supply: 175 mA (max)

Input Drive Signals: TTL logic-level control signals from Communications Controller module.

Receiver Sensitivity: See Table 22-1.

Tx Level: See Table 22-1.

Temperature:
Operating: -30^{O}C to +60^{O}C (-22^{O}F to +140^{O}F).

Relative Humidity: 90 percent, non-condensing @ 40^{o}C.

Dimensions:
Width (including panel) 1.4 inches (3.6 cm)
Height (including panel) 5 inches (12.7 cm)
Depth (behind panel) 4.7 inches (12.0 cm)

22.2.3 CONTROLS AND INDICATORS

Figure 22-2 shows the location of all controls and indicators on the RFL 93 SH FIBER module. These controls and indicators are described below.

Controls

DS9	Fiber optic emitter
U7	Fiber optic detector
J1	Motherboard connector

Indicators

D1	Data LED (Green):	Loss of signal when not illuminated. Active when fiber data is valid with no bit errors. Extinguished indicates loss of signal. Pulsing indicates bit errors.
D2	Yellow Alarm LED (Amber):	Yellow alarm when illuminated. Indicates that the remote fiber receiver has failed and the remote transmitter is sending yellow code detected by the local fiber receive channel.

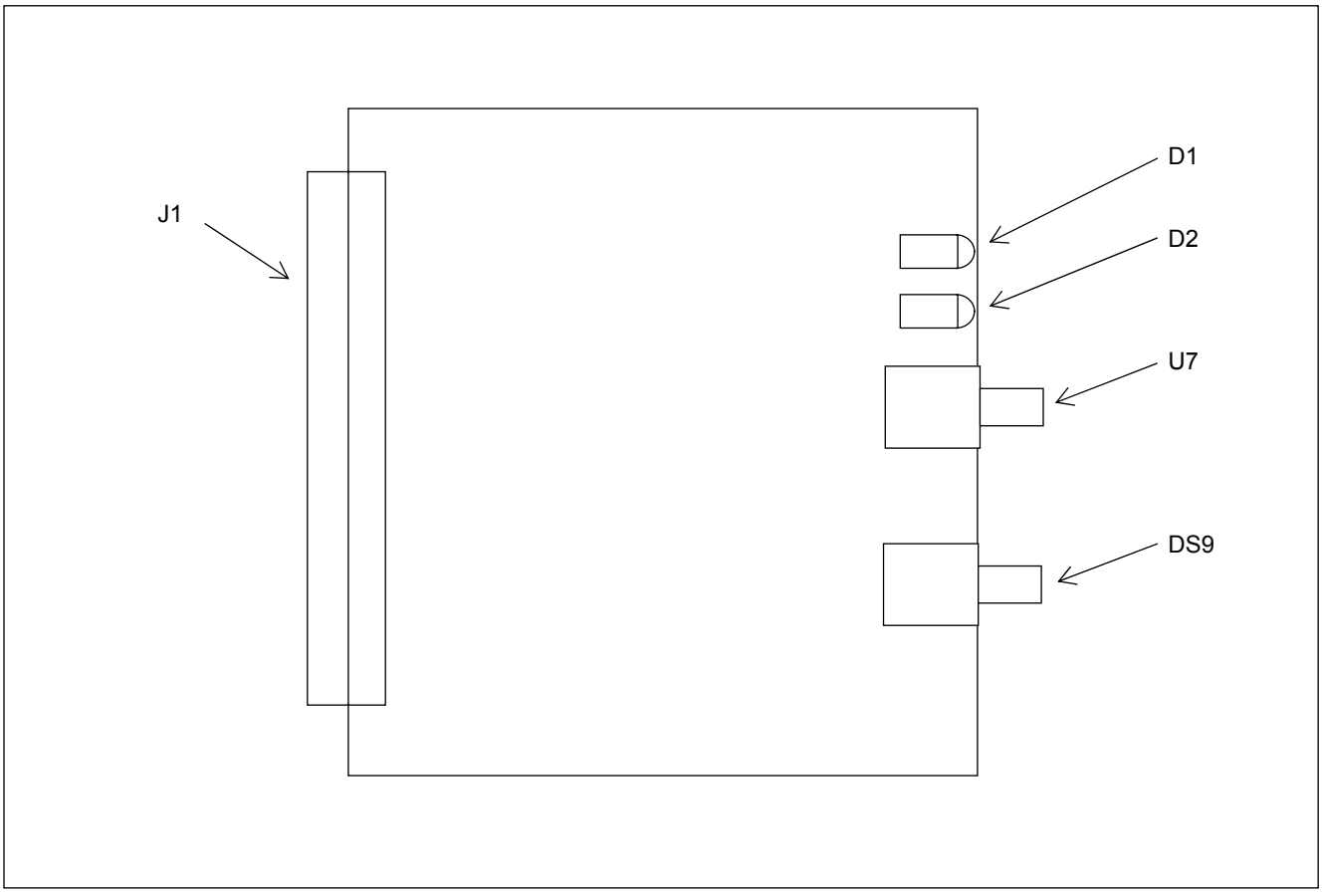


Figure 22-2. Controls and indicators, RFL 93 SHFI short haul fiber interface module

22.3 FIBER SERVICE UNIT

The RFL FSU Fiber Service Unit (Figure 22-1b) is used with the RFL SH FIBER Short Haul Fiber Interface module (Figure 22-1a). The FSU consists of an input section (detector) and an output section (emitter) and is housed in a black anodized aluminum box. There are four types of Fiber Service Units, providing RS-449, G.703, V.35 or X.21 as inputs and outputs on the non-fiber side of the connection. The FSU can be located up to 2km away from the RFL 9300.

The RFL FSU Fiber Service Unit has a 15-pin or 37-pin male D-subminiature connector on its front panel depending on the application. During installation, make sure that the screws on both ends of the mating connector are tightened to secure the connector to the FSU panel. Fiber optic cables with type ST series bayonet fiber optic connectors (or their equivalent) must be connected to the fiber optic heads on the rear panels of the RFL FSU module and the RFL SHFI module. The exact mating connectors used will depend upon the heads that are installed in these modules and the specific optic cable being used. When connecting fiber optic cables, make sure the connectors are properly aligned before tightening, and then fully tighten them. This will help minimize losses in the connector. Figure 22-3 shows a typical Fiber Service Unit installation.

Refer to the Fiber Service Unit Instruction Data sheet (publication number:ID C37.94FSU) for additional information.

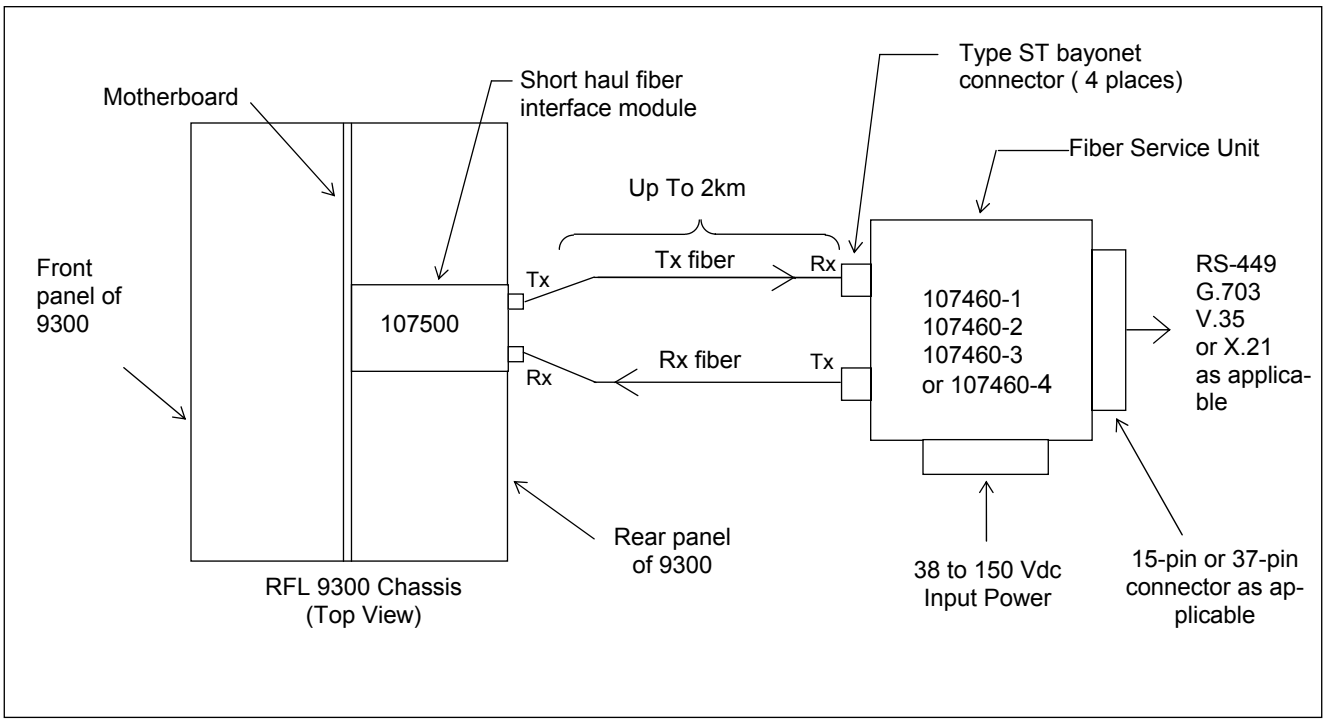


Figure 22-3. Typical Fiber Service Unit Installation

Table 22-2. Replaceable parts, RFL 93 SHFI short haul fiber interface module
Assembly No. 107500

Circuit symbol (Figs 22-4 & 22-5)	Description	Part number
	CAPACITORS	
C3, 4, 10, 19, 21, 34, 36, 37, 41, 42, 45-52, 54-56	Capacitor, ceramic, 0.1uF, 10%, 50V	151-10104040603
C7, 23	Capacitor, ceramic, 100pF, 5%, 50V	151-05101040503
C8, 24, 25	Capacitor, ceramic, 0.01uF, 10%, 50V	151-10103040603
C9, 20	Capacitor, ceramic, 0.047uF, 10%, 50V	151-10473040603
C13	Capacitor, ceramic, 820pF, 5%, 50V	151-10821050603
C17, 43	Capacitor, ceramic, 0.47uF, 10%, 50V	151-10474040612
C22, 35, 39, 44, 67	Capacitor, tantalum, 100uF, 10%, 10V	153-107070206
C38, 40	Capacitor, ceramic, 10uF, 10%, 10V	151-10106010607
	RESISTORS	
R1, 2	Resistor, thick film, 243Ω, 1%, 1/8W	700-15243034
R3, 12	Resistor, thick film, 4.75K, 1%, 1/8W	700-15475134
R6	Resistor, thick film, 162Ω, 1%, 1/8W	700-15162034
R7, 11, 13	Resistor, thick film, 60.4Ω, 1%, 1/4W	700-2060R435
R8	Resistor, thick film, 22.1Ω, 1%, 1/8W	700-1522R134
R10, 33, 37	Resistor, thick film, 10K, 1%, 1/8W	700-15100234
R14, 35	Resistor, thick film, 2.21K, 1%, 1/8W	700-15221134
R15	Resistor, thick film, 332Ω, 1%, 1/8W	700-15332034
R18	Resistor, thick film, 4.22K, 1%, 1/8W	700-15422134
R19	Resistor, thick film, 6.81K, 1%, 1/8W	700-15681134
R27, 28	Resistor, thick film, 4.7Ω, 1%, 1/8W	700-154R7034
R29	Resistor, thick film, 0.01Ω, 1%, 1W	700-40R01037
R30	Resistor, thick film, 10Ω, 1%, 1/8W	700-1510R034
R31	Resistor, thick film, 6.65K, 1%, 1/8W	700-15665134
R32	Resistor, thick film, 20Ω, 1%, 1/8W	700-1520R034
R34	Resistor, thick film, 2.43K, 1%, 1/8W	700-15243134
R36	Resistor, thick film, 124Ω, 1%, 1/8W	700-15124034
R38	Resistor, thick film, 0.56Ω, 1%, 1/4W	700-20R56034
R39	Resistor, thick film, 47.5Ω, 1%, 1/4W	700-2047R534
R42	Resistor, thick film, 0Ω, 1%, 1/8W	700-15000034
RZ1	Resistor network, 10K, 8R/PKG, SIP	95571

Table 22-2. Replaceable parts, RFL 93 SHFI short haul fiber interface module Assembly Number 107500 – continued

Circuit symbol (Figs 22-4 & 22-5)	Description	Part number
	SEMICONDUCTORS	
D10	Diode, general purpose, 4148	340-100
Q1	Transistor, MOSFET, N-CH, IRLML2502	940-10105
U1	Integrated circuit, FPGA, XCS20XL-4VQ100I	500-123
U3	Integrated circuit, PROM, XC17S20XL	0640-37
U4	Crystal oscillator, 32.768 mHz	300-10101
U5	Integrated circuit, hot-swap controller, 1422	510-103
U6	Integrated circuit, linear regulator, 3.3V, LM1117	510-128
U7	Opto device, fiber-optic receiver	103208
U8	Integrated circuit, fiber-optic data quantizer, ML4622	500-106
U9	Integrated circuit, MOS, PLL with VCO, 74HCT4046A	500-122
U10	Integrated circuit, QUAD 2-INPUT, 74F3037	500-121
U11	Integrated circuit, QUAD 2-INPUT AND gate, 74ACT08	500-120
U12	Integrated circuit, PROM, XC17S20XL	505-114
U13, 14	Integrated circuit, MOS TRI-ST, OCTAL buffer, 74ABT244	500-102
U15	Integrated circuit, QUAD, TRANS, MAX3041	505-113
	MISCELLANEOUS COMPONENTS	
D1	Opto device, LED, green	32567
D2	Opto device, LED, amber	99798
DS9	Opto device, fiber-optic transmitter	101112
J1	Connector, plug, female, 64 contact, DIN	99134
J2	Connector, header, single 7 CKT	32802-7
L1, 2	Inductor, molded, 22uH, 227mA, 10%	470-10103
L3	Inductor, molded, 4.7uH	470-10104
TP3, 4	Testpoint, terminal, orange	98441-3

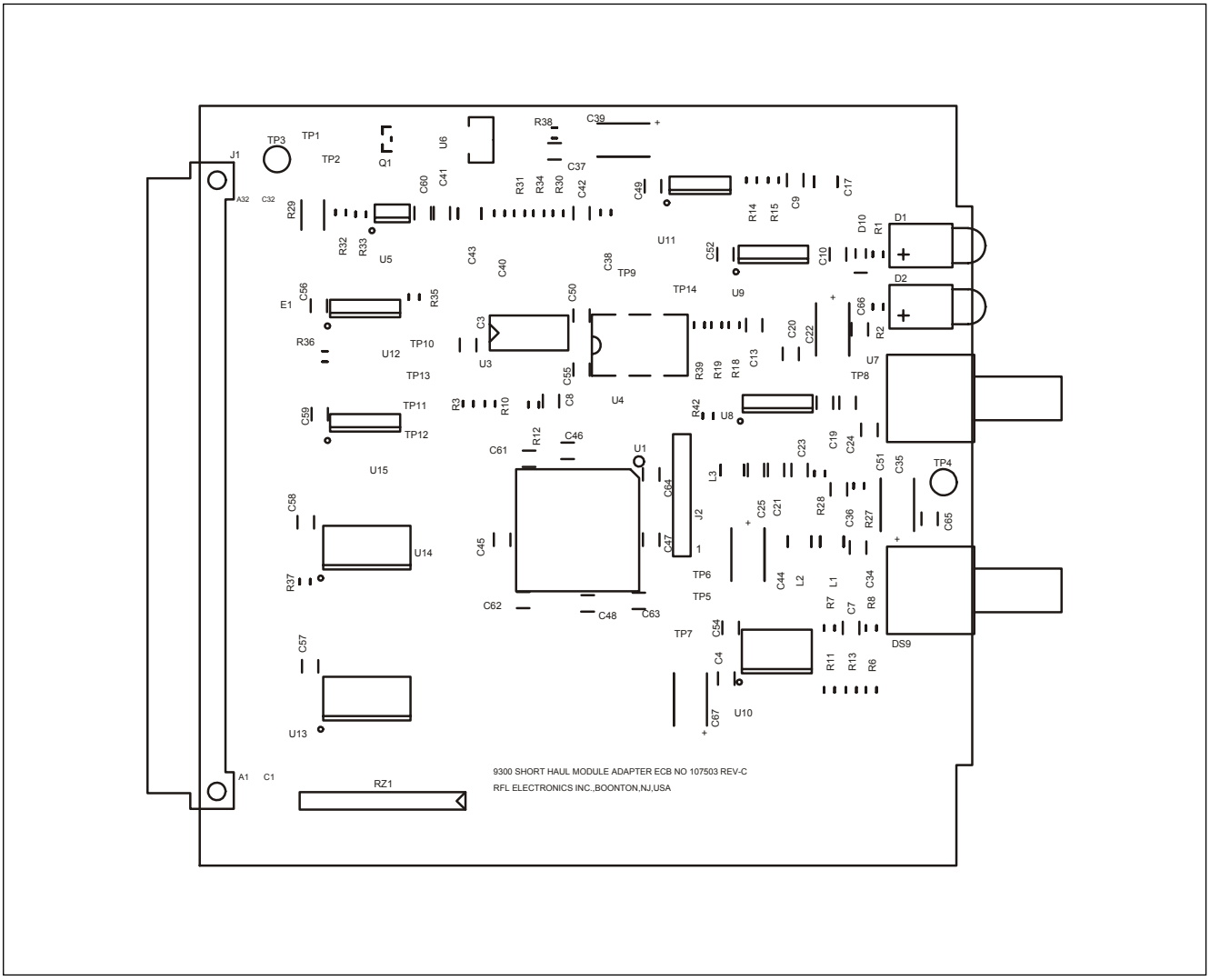


Figure 22-4. Component locator drawing, RFL 93 short haul fiber interface module (Assembly No. 107500)

Figure 22-5. Schematic, RFL 93 Short Haul Fiber Module (3 sheets) (Assembly No. 107500; Schematic No. D-107504-C)

Please see Figure 22- 5, in Section 32: Schematics

This page intentionally left blank

SECTION 23: G.703 INTERFACE I/O MODULE

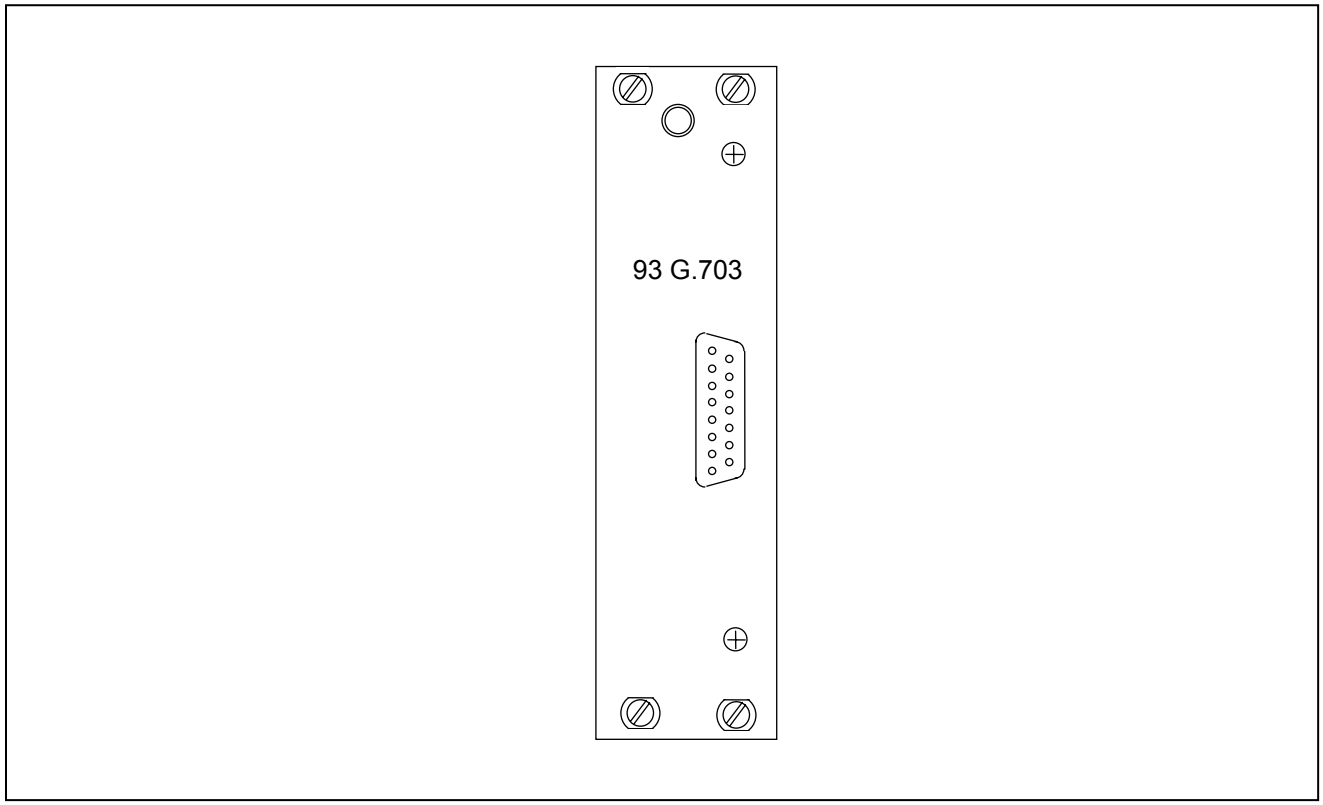


Figure 23-1. RFL 93 G.703 Interface I/O Module

23.1 DESCRIPTION

The RFL 93 G.703 Interface I/O Module (Fig. 23-1), plugs into the back of the 9300 chassis and provides a full duplex serial link to a remote 93 G.703 module. It does this without an additional board plugged into the front of the chassis since all logic is contained in the rear module.

23.2 CONTROLS AND INDICATORS

The RFL 93 G.703 Interface I/O Module circuit board contains three programmable jumpers that prepare it for use, two potentiometers, three test points and a rear-panel 15-pin D-subminiature connector. Figure 23-2 shows the jumper locations, and their functions are described below. The jumpers, potentiometers, and test points can only be accessed when the RFL 93 G.703 is out of the chassis or is on a card extender.

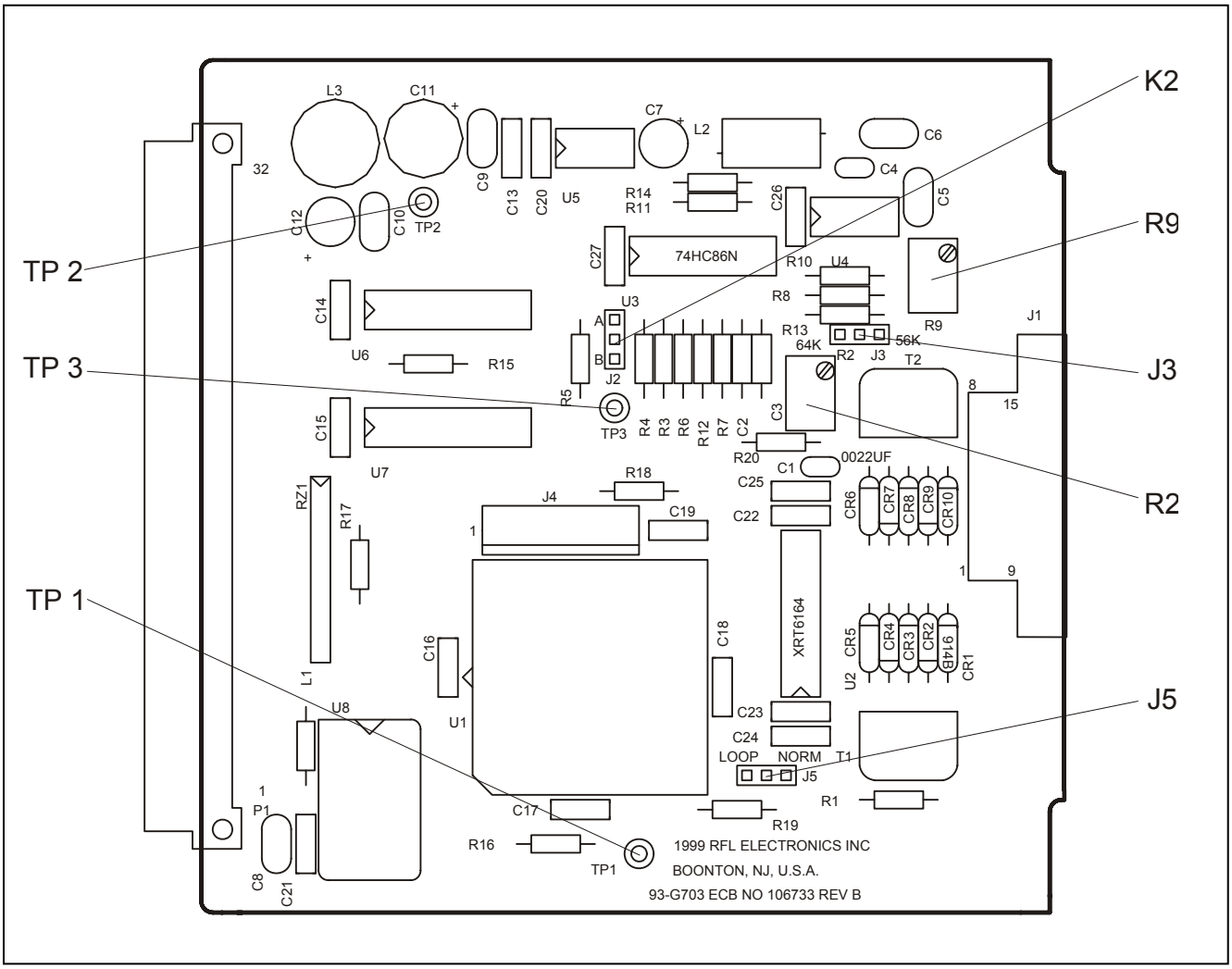


Figure 23-2. Controls and indicators, RFL 93 G.703 Interface I/O Module

REAR-PANEL CONNECTOR

J1 Rear-panel 93 G.703, DB15 connector. The following pins are supported, and all other pins are not connected:

Pin No.	93 G.703 Signal
1	Shield Ground
2	Transmit A
4	Receive A
9	Transmit B
11	Receive B

JUMPERS

J2 A position is for normal operation. (phase locked loop is enabled)
B position is used for factory testing. (phase locked loop is disabled)

J3 Selects 56kbps or 64kbps data rate

J5 Selects Loop or Normal operation. When set to Loop, the receiver clock is looped back out to the transmitter as shown in Figure 23-3.

POTENTIOMETERS

R2 Used to adjust the G.703 output voltage level. Factory adjustment only.

R9 Used to adjust the phase locked loop. Factory adjustment only.

TEST POINTS

TP1 3.584 mHz clock

TP2 Signal ground

TP3 Used for factory testing only

23.3 THEORY OF OPERATION

23.3.1 SYSTEM OVERVIEW

The 93 G.703 creates a full duplex 64kbps serial link to a remote 93 G.703 module. The 9300 is considered Data Terminal Equipment (DTE). The 93 G.703 plugs into the back of the 9300 and does not require a card to be plugged into the front of the chassis since all logic is contained on the rear board. The G.703 protocol is a pulsed AMI 2 wire TX pair and an AMI 2 wire RX pair. The polarity of the pulses are constantly toggled, therefore, the DC component is a zero. Since there is no DC component, isolation transformers can be present in both the RX and TX ports. If the AMI pulses are at 128 kHz, the digital signal is a 0 and if it is at 64 kHz then the digital signal is a 1. The receiver contains an analog phase locked loop to recover the remote TX clock and create the local RX clock. The transmitter output can get the transmitter clock timing from any one of the following three sources: from a local crystal oscillator, from the incoming receiver clock or from an adjacent 93 G.703 module.

The 93 G.703 module can be used in any of the three 9300 configurations. These include two terminal, two terminal with hot standby and three terminal. Hot standby and three terminal operation require that both transmitter clocks are locked together. In the case of hot standby, there is only one CC card to shift out transmitter data to both 93 G.703 modules. In the case of three terminal, the transmitter clocks should also be locked together to keep the clocks from walking on the back plane and potentially interfering with each other. For this reason, the 93 G.703 card plugged in the first card slot will present the TX clock to the 93 G.703 in the second position. In hardware (in the Actel), the second 93 G.703 will see the adjacent card clock transitions and use this clock source for transmitter timing. This is done automatically by the hardware and does not require any software or jumper settings from the supervisor card. The transmitter timing is recovered inside the Actel chip with a digital phase locked loop. The reference input comes from the adjacent 93 G.703 card. If the receiver clock is looped back out of the transmitter, the local oscillator and the adjacent TX clock reference are not used. This option is the most likely configuration to be used in the field.

In most cases an interposing piece of communication equipment (DCE) will send and receive the data and timing over a communication path to the remote terminal. The DCE then becomes a clock source to both the remote and local terminals. The DCE equipment will be the source of both the transmitter and receiver clocks. This is accomplished in the 93 G.703 by looping the receiver clock back out to the transmitter. For in-house testing or for relays connected over metallic pairs, the local Tx oscillator is the best choice since the DCE interface does not exist. A jumper on the 93 G.703 module allows the RX clock to be looped out of the TX port.

23.3.2 CLOCKING AND CONFIGURATIONS

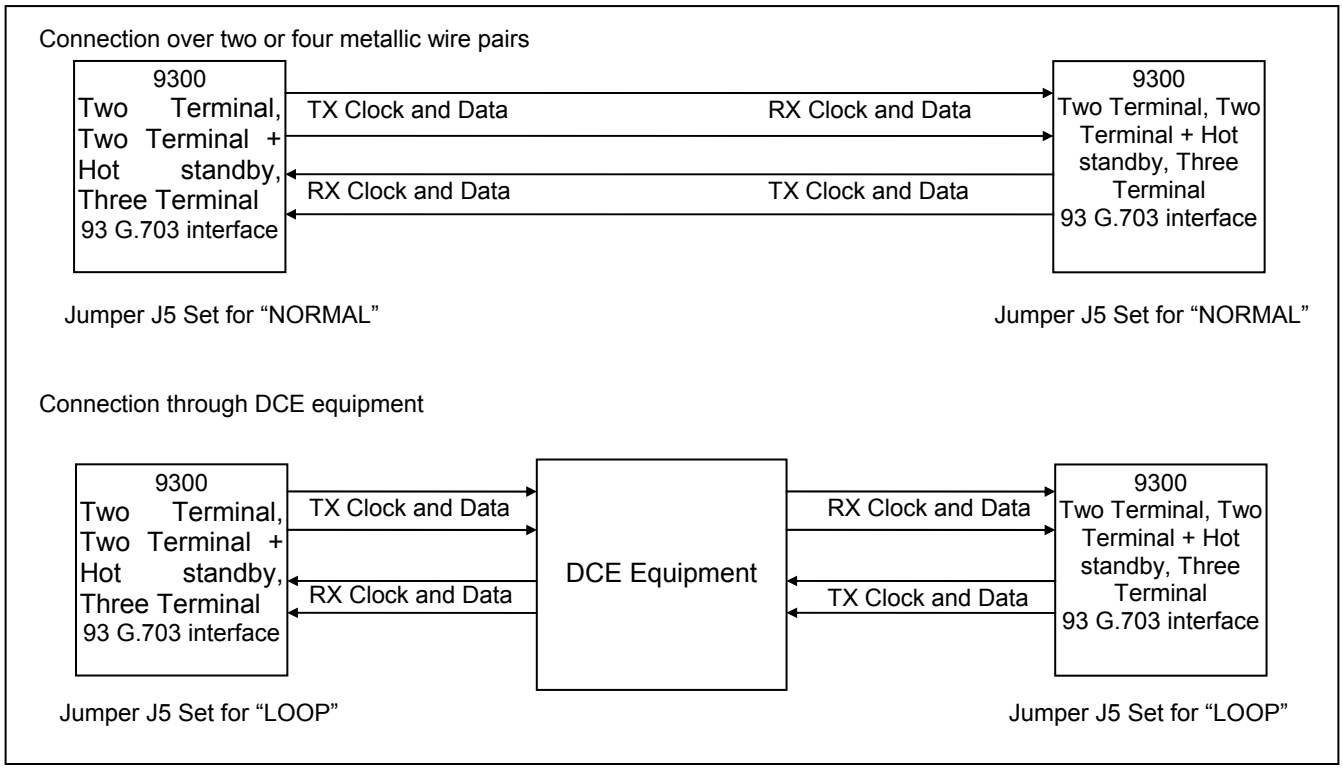


Figure 23-3. Setting J5 for Normal or Loops Operation

23.3.3 PULSE INPUT/ OUTPUT CIRCUIT DESCRIPTION

The XRT6164 chip combined with transformers T1 and T2 forms a G.703 analog pulse to TTL pulse interface with the Actel (U1). The G.703 protocol is an AMI return to zero pulse. The TTL output from U2 separates the positive and negative G.703 pulses and outputs a positive going pulse on S+R and S-R. This is a non-return to zero signal that is suitable for digital logic. The specification for a G.703 pulse is one volt peak. Diodes at the transformers (CR1- CR4) and (CR6 - CR9) limit transient peaks induced on the wires from coming into the module. The diodes limit incoming signals to three forward diode drops or about 2.1 v. R2 is in series with the transformer and transistor collector outputs from the XRT6164 (TXD+ and TXD-). This allows adjustment of peak levels into the 120 ohm termination presented by the external equipment. Transmitter calibration is accomplished by connecting a 120 ohm load between pins 2 and 9 of J1 and with the aid of an oscilloscope, set the peak levels at 1 volt. R20 prevents overloading the transistors in U2 and damaging the chip.

23.3.4 RECEIVER PHASE LOCK LOOP CIRCUIT DESCRIPTION

The receiver phase lock loop consists of U1, U3, U4 and the surrounding discrete resistors and capacitors. U1 does very little in the phase locked loop. It only divides the output from U3 by 2 and outputs it on VCO_2. In addition, U1 combines positive and negative G.703 pulses into RX_P and RX_N with an OR gate and outputs the resultant signal on PH_DET. This line contains all transitions and is the input to the receiver phase locked loop circuit through J2. U3 combined with R5, R6, C2, R7 and C3 form a phase detector. The PH_DET line into U3 is the reference. The VCO_2 line into U3 is the output from the phase detector, a 128 kHz signal. VCO_1 is a 256 kHz signal that is divided by two in the ACTEL and output on VCO_2. The G.703 RX pulses are at 128 kHz or 64 kHz depending on if the digital communication between 9300's is sending a 0 or a 1. U4 is limited in output frequency so that is must output a signal at or about 256 kHz even if the reference on PH_DET is 64 or 128 kHz. This keeps the phase locked loop from locking an octave away from the correct signal. Changes in the clock rate from the receiver are slowly tracked and integrated. The resultant 128 kHz signal is again divided in the Actel to create the receiver clock, a 64 kHz pulse.

23.3.5 ACTEL DESCRIPTION

The Actel chip performs all of the digital processing required in the interface. The receive pulses from U2 are non-return to zero pulses. The recovered RX 64 kHz clock from the phase lock loop is recover from the combined non-return to zero data stream. The 64 kHz clock could be inverted out of the divider. If necessary, the sync detector in the Actel inverts the clock. If J5 is set to “LOOP”, the recovered 128 kHz receive clock is used for generating the TX signals. If J5 is set to “NORMAL”, the TX source comes from a TX PLL module within the Actel. The TX PLL module always outputs a 128 kHz clock. The clock may be phase locked to the TX reference input line or it could be free wheeling. The TX PLL module looks for transitions on the TX reference input and if they are absent, the module outputs a centered 128 kHz signal. It is not pulled to the high or low end of the PLL. The TX clock is then used to read the TX data from the communications card. The TX LOGIC module in the Actel then generates two outputs for the AMI G.703 transmitter, the positive and negative TX pulse signals. In addition, it also creates the local TX clock.

The TX PLL module will free wheel on the 3.584 mHz crystal clock to create the 64 kHz TX clock. If the reference clock is present, the TX PLL will add or subtract one 3.584 mHz clock pulse interval to the 64 kHz output on every rising edge of every 32nd reference clock pulse. This results in a very limited pull range with very little average jitter. This means that at the most, one correction of 279 ns will be added or subtract once every 500,000 ns, or one part in 1,792.

Table 23-1. Replaceable parts, RFL 93 G.703 Interface I/O Module (Assembly No. 106730)

Circuit Symbol (Figs. 23-4 & 23-5)	Description	Part Number
	CAPACITORS	
C1	Capacitor, ceramic dip, 0.0022μF, 5%, 50V	1007 1654
C2	Capacitor, ceramic, 560pF, 5%, 100V	0125 15615
C3	Capacitor, ceramic, 0.0056μF, 5%, 100V	0125 15625
C4	Capacitor, ceramic dip, 330pF, 10%, 100V	1007 1672
C5, 6, 8, 9, 10	Capacitor, ceramic dip, 0.01μF, 5%, 100V	1007 1645
C7	Capacitor, tantalum, 10μF, 10%, 20V	1007 1465
C11	Capacitor, electrolytic, 100μF, 20%, 25V	1007 1795
C12	Capacitor, electrolytic, 47μF, 20%, 35V	1007 1578
C13-27	Capacitor, ceramic dip, 0.1μF, 10%, 50V	0120 38
	RESISTORS	
R1	Resistor, metal film, axial, 487Ω, 1%, 1/4W	0410 1258
R2	Resistor, metal film, variable, 1K, 10%, 1/2W	49995
R3	Resistor, metal film, axial, 100K, 1%, 1/4W	0410 1480
R4, 16	Resistor, metal film, axial, 1K, 1%, 1/4W	0410 1288
R5	Resistor, metal film, axial, 78.7K, 1%, 1/4W	0410 1470
R6	Resistor, metal film, axial, 182K, 1%, 1/4W	0410 1505
R7	Resistor, metal film, axial, 8.45K, 1%, 1/4W	0410 1377
R8	Resistor, metal film, axial, 4.02K, 1%, 1/4W	0410 1346
R9	Resistor, metal film, variable, 2K, 10%, 1/2W	90392
R10	Resistor, metal film, axial, 681Ω, 1%, 1/4W	0410 1272
R11	Resistor, metal film, precision, 10Ω, 1%, 1/4W	1510 1015
R12	Resistor, metal film, axial, 2K, 1%, 1/4W	0410 1317
R13, 17, 19	Resistor, metal film, axial, 10K, 1%, 1/4W	0410 1384
R14	Resistor, fixed composition, 2.7Ω, 5%, 1/4W	1009 900
R15	Resistor, metal film, axial, 124Ω, 1%, 1/4W	0410 1201
R18	Resistor, metal film, axial, 49.9K, 1%, 1/4W	0410 1415
R20	Resistor, metal film, axial, 100Ω, 1%, 1/4W	0410 1192
RZ1	Resistor network, 10K, 8R/PKG, SIP	95571

Circuit Symbol (Figs. 23-4 & 23-5)	Description	Part Number
	SEMICONDUCTORS	
CR1-10	Diode, silicon, 1N914B/1N4448	26482
U2	Integrated Circuit, interface, line transceiver	0680 21
U3	Integrated Circuit, MOS Quad, 2-input exclusive OR gate	0615 268
U4	Integrated Circuit, voltage to frequency converter	0625 34
U5	Integrated Circuit, +5V linear voltage reference	0620 308
U6	Integrated Circuit, MOS quad, differential line receiver	0615 394
U7	Integrated Circuit, MOS quad, differential line driver	0615 395
U8	Crystal, hybrid clock oscillator, 3.584 mHz	103347
	MISCELLANEOUS COMPONENTS	
J1	Connector, JK-male, 15 pin	103342
J2, 3, 5	Connector, header, single, 3 circuit	32802 3
J4	Connector, wafer assembly, 8 circuit	97223 8
L1	Inductor, molded, 100μH, 10%, 84 mA DC	32505 1
L2	Bead, ferrite shield	103344
L3	Inductor, power line, 10μH	30063
P1	Connector, plug, female, 64 contact, DIN	99134
T1,2	Transformer, 1:1 coupling	103343
TP1, 2, 3	Test point, terminal, orange	98441 3

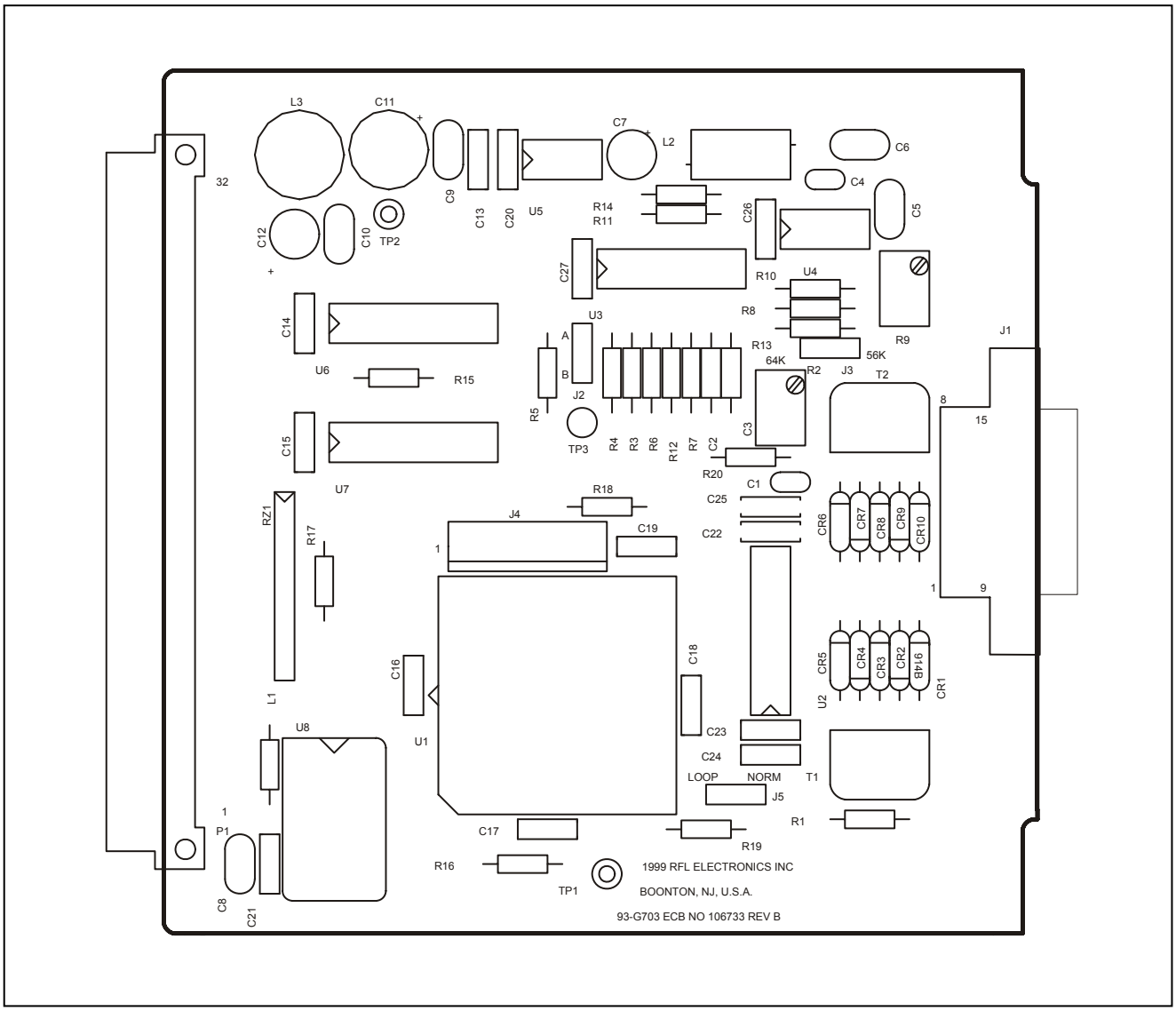


Figure 23-4. Component locator drawing, RFL 93 G. 703 Interface I/O Module (Assembly No. 106730)

Figure 23-5. Schematic, RFL 93 G.703 module (Assembly No. 106730; Drawing No. D-106734-B)

Please see Figure 23- 5, in Section 32: Schematics

This page intentionally left blank

SECTION 24: SINGLE POLE CHASSIS

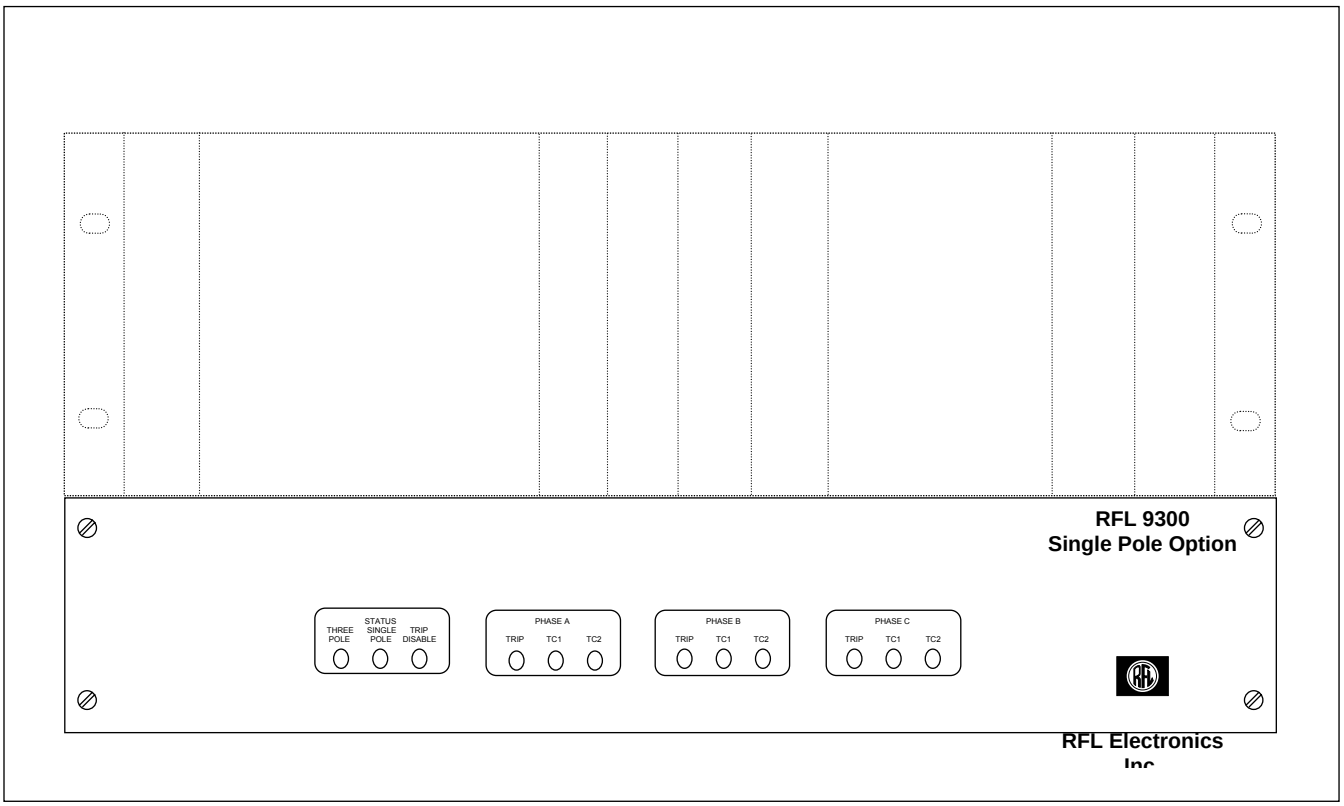


Figure 24-1. Typical RFL 9300 Single Pole Chassis, front panel view

24.1 DESCRIPTION

Single Pole Tripping is an optional feature of the RFL 9300, which requires an additional chassis mounted below the existing RFL 9300 chassis. The Single Pole Chassis contains all of the circuitry required for Single Pole Tripping, which allows phase A, B or C to trip independently of the other two phases. A front panel view of the RFL 9300 Single Pole Chassis is shown in Figure 24-1. A rear panel view of the RFL 9300 Single Pole Chassis is shown in Figure 24-3.

Table 24-1 provides general information about the Single Pole Chassis, Tables 24-2 and 24-3 are lists of replaceable parts, Figures 24-6 and 24-8 are component locator drawings, and Figures 24-7 and 24-9 are schematic diagrams.

Table 24-1. RFL 9300 Single Pole Chassis, General Information

Model Number	Assembly Number	Width	Height
9300 CC SINGLE POLE TRIP	106700	17.25 in (43.82 cm)	3.375 in (8.57 cm)

24.2 CONROLS AND INDICATORS

The controls and indicators for the Single Pole Chassis consist of front panel LED indicators, rear panel terminal blocks, and circuit board test points. Figures 24-2, and 24-3 show the locations of all controls and indicators on the Single Pole Chassis. Note that the front panel has LEDs only, and the rear panel has terminal blocks only.

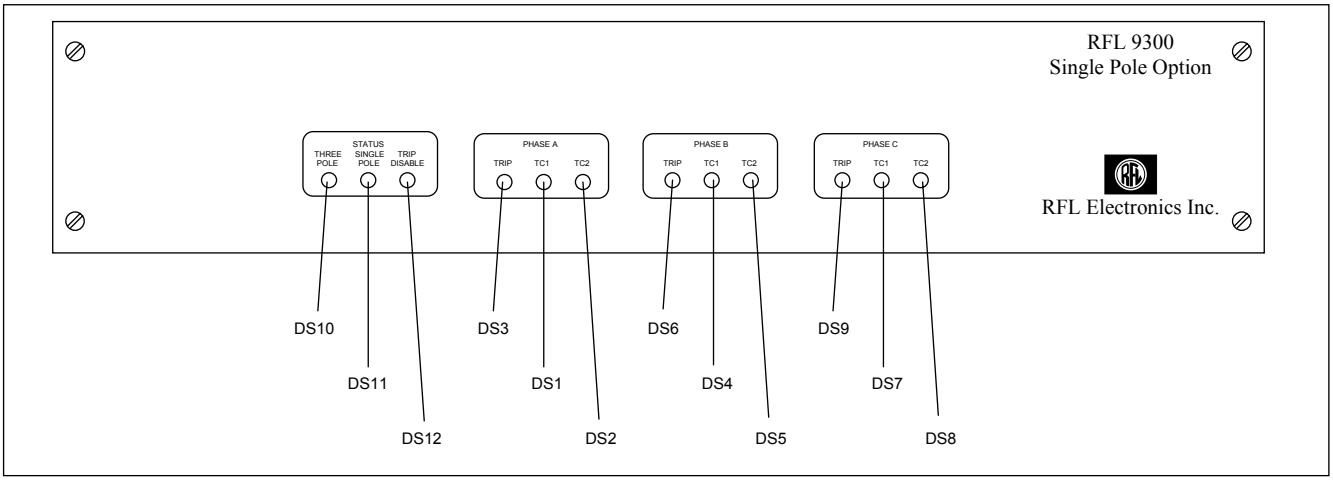


Figure 24-2. Typical RFL 9300 Single Pole Chassis, front panel view showing LED indicators

24.2.1 LED INDICATORS (See note on page 24-7)

All LEDs are latched targets except DS10, DS11 and DS12. All targets are cleared by pressing the RESET button on the Display Controller. Terminal block connections for TB1, TB2 and TB3 can be seen in Figures 24-3 & 24-7.

DS10 When “THREE POLE” LED is lit, indicates that all three phases will trip simultaneously if a trip is commanded.

DS11 When “SINGLE POLE” LED is lit, indicates that if a trip is commanded, only the phase commanded to trip, will trip.

DS12 When “TRIP DISABLE” LED is lit, indicates that the single pole chassis (lower chassis) has not been initialized and all trips are blocked.

DS3 When “PHASE A TRIP” LED is lit, indicates circuit closure between TB1A-1 and TB1A-2, TB1A-3 and TB1A-4, TB1A-5 and TB1A-6, TB1B-1 and TB1B-2, TB1B-3 and TB1B-4, TB1B-5 and TB1B-6.

DS1 When “PHASE A TC1” LED is lit, indicates circuit closure between TB1B-1 and TB1B-2 and current flow has been sensed.

DS2 When “PHASE A TC2” LED is lit, indicates circuit closure between TB1B-3 and TB1B-4 and current flow has been sensed.

DS6 When “PHASE B TRIP” LED is lit, indicates circuit closure between TB2A-1 and TB2A-2, TB2A-3 and TB2A-4, TB2A-5 and TB2A-6, TB2B-1 and TB2B-2, TB2B-3 and TB2B-4, TB2B-5 and TB2B-6.

DS4 When “PHASE B TC1” LED is lit, indicates circuit closure between TB2B-1 and TB2B-2 and current flow has been sensed.

DS5 When “PHASE B TC2” LED is lit, indicates circuit closure between TB2B-3 and TB2B-4 and current flow has been sensed.

DS9 When “PHASE C TRIP” LED is lit, indicates circuit closure between TB3A-1 and TB3A-2, TB3A-3 and TB3A-4, TB3A-5 and TB3A-6, TB3B-1 and TB3B-2, TB3B-3 and TB3B-4, TB3B-5 and TB3B-6.

DS7 When “PHASE C TC1” LED is lit, indicates circuit closure between TB3B-1 and TB3B-2 and current flow has been sensed.

DS8 When “PHASE C TC2” LED is lit, indicates circuit closure between TB3B-3 and TB3B-4 and current flow has been sensed.

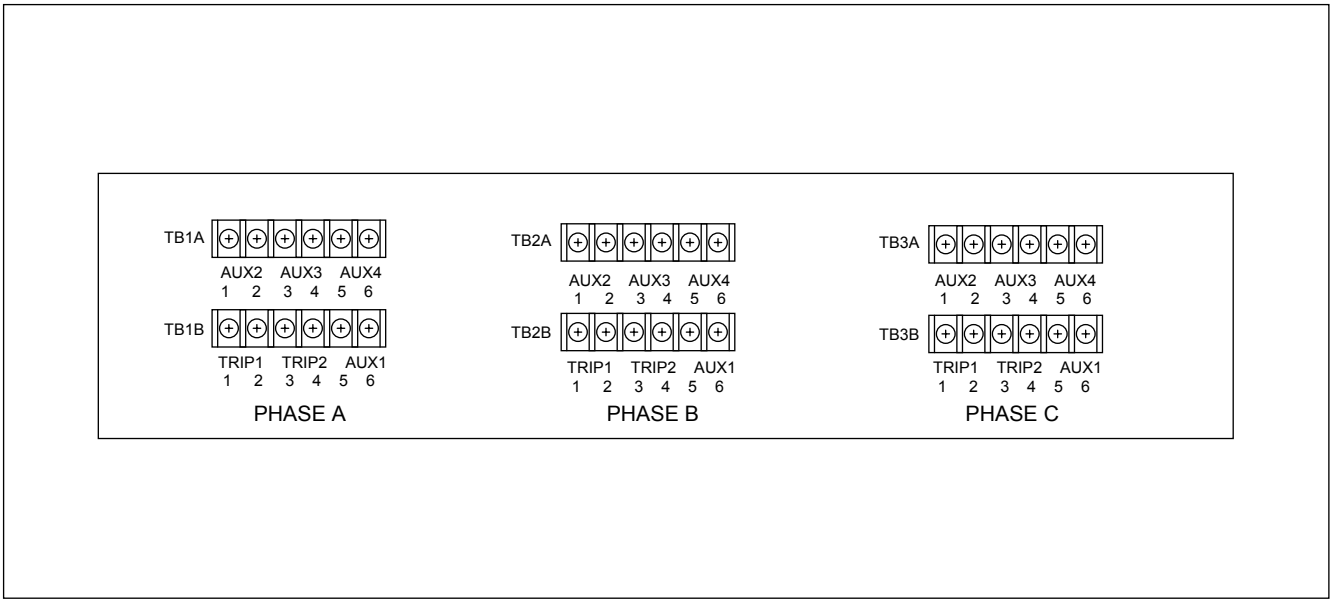


Figure 24-3. Typical RFL 9300 Single Pole Chassis, rear panel view

24.2.2 TERMINAL BLOCKS

24.2.2.1 PHASE A TERMINAL BLOCKS

TB1A

1	AUX2	Auxiliary contacts available to the user for phase A
2		
3	AUX3	Auxiliary contacts available to the user for phase A
4		
5	AUX4	Auxiliary contacts available to the user for phase A
6		

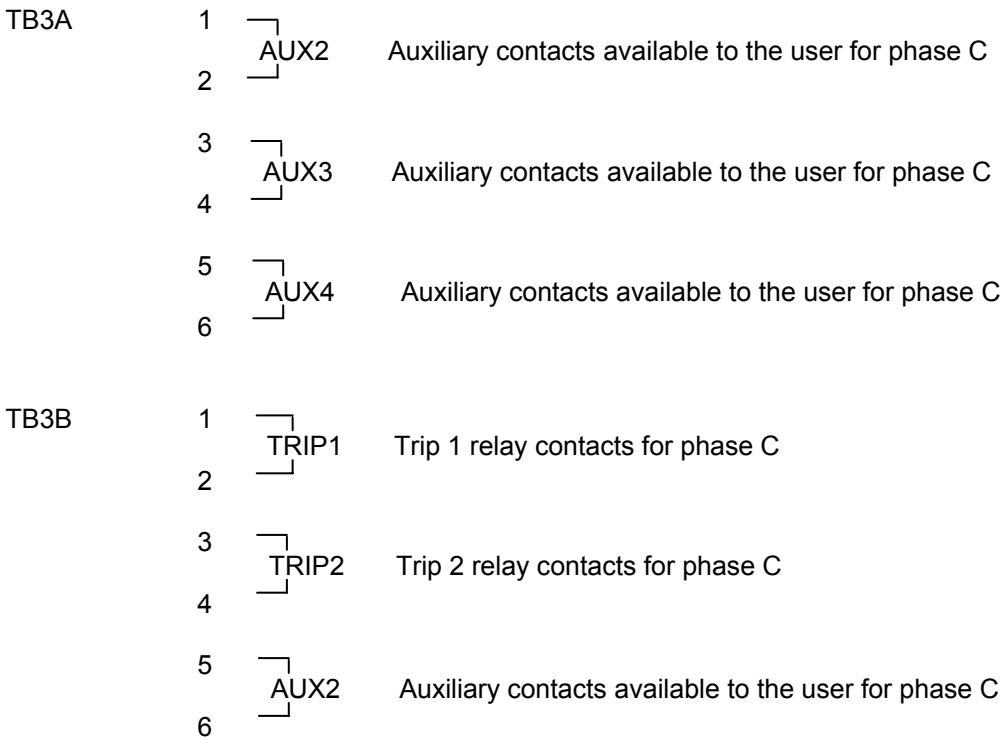
TB1B

1	TRIP1	Trip 1 relay contacts for phase A
2		
3	TRIP2	Trip 2 relay contacts for phase A
4		
5	AUX1	Auxiliary contacts available to the user for phase A
6		

24.2.2.2 PHASE B TERMINAL BLOCKS



24.2.2.3 PHASE C TERMINAL BLOCKS



24.2.3 TEST POINTS

TP1	TRIP_A_IN	A logic low trip command for phase A from the RFL 9300
TP2	SV_DAT	Serial data line to the supervisor module
TP3	A_SENSE_1	Logic high when trip current is sensed in trip relay 1 for phase A
TP4	A_SENSE_2	Logic high when trip current is sensed in trip relay 2 for phase A
TP5	TRIP_A_OUT	Processed trip command signal which will close relays K3 – K8
TP6	GROUND	Signal ground
TP7	TRIP_B_IN	A logic low trip command for phase B from the RFL 9300
TP8	SPARE	Spare test point
TP9	B_SENSE_1	Logic high when trip current is sensed in trip relay 1 for phase B
TP10	B_SENSE_2	Logic high when trip current is sensed in trip relay 2 for phase B
TP11	TRIP_B_OUT	Processed trip command signal which will close relays K11 – K16
TP12	GROUND	Signal ground
TP13	TRIP_C_IN	A logic low trip command for phase C from the RFL 9300
TP14	SP_CHAS	Logic low used by supervisor module to detect presence of single pole chassis
TP15	C_SENSE_1	Logic high when trip current is sensed in trip relay 1 for phase C
TP16	C_SENSE_2	Logic high when trip current is sensed in trip relay 2 for phase C
TP17	TRIP_C_OUT	Processed trip command signal which will close relays K19 – K24
TP18	GROUND	Signal ground
TP19	TRIP_DISABLE	Trip disable command from RFL 9300. Logic high blocks tripping.
TP20	DISP_DATA	Serial data line from the RFL 9300 display module to the single pole chassis
TP21	CLK_IN	3.584 mHz local oscillator clock
TP22	DISP_CLK	Clock burst from 9300 display module to single pole chassis
TP23	SYS_CLK	2kHz system clock from 9300 used for serial communications to supervisor module
TP24	+15V	+15 Vdc
TP25	-15V	-15Vdc
TP26	+5V	+5Vdc
TP27	TP	Spare test point for factory use only
TP28	TP	Spare test point for factory use only
TP29	TP	Spare test point for factory use only

24.3 THEORY OF OPERATION - HARDWARE

For the following discussion, refer to Figures 24-3 and 24-7.

24.3.1 SYSTEM OVERVIEW

The Single Pole Chassis receives phase specific trip command signals from the 9300 back plane. If the unit is programmed to be in the single pole mode, phases A, B or C can trip independently of the other two phases. If the unit is programmed to be in the three pole mode and any one phase has a trip command, all three phases will trip simultaneously. Each phase (A, B and C) has six “form A” relays that are energized if a trip is active and if the global trip disable is inactive. Trip release will occur based on any one of the following three trip release options:

1. Trip signal no longer received and no dc trip coil current sensed.
2. Trip signal no longer received.
3. 100ms after trip signal no longer received.

The trip release options are programmed into the Display Controller and downloaded to the Single Pole Chassis during system initialization. The Single Pole Chassis is disabled and the trip disable LED is on until the first valid download has been received from the display controller.

One of the trip release options will latch the trip relays until the dc trip coil current drops below 100ma. Two trip relays for each phase have associated sense current capability. The other two trip release options will open the relays regardless of current sense after the trip command is no longer active. One option has no delay to release and the other option will release after a delay of 100 ms. If the sense current relays are active when there is no trip or if the sense current is on for more than 500ms, a current sense alarm signal (alarm #27) is passed to the supervisor. The supervisor look for changes in the target data and alarm status. When a change is detected, the supervisor sends the alarm status and target information to the display controller. When a trip is active or if current is sensed in either of the two relays, the trip and or sense indications are latched into the front panel LEDs of the Single Pole Chassis. These LEDs will remain on even after the trip clears and the sense current goes to zero. When the unit is turned off and then back on again, the old trip target and current sense information is downloaded to the Single Pole Chassis from the Display controller and again the LEDs remain on. This download process uses 2 wires for loading the old target information, single pole/three pole and trip release modes. Resetting the LED targets occurs when the display controller downloads target information with a value of zero. With each download, the Single Pole Chassis initiates a three second LED test where all the LEDs are turned on. After three seconds has expired, the target information downloaded from the display controller is shown on the panel.

The supervisor monitors the operational condition of the Single Pole Chassis. The target and alarm status as well as the trip release codes are passed to the supervisor every 264 ms. This is an indication to the supervisor that the Single Pole Chassis is present and the alarms are off. Each of the phases acts independently. The description below will be for phase A.

24.3.2 TRIP OPERATION

The trip inputs from the phase controllers are a normal high on the 9300 back plane. When the trip becomes active JP1-1 and A_IN go low. If trip disable is also low, a trip signal will go high out of A_TR1. Trip disable will block a trip inside the Actel and through the circuitry associated with TRIP_DIS_OUT. If TRIP_DIS_IN is low, TRIP_DIS_OUT is also low. This turns on Q1 and Q2 which activates relay K1. This supplies power to the tripping relays K3 - K8, K11 - K16 and K19 - K24. Associated with each phase group of relays is a capacitor. For phase A, C14 will be charged up by the +15 Volt supply. If a trip becomes active the relays are energized, and C14 provides the energy to pull in the relays in less than 4ms. When the relays are energized, the voltage on C14 decreases because of the drop across R11, R12 and R66. This lowers the steady state drain on the +15 Volt supply without affecting the operate speed of the relays. A debounce delay is created in the Actel between the A_IN signal and the A_TR1 trip output signal. This delay is from .5 to 1 ms. This results in a total trip delay of less than 5 ms.

24.3.3 CURRENT SENSE

Two of the six relays for Phase A, K3 and K4 are intended to trip a power utility breaker. The current in the contacts of these relays is monitored by relays K9 and K10, which will activate if a current of 250 ma or greater is present in the trip relay. The current sense inputs, A_SENSE1 and A_SENSE2, are debounced in the Actel. If current is present while a trip is active and the trip release is programmed for current sense, the Actel will keep the trip relay energized until the sense current goes to zero. The relay will remain energized even if the trip is no longer active as long as the sense current continues to be present. This is required to keep the contacts in the trip relay from burning out. External relays in the substation are intended to remove the current in the trip relay after the breaker contacts open.

24.3.4 CURRENT SENSE ALARM

A serial message is sent to the supervisor board over a single wire (SV_DAT) JP1-23. The system clock from the supervisor JP1-7 is used to clock messages from the Single Pole Chassis to the supervisor. If the current sense input to the ACTEL (A_SENSE1 or A_SENSE2) is active without any trip signal in at A_IN, the current sense alarm for Phase A will be active in 32 ms. This could only happen if there is a hardware failure in the Single Pole Chassis. This alarm will always be active if a current is sensed for 500 ms or longer.

The supervisor will not accept the signal as an alarm unless it is read twice. If the pulses are not present for more than 500 ms, the supervisor will issue an alarm indicating a problem in the Single Pole Chassis. The clock may have failed or the connector may have been unplugged. The missing serial messages will indicate a broken connection or board failure.

24.3.5 TARGETS (See note below)

If a trip input from the back plane lasts for more than 1ms, the “TRIP” LED is latched on. In addition, if a sense current input from one of the current sense relays lasts for more than 4 ms, the “TC1” or “TC2” LED is latched on. This will be a record of a trip or a sense current, after the trip has released or the sense current has been turned off. The target LEDs can be reset by pressing the reset button on the display controller. The reset will cause a three-second LED test which causes all LEDs to turn on for 3 seconds. If the trip is not active or if the sense current is not active, the LED targets will turn off. If the sense current is still on, the targets will not be reset.

NOTE

A Target is a visual indicator, such as an LED, which remains ON after the event has occurred.

24.3.6 TARGET DOWNLOAD

When the Single Pole Chassis is first turned on, the active targets, current sense targets, three pole/ single pole and trip release code stored in the display controller are sent down to the Single Pole Chassis. A trip may have occurred and the power to the unit was turned off. When the power is turned on again, the target information is still present in the display controller. The Single Pole Chassis does not have battery backup to save the targets and must get the beginning target status from the display controller. After the power is on, any new target information is latched from the trip and sense current signals as described in the TARGET section above.

24.3.7 POWER SUPPLY CIRCUITS

The +15, -15 and +5 volt supplies are monitored by the trip disable circuitry. If any of the supplies are not present, trip is disabled since the relays do not have power to operate.

24.4 THEORY OF OPERATION - SOFTWARE

24.4.1 INITIALIZATION OF THE SINGLE-POLE LOGIC

The Display Controller works closely with the Supervisor Controller to initialize and monitor the interface between the RFL 9300 relay and the Single-Pole chassis.

The Supervisor will test SP_DETECT (JP1-25) to determine if the Single-Pole chassis is present in the system. If it is present, the generic Single-Pole Chassis alarm (Alarm #54) will become active and the alarm message will be transmitted to the Display Controller using DISP_DATA (JP1-5). When the Display Controller is powered, it transmits at least one 16-bit initialization message to the Single-Pole chassis whether it's present in the system or not. This message will contain trip targets, current sense targets, and the trip release code all previously stored in non-volatile ram. The message will also contain a bit signifying whether the system is configured as single-pole or three-pole and a bit signifying whether or not the targets should be loaded or ignored. The Display Controller will continue to send the initialization message to the Single-Pole chassis at 750ms intervals for as long as the alarm remains active. If the Single-Pole chassis is not detected by the Supervisor the alarm will never become active and no further initialization messages will be sent. The format of the initialization message word is shown in Fig. 24-4. The Display Controller provides a clock signal on DISP_CLK (JP1-6) to enable the single-pole logic to clock-in the message bits on the rising edge of each clock cycle.

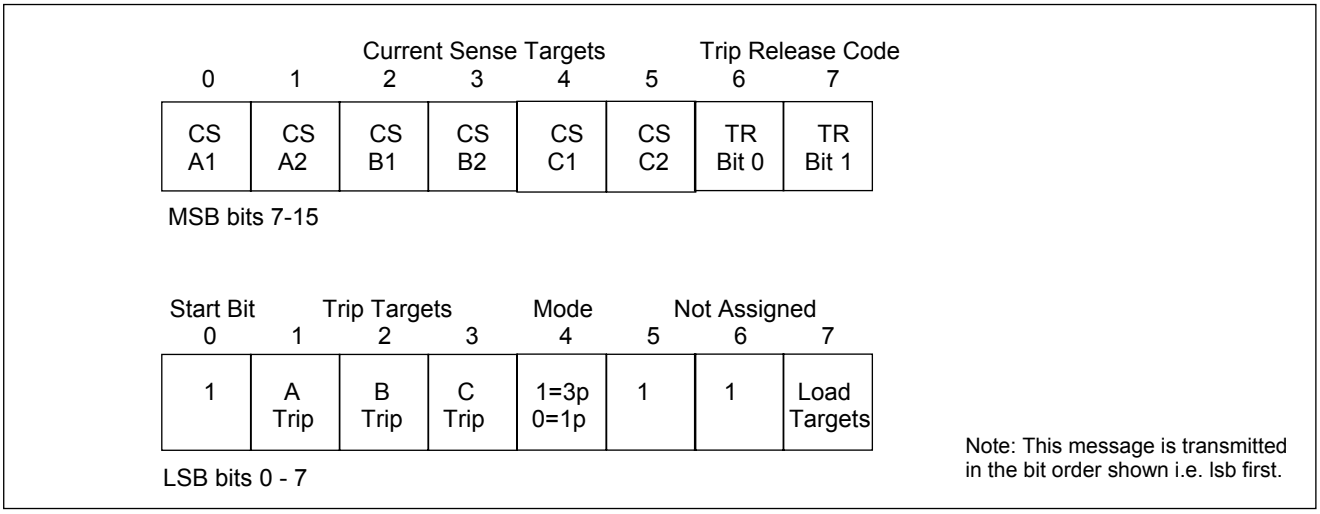


Figure 24-4. Target Message Word sent from the Display Controller to the Single-Pole Chassis

- Start Bit — Bit 0 Always a logic 1
- Target Bits — Bits 1- 3 (Phase [x] Trip) , 8 - 13 (Phase [x] DC Current Sense - read from NV RAM)
  1 = Target On
  0 = Target Off
- Mode Bit — Bit 4 (read from NV RAM)
  0 = Relay configured for single-pole trip
  1 = Relay configured for three-pole trip
- Load Targets — Bit 7
  1 = Ignore target & mode bits
  0 = Accept all bits
- Trip Release Code — Bits 14-15 (read from NV RAM)

Bit 14	Bit 15	
0	0	Trip released when current sensor and trip signals no longer active. Display indication for this code is: CS+TRIP
0	1	Trip released 100ms after trip signal is no longer active. Display indication for this code is: TRIP+100
1	0	Trip released without delay after trip signal is no longer active Display indication for this code is: TRIP+0
1	1	Not used

Once the single-pole logic has been initialized, it will begin transmitting a 16-bit status word (Fig.24-5) to the Supervisor at 264ms intervals. The transmission will be asynchronous with a start bit (active low), 16 data bits and one stop bit (active high) The message bits will be synchronized to the system clock and will be in the mark, or logic 1 condition when no messages are being transmitted. SV_DAT (JP1-23) will be utilized to transmit the message. The first time that the Supervisor detects one of these messages and determines that it is valid, a message will be sent to the Display Controller rescinding the Single-Pole Chassis alarm. On receiving this message the Display Controller will cease sending the initialization message to the single-pole logic.

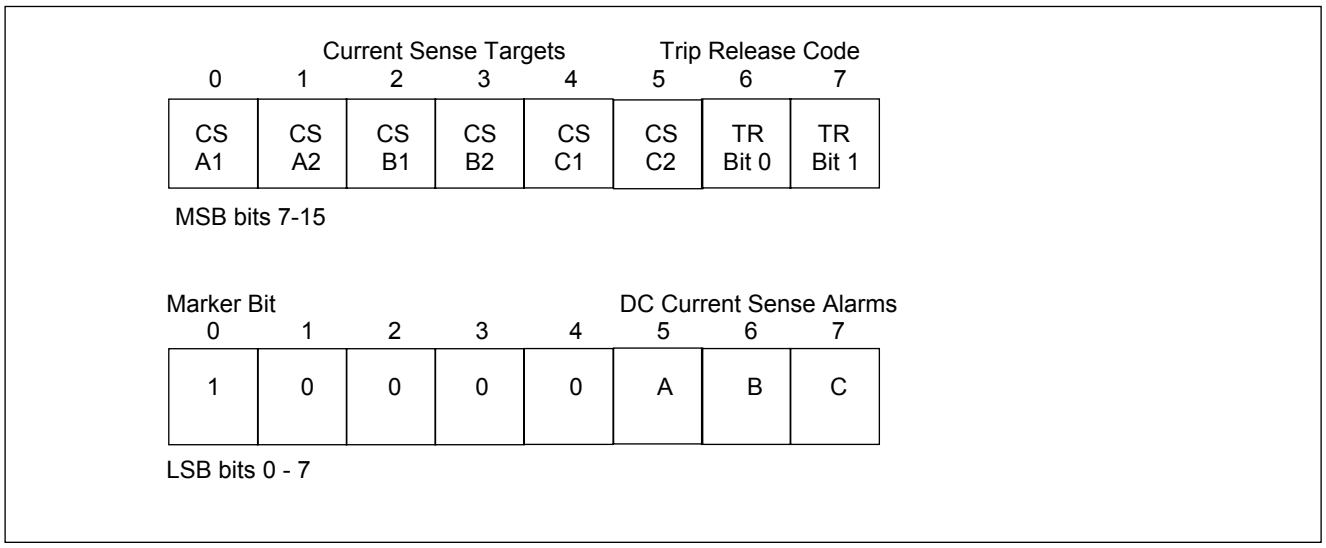


Figure 24-5. 16-bit Status messages transmitted by the Single-Pole logic to the Supervisor at 250ms intervals

- Marker Bit — Bit 0 - Always a logic 1
- Spare Bits — Bits 1- 4
- DC Current Sense Alarm Bits — Bits 5 - 7 (Phase [x])
  1 = Phase (x) Alarm Active
  0 = Phase (x) Alarm not active
- Target Bits — Bits 8 - 13 (Phase [x] DC Current Sense - active)
  1 = Target On
  0 = Target Off
- Trip Release Code — Bits 14-15 (active)

24.4.2 NORMAL OPERATION AFTER INITIALIZATION IS COMPLETE

After initialization, the single-pole logic will continue to transmit its 16-bit status message (Fig.24-5) to the Supervisor at 264ms intervals. The Supervisor will not accept any status changes as valid until it receives two identical messages in succession. If a status change is accepted as valid, the Supervisor will transmit byte 2 of the status message (Fig.24-5) as received from the single-pole logic to the Display Controller. As long as there are no changes in single-pole logic status detected by the Supervisor, byte 2 of every 10th status message (2.64 second interval) will be transmitted to the Display Controller. This is to insure that the Display Controller will not miss a change in single-pole logic status.

When the Display Controller receives this message it will be saved in NV RAM. If the trip release code received from the Supervisor differs from the latest code known to the Display Controller, or if a new trip release code is programmed by the operator, the initialization message (Fig. 24-4) will be transmitted to the single-pole logic, with bit 7 = logic 1. This will signal the single-pole logic to ignore the target & mode bits but to accept the Trip Release code.

If the Supervisor has gone 600ms without receiving a status message from the single-pole logic, or if it detects that the single-pole jumper position on the Supervisor card (J5) has changed, it will declare a SINGLE-POLE CHASSIS ALARM locally and transmit the alarm message to the Display Controller. As long as this alarm remains active the Display Controller will transmit the initialization message with bit 7 = logic 0, at 750ms intervals.

24.4.3 RESET

If there are no SINGLE-POLE CHASSIS ALARMS, once the power-up interval is completed, the only time that the Display Controller will transmit the initialization message with bit 7 = logic 0 is when a reset signal is issued. In that case the message will be transmitted to the single-pole logic with all target bits set at logic 0.

The RESET switch on the front of the Display Assembly serves a dual purpose. When it is pressed, and there are no active trip signals, all LED status indicators on both the Display and Single-Pole Assemblies will be reset after a 3-second LED test. After the LED test is completed, the remaining modules, except for the comms cards in the RFL 9300, will execute a 3-second LED test. If there are any active trip signals on the main chassis a "TRIP ACTIVE" message will appear on the display and the reset signal will have no effect. Even if there are active trip signals detected on the main chassis the reset signal will still be transmitted to the single-pole logic where LED status indicators will be reset only on phases without active trip signals. The RESET switch is also used to reset any alarms generated by the Display Controller. Alarms transmitted to the Display Controller by the RFL 93B SV and the single-pole logic will not be reset when the RESET switch is pressed. These alarms will only be reset when the alarm condition itself disappears. When the single-pole logic is configured for three-pole trip, the reset signal is ignored if there is an active trip on any phase. This differs from the single-pole case where the reset signal is processed on a phase-by-phase basis.

24.4.4 SERIAL COMMUNICATIONS LINK WITH THE SUPERVISOR

The single-pole logic utilizes the SV_DAT (JP1-23), SP_DETECT (JP1-25) and SP_CHASSIS (JP1-26) signal lines to interface with the Supervisor. Messages from the Single-Pole chassis are transmitted on the SV_DAT output. SP_DETECT is used by the Supervisor to detect the presence or absence of the Single-Pole chassis. A low signal on this line indicates that the Single-Pole chassis is connected to the RFL 9300. In order for single-pole trip to be active, SNGPOLE (U1-2) on the 93B SV card, must be a logic low. This can only happen when jumper J5 on the 93B SV card is in the single-pole position (G), and the Single-Pole chassis is connected to the RFL 9300 via a ribbon cable which in turn connects SP_CHASSIS to ground. If the 93B SV detects that any of these connections have changed since the interface with the Single-Pole chassis was initialized it will declare a SINGLE-POLE CHASSIS ALARM locally (#54) and transmit the alarm message to the Display Controller. If the Single-Pole chassis is connected to the RFL 9300 but jumper J5 is in the H position, the Single-Pole chassis is said to be in three-pole mode. In this mode none of the single-pole trip algorithms apply and the RFL 9300 operates as a normal two-terminal or three-terminal relay with six additional output trip contacts per phase.

24.4.5 SINGLE-POLE TRIP ALGORITHMS

Open Breaker - When the RFL 9300 is configured for single-pole operation the open breaker condition is determined on a phase-by-phase basis. Any Phase Controller sending a ZTC signal to the RFL 93B SV will wait to declare its' breaker to be open until the RFL 93B SV returns the open breaker signal.

Reclose Block - The RFL 93B SV monitors all trip signals originating at both the local and remote terminals.. If the RFL 9300 is configured for single-pole trip operation and a trip signal is detected, a 3-second timer is started. If trip signals, originating either at the local or remote terminals, are detected on the remaining two phases before the 3-second timer expires the reclose block output relay will be energized for 50ms.

Selective Pole Relaying - If Selective Pole Relaying is not enabled and multiphase trips are calculated locally, all three single-pole breakers will be tripped and a reclose block output signal will be issued. If Selective Pole Relaying is enabled and multiphase trips are calculated locally, only the breakers on the faulted phases will be tripped. A reclose block output signal will be issued only when a three-phase trip is detected within the required 3-second time window.

Backup Mode Trip - If the RFL 9300 is configured for single-pole trip operation and the relay is operating in backup mode, any trip signal that is calculated locally will result in all three single-pole breakers being tripped and a reclose block signal being issued. This is the case regardless of the status of Selective Pole Relaying which does not apply when backup mode is active. In three-terminal systems it is very possible that during a communications outage between two of the terminals, the third terminal may still be providing differential protection. Only the two terminals experiencing the communications problem may be in backup mode (if enabled). If the third terminal calculates a permissive trip it will transmit trip signals to the two terminals operating in backup mode. Since the trip was not calculated locally these terminals will trip only on the faulted phase(s).

3I0 Trip Algorithm - When the RFL 9300 relay is configured for single-pole operation the GROUND DELAY function takes on an additional role. If GROUND DELAY is not enabled, trips calculated by the 3I0 controller will have no effect. In certain applications, such as tapped loads, the ground bias may be set much more sensitive than the phase bias and only a 3I0 trip signal will be available to clear low-level internal faults. In this case, GROUND DELAY must be enabled to insure that there will be adequate time to allow the individual Phase Controllers to trip their breakers. Then, when the 93B SV receives a trip signal from the 3I0 controller, if none of the other Phase Controllers has issued a trip signal all three will be commanded to trip. It's ok to do this since the 3I0 controller can't pass its trip signal to the 93B SV unless the programmed GROUND DELAY has already expired.

When GROUND DELAY is enabled specifically for the purpose of allowing 3I0 single-pole trips it is recommended that a setting of 50ms be used. Keep in mind that the ground delay timer doesn't start until a 3I0 trip signal would have been issued in a three-pole application i.e. after the normal 3I0 trip delay. This means that with a 50ms setting the timer may not expire until as much as 80 to 90ms after the fault. Remember that trip signals are calculated at the conclusion of positive half-cycles of line current. Should a positive half-cycle terminate just prior to the 50ms time-out it will be an additional 16ms before the 3I0 trip will be passed to the 93B SV which must then pass the trip command to the phase controllers.

24.4.6 SINGLE-POLE ALARMS

The alarms listed below are specific to a single-pole system:

054 - SPT Trip General — Single-pole logic general alarm. Problem on Single-Pole chassis detected by 93B SV . Problem with (or no) serial message sent by SP logic.

055 - PH A SG POLE CS — Phase A single-pole trip alarm: Phase A dc trip current sensed for more than 500ms by single-pole logic or Phase A dc trip current sensed without a Phase A trip signal having been issued.

056 - PH B SG POLE CS — Phase B single-pole trip alarm: Phase B dc trip current sensed for more than 500ms by single-pole logic. Phase B dc trip current sensed without a Phase B trip signal having been issued.

057 - PH C SG POLE CS — Phase C single-pole trip alarm: Phase C dc trip current sensed for more than 500ms by single-pole logic. Phase C dc trip current sensed without a Phase C trip signal having been issued.

Table 24-2. Replaceable parts, RFL 9300 single pole chassis
Assembly No. 106710

Circuit Symbol (Figs. 24-4 & 24-5)	Description	Part Number
	CAPACITORS	
C1-3	Capacitor, electrolytic, 22μF, 100V	1007 1429
C4-13, 15-18, 21, 23-29, 31-34, 36	Capacitor, ceramic dip, 0.1μF, 10%, 50V	0120 38
C14, 22, 30, 37, 38, 39	Capacitor, tantalum, 100μF, 20%, 20V	1007 883
C35	Capacitor, ceramic dip, 0.01μF, 10%, 100V	1007 1390
	RESISTORS	
R1	Resistor, metal film, axial, 49.9K, 1%, 1/4W	0410 1451
R2	Resistor, metal film, axial, 3.01K, 1%, 1/4W	0410 1334
R3, 6	Resistor, metal film, axial, 5.9K, 1%, 1/4W	0410 1362
R4	Resistor, metal film, axial, 6.81K, 1%, 1/4W	0410 1368
R5	Resistor, metal film, axial, 3.16K, 1%, 1/4W	0410 1336
R7, 13, 24, 31, 40, 47, 67	Resistor, metal film, axial, 10K, 1%, 1/4W	0410 1384
R9, 10, 14, 15, 25, 26, 32, 33, 41, 42, 48, 49, 60-65	Resistor, metal film, axial, 1K, 1%, 1/4W	0410 1288
R11, 12, 27, 28, 43, 44, 66, 71, 72	Resistor, metal film, axial, 200Ω, 1%, 1/2W	0410 2221
R16-21, 29, 30, 36-39, 45, 46, 52-55	Resistor, metal film, axial, 69.8Ω, 1%, 1/4W	0410 1177
R22, 23, 34, 35, 50, 51, 56, 57, 58, 68, 69, 70	Resistor, metal film, axial, 499Ω, 1%, 1/4W	0410 1259
R59	Resistor, metal film, axial, 100Ω, 1%, 1/4W	0410 1192
RZ1	Resistor, network, 100K, 9R/PKG	32623
	SEMICONDUCTORS	
CR1-5, 8-10, 12-14	Diode, silicon , rectifier, 1 Amp, 1N4003	30769
CR6, 7, 11	Diode, Schottky, 1 Amp, 20 Volt, 1N5817	30150
Q1	Transistor, silicon, PNP, 2N3906	21565
Q2	Transistor, NPN, 40 Volts, 2N4401	42574
U1	Integrated circuit, MOS, field programmable gate array	0615 450
U2, 3, 4	Transistor, array, ULN2803A	0720 7
	MISCELLANEOUS COMPONENTS	
DS1-2	Optoelectric device, LED, green	32567
DS3-12	Optoelectric device, LED, red	99294
J1	Connector, wafer assembly, 8 circuit	45142 8
J2, 3, 4	Connector, male, 15 pin, DIN41612	102868
JP1	Connector, JK male, 26 pin, vertical	95617
K1, 2	Relay, SPDT, 12 Volt, PCB, sealed	101236
K3-8, 11-16, 19-24	Relay, SPST, 12Vdc, 37.5ma, special	102860
K9, 10, 17, 18, 25, 26	Relay, reed, SPST, 100 Volt, 250ma	102859
TP1-29	Test point, terminal, orange	98441 3
Y1	Crystal, hybrid, clock oscillator, 3.584 mHz	103347

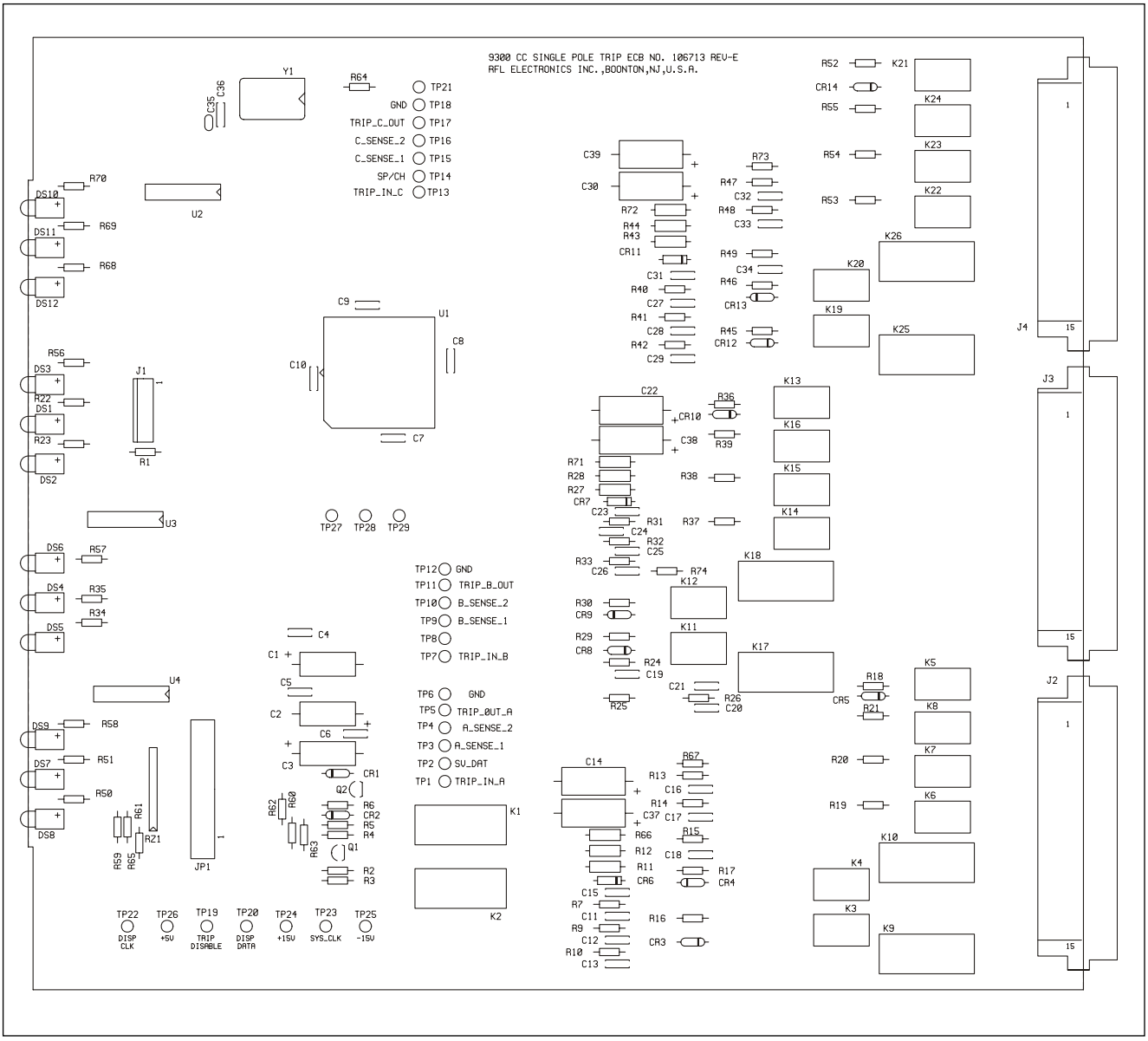


Figure 24-6. Component locator drawing, RFL 9300 single pole chassis, main circuit board (Assembly No. 106710)

Figure 24-7. Schematic, 9300 Single Pole Chassis (Drawing No. D-106714-B) Sheet 1 of 2

Please see Figure 24-7, Sheets 1 of 2 and 2 of 2, in Section 32: Schematics.

Table 24-3. Replaceable parts, RFL 9300 single pole chassis, rear panel assembly (Assembly No. 106705)

Circuit Symbol (Figs. 24-6 & 24-7)	Description	Part Number
C1-36	Capacitor, ceramic disc, 0.005μF, 20%, 3kV	1007 1264
J2, 3, 4	Connector, female, 15 position, DIN41612	102869
TB1A, B	Terminal block, 6 terminal	101233
TB2A, B	Terminal block, 6 terminal	101233
TB3A, B	Terminal block, 6 terminal	101233

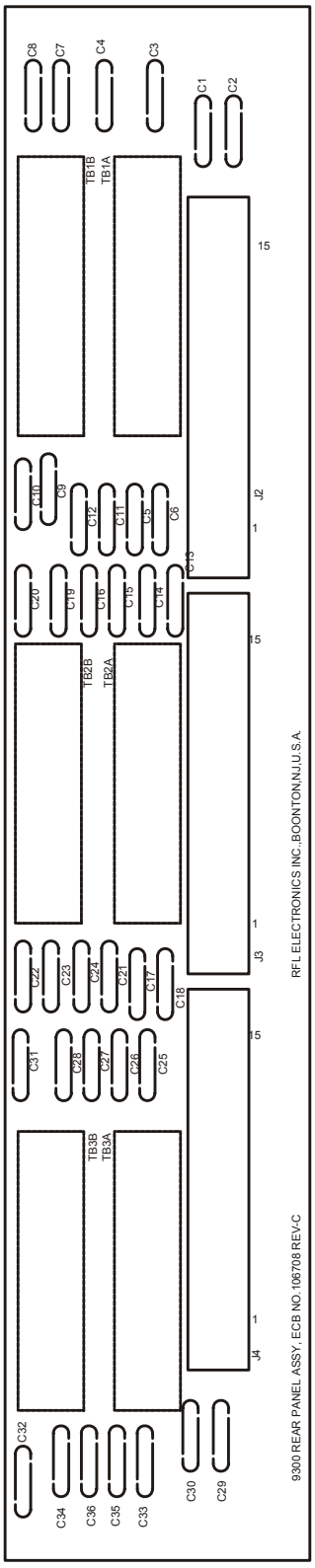


Figure 24-8. Component locator drawing, RFL 9300 single pole chassis, rear panel (Assembly No. 106705)

Figure 24-9. Schematic, 9300 Single Pole Chassis, Rear Panel (Drawing No. D-106709-C)

Please see Figure 24-9, in Section 32: Schematics

This page intentionally left blank

SECTION 25. CHASSIS AND FRONT PANEL RS-232 MODULE

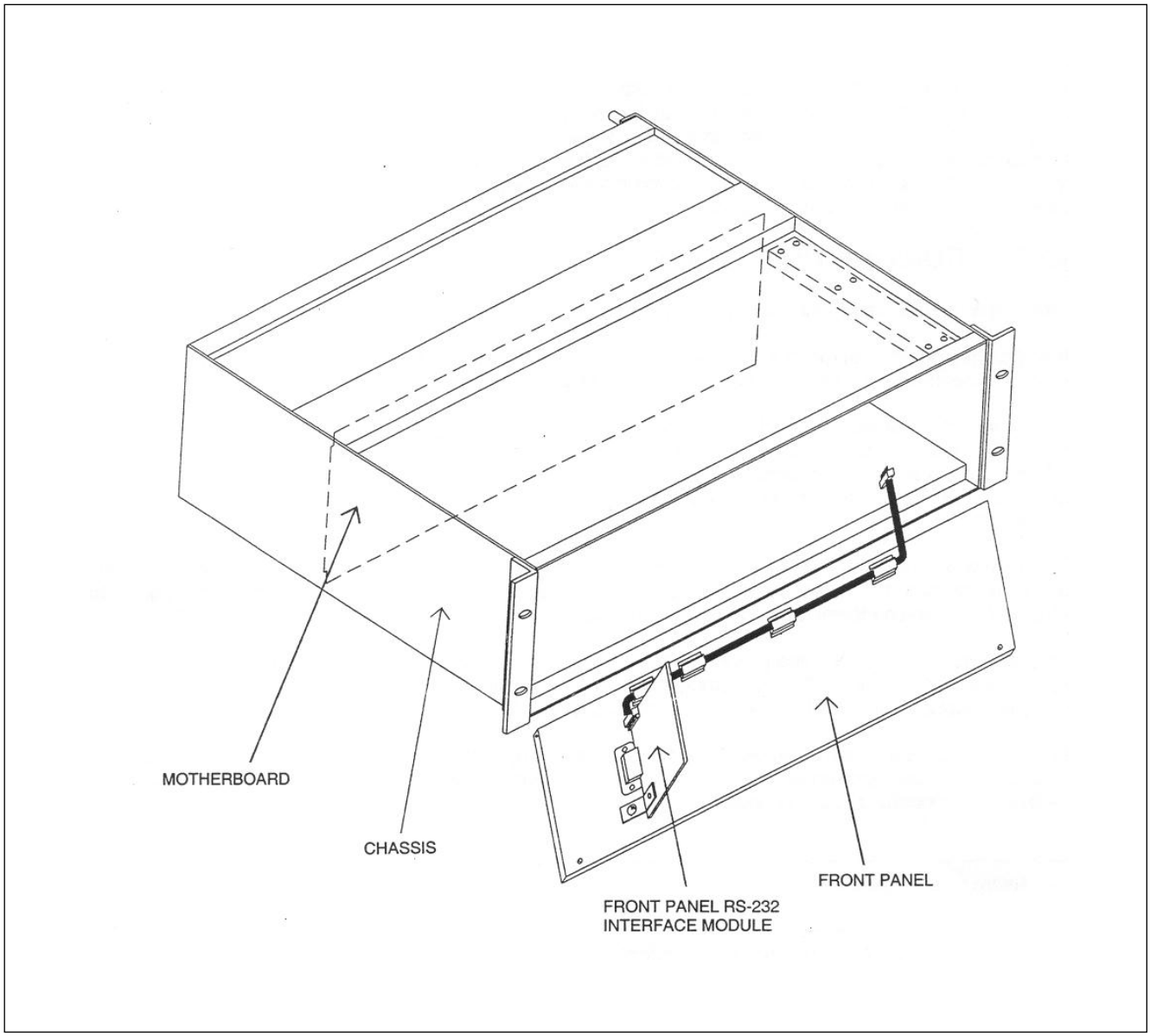


Figure 25-1. Typical RFL 9300 chassis

25.1 DESCRIPTION

The RFL 9300 chassis shown in Figure 25-1 serves as a protective enclosure for all 9300 plug-in modules. It also houses the RFL 93 INTER Interconnect Motherboard and the front panel RS-232 interface module. The motherboard and the RS-232 module can be seen with more detail in Figures 25-3, and 25-5 respectively. Parts lists and schematic diagrams are also included in this section.

25.2 FRONT PANEL RS-232 INTERFACE MODULE

The RS-232 interface module provides the RFL 9300 with a front panel RS-232 port. There is also an RS-232 port on the rear panel of the 9300 chassis which is located on the Relay I/O module. This can be seen in Figure 20-1. The rear panel RS-232 port is normally active. When the front port is activated, the rear port is automatically deactivated. The front port is activated by enabling the DTR line on pin 4 of the standard DB9 female connector. This will normally happen with any communication software running on a laptop. A straight through male to female cable is required for most computers.

25.2.1 THEORY OF OPERATION

For the following discussion, refer to Figures 25-2 and 25-6

The RS232 board (106755) mounts to the front panel of the 9300 and connects via a cable to the Display Controller. It operates in two modes, Pass Through or Insert.

In Pass Through mode the TTL level Transmit and Receive lines coming from the 80C196 on the display controller are converted to RS-232 levels by U1, run through relay K1 and are converted back to TTL levels by U1. These signals are then connected back through the Display Controller to the Relay I/O, where they are routed to the rear RS-232 port. Pass Through mode is invoked whenever nothing is connected to the front RS-232 connector.

In Insert Mode the Transmit and Receive lines from the front RS-232 port are routed via the relay K1 to U1 where they are converted to TTL levels and connected to the Display Controller processor. In this mode the signals from the Relay I/O are disconnected from the rest of the system. Insert Mode is invoked when K1 is energized.

K1 is energized when the DTR line (pin 4 on J1) is active. This normally happens when a PC terminal emulation program takes control of the PC port. A straight through 9-pin cable is all that is needed to drive this signal active. This signal causes Q2 and Q1 to conduct and turn on the relay K1.

If no source for DTR is present, the relay can be forced active by putting jumper JP1 in the B position and using a special cable with pin 1 grounded. This will turn on Q1 and energize the relay. Jumper JP1 should be placed in the A position for normal system operation.

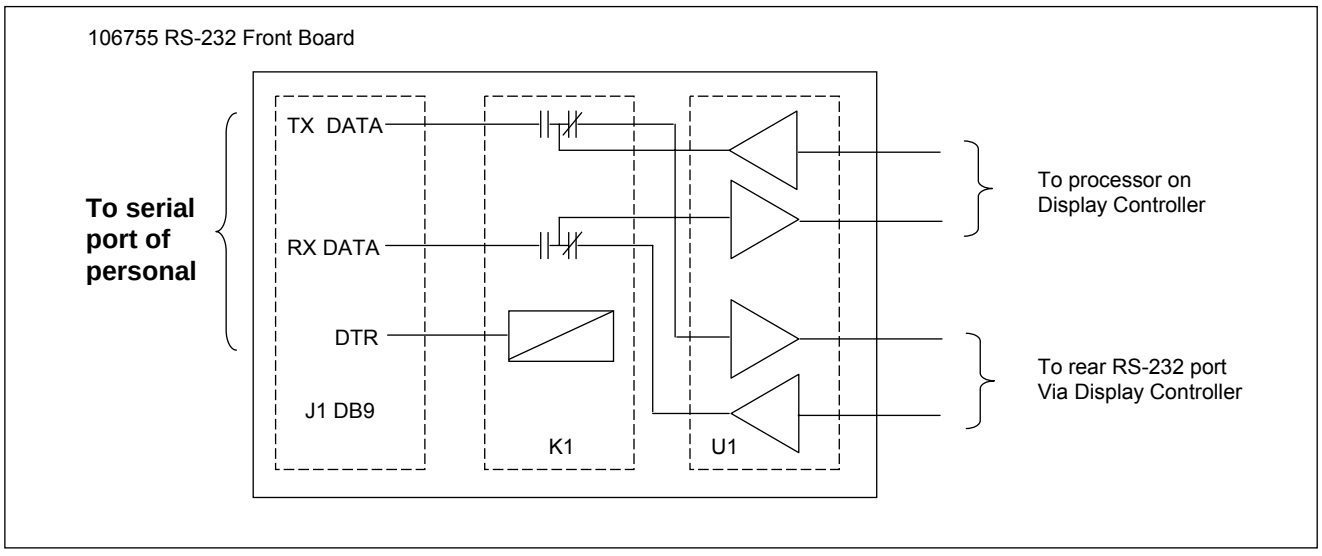


Figure 25-2. Block diagram of RS-232 front board

Table 25-1. Replaceable parts, RFL 93 INTER Interconnected Motherboard Assembly No. 103905-1

Circuit Symbol (Figs. 25-3 & 25-4)	Description	Part Number
C1-3	Capacitor, tantalum, 22uF, 20%, 35V	1007 657
C4-34	Capacitor, ceramic, 0.1uF, 10%, 100V	0130 11041
J1, 4-9, 12, 13	Connector, JK female, 64 contact, DIN	101280 1
J2, 3, 10, 11	Connector, JK female, 64 contact, DIN	101281 1
J14	Connector, male, 26 pin	102863
R1	Resistor, metal film, zero-ohm,1/4-watt	1510 2217

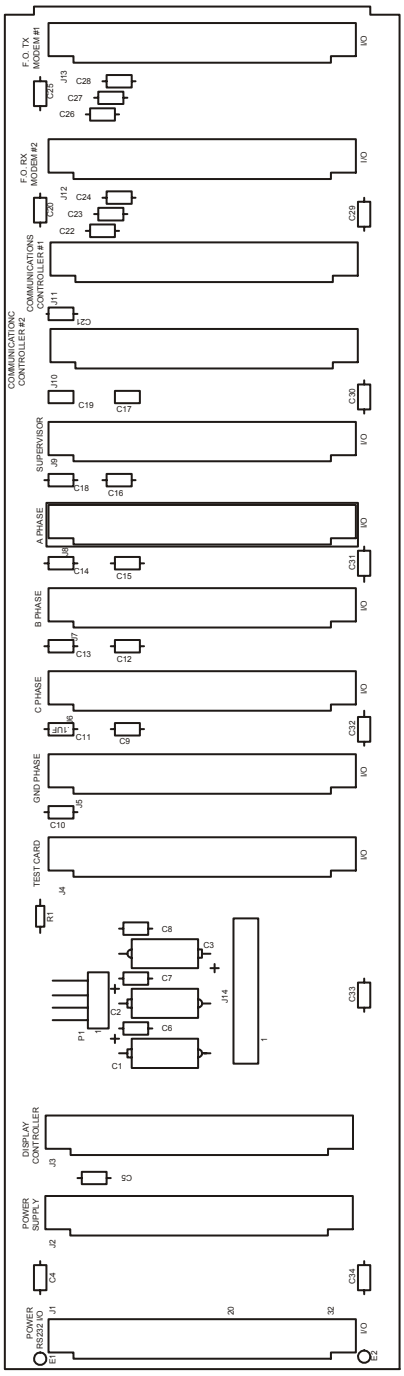


Figure 25-3. Component locator drawing, RFL 93 INTER Interconnect Motherboard (Assembly No. 103905-1; Drawing No. D-103908-1-C)

Figure 25-4. RFL 93 INTER Interconnect Motherboard (Assembly No. 103905-1; Schematic No. D-103909-1-D)

Please see Figure 25- 4, in Section 32: Schematics.

Table 25-2. Replaceable parts, RFL 9300 front panel RS-232 interface module Assembly No. 106755

Circuit Symbol (Figs. 25-5 & 25-6)	Description	Part Number
C1, 2	Capacitor, ceramic, 0.1uF, 10%, 100V	151-10104050608
C3-5, 8-10	Capacitor, ceramic, 0.1uF, 10%, 50V	151-10104040603
C6, 7	Capacitor, electrolytic, 10uf, 35V, 20%	150-05100060103
CR1-4	Suppressor, transient voltage, bidirectional, 27-36V	102986
CR5-7	Diode, general purpose, 1N4148	340-100
J1	Connector, jack, female, 9-pin	30099
J2	Connector, wafer assembly, right angle, 8 circuit	41463-8
JP1	Connector, header, single, 3-circuit	32802-3
K1	Relay, DPDT, 12V, 1028 Ohm	98439
Q1	Transistor, silicon, PNP, 2N2907A	37439
Q2	Transistor, NPN, 40V, 2N4401	42574
R1	Resistor, thick film, 1K, 1%, 1/8 watt	700-15100134
R2-5	Resistor, thick film, 4.99K, 1%, 1/8 watt	700-15499134
R6	Resistor, thick film, 100Ω, 1%, 1/8 watt	700-15100034
U1	Integrated circuit, RS232 driver/receiver, dual	505-100

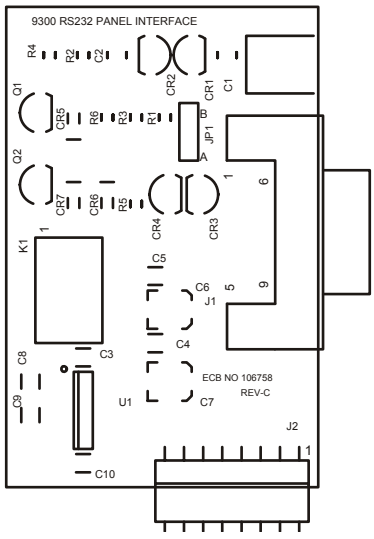


Figure 25-5. Component locator drawing, RFL 9300 front panel RS-232 module (Assembly No. 106755; Drawing No. C-106758-C)

Figure 25-6. RS-232 Front Panel Interface (Assembly No. 106755; Schematic No. C-106759-B)

Please see Figure 25- 6, in Section 32: Schematics.

This page intentionally left blank

SECTION 26: EXPANSION CHASSIS

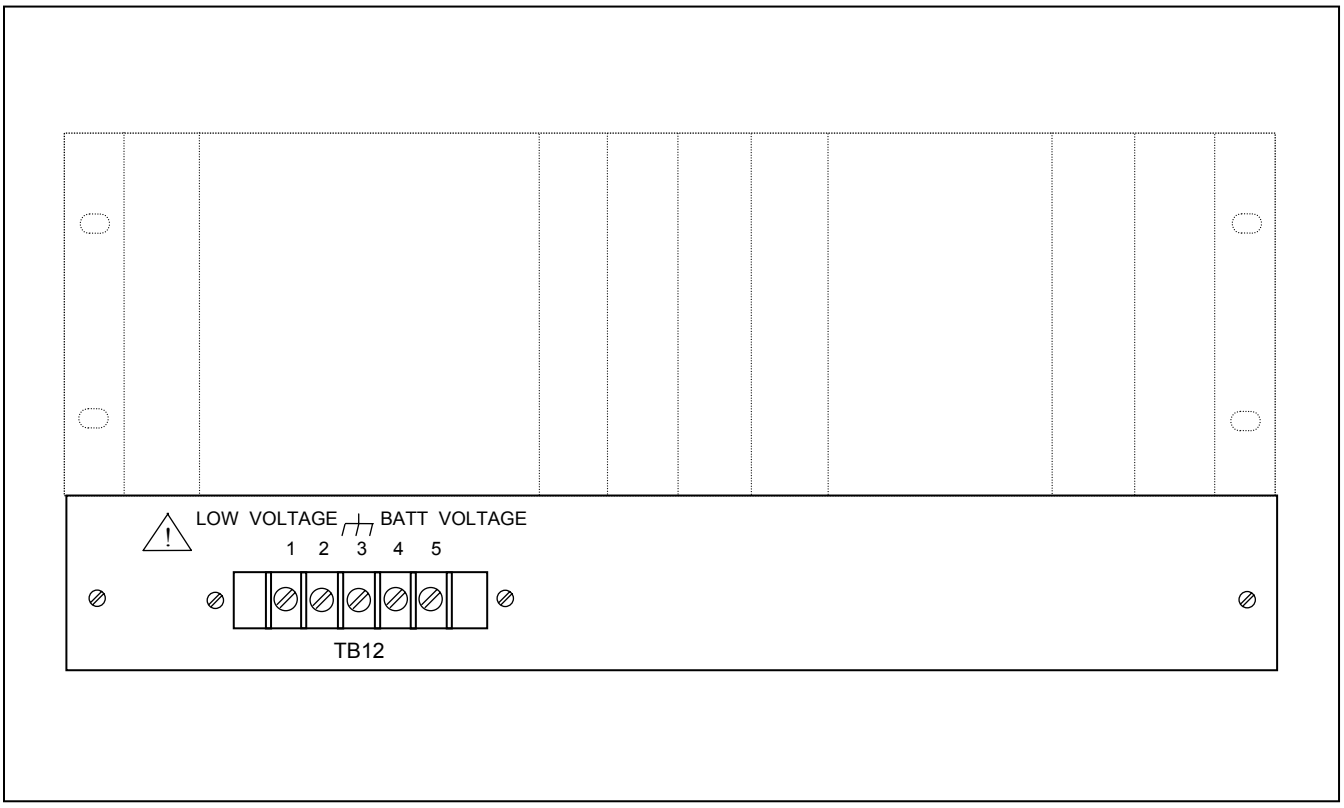


Figure 26-1. Typical RFL 9300 Expansion Chassis, rear view

The rear view of the RFL 9300 expansion chassis is shown in Figure 26-1. The front view of the expansion chassis is not shown since it is a blank panel. The expansion chassis allows the RFL 9300 to operate from 250VDC station battery power. The expansion chassis contains a power supply which converts 250VDC station battery power to 48VDC. The 48VDC is then used to power the RFL 9300 chassis via TB1 at the rear of the Relay I/O module (Section 20). The expansion chassis is an option which is only used in some RFL 9300 installations. Table 26-1 provides general information about the expansion chassis, Table 26-2 is a list of replaceable parts, Figure 26-2 is a component locator drawing, and Figure 26-3 is a schematic diagram.

Table 26-1. Expansion Chassis, General Information

Model Number	Width	Height	Expansion Chassis Assembly Number	Power Supply Assembly Number	Input Voltage Range	Maximum Input Current *
POWER CONV I/O - 250VDC	17.19 in (43.66 mm)	1.718 in (4.36 mm)	105875	106350	210 to 280 VDC	305ma

* Maximum current is drawn when power supply module is operating at full load with minimum voltage present at its input terminals.

Table 26-2. Replaceable parts, RFL 9300 expansion chassis power supply (Assembly No. 106350)

Circuit Symbol (Figs. 26-2 & 26-3)	Description	Part Number
C1,2	Capacitor,ceramic disc,.005μF,20%,3KV	1007 1264
C3	Capacitor,electrolytic,47μF,20%,100V	1007 1484
C4,5,6,7,8,9	Not applicable	
CR5	Suppresor,transient voltage,1.5KE200CA	30266
DS1	Not applicable	
R1,2,3	Not applicable	
F1	Fuse,1/2A,250V,normal-blo	9348
L1,2	Inductor,10μH,5%,1.5A max	30285
L3	Not applicable	
TB1	Terminal block,5 terminal,right angle	101121
U1	Converter,DC-DC,48V,100W	102843
U2	Not applicable	

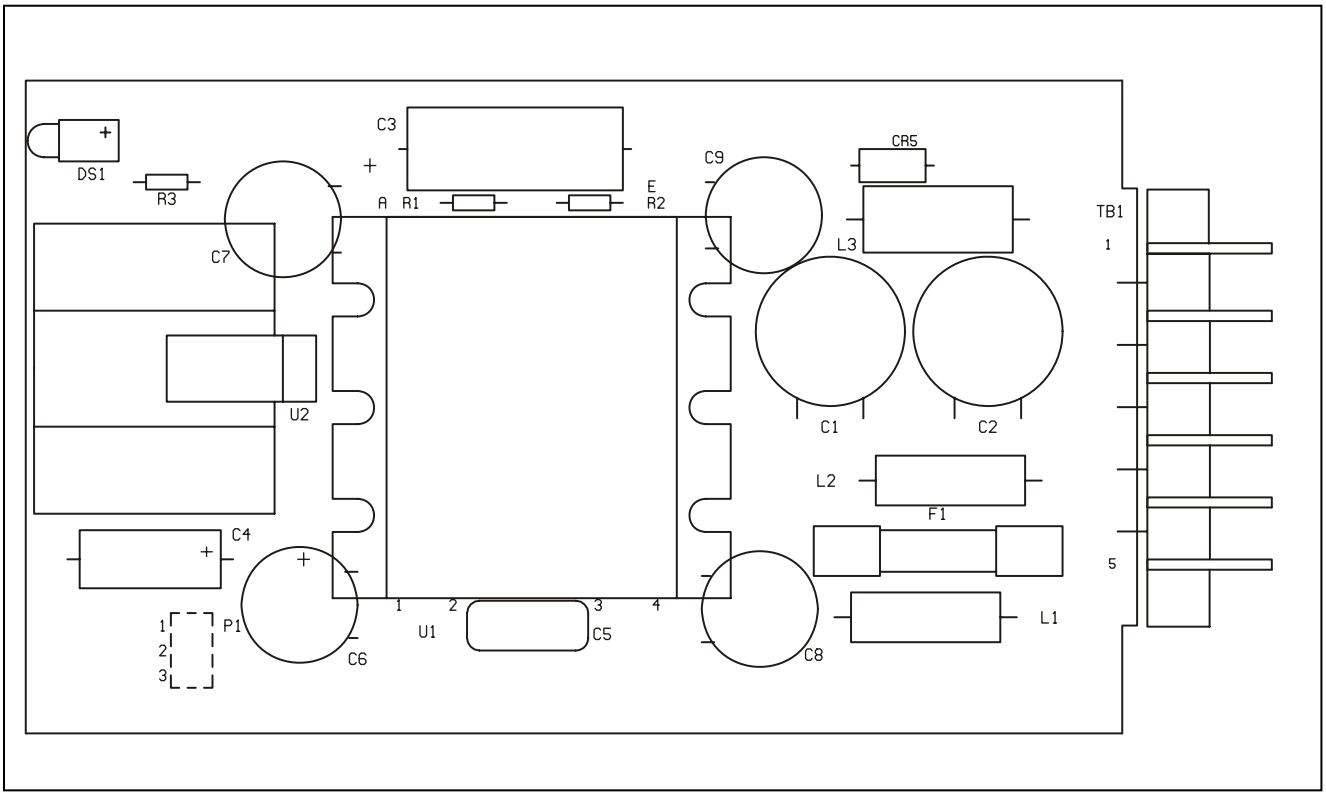


Figure 26-2. Component locator drawing, RFL 9300 expansion chassis power supply (Assembly No. 106350)

Figure 26-3. Schematic, Power Converter I/O – 250 Vdc, For RFL 9300 Charge Comparison System (Assembly No. 106350; Schematic, No. C-106354-B)

Please see Figure 26- 3, in Section 32: Schematics

This page intentionally left blank

SECTION 27. PROTOCOL CONVERTERS

27.1 DESCRIPTION

RFL 9300 Protocol Converters provide standard communications over the Modbus RTU and DNP based substation networks. The converters come in a variety of physical and software variations to suit different applications.

The most common application is with a 2 terminal 93B relay with a single communications path. In this application, the converter is installed in the unused communications adapter slot and is wired to the 9300 relay I/O via an internal cable. This cable brings the RS232 signals that used to go to the rear DB9 connector to the converter. This allows the converter to communicate directly with the 9300 as if it were attached to the rear comms port.

The converter interrogates the 9300 and maps the responses into variables conforming to one of two specifications. Both Modbus and DNP 3.0 are supported. With the appropriate interrogation software the user can get the settings, measured values, and sequence of events data from the relay.

Due to security concerns, RFL has elected not to make settings changeable via the external protocols. These protocols are networked with unknown devices and contain little error checking and no security provisions. In order to make setting changes one must use the front panel keypad or the RS232 port.

27.2 CONFIGURATIONS

The converters are available as two different hardware versions to support operation with an RS232 selector board and without. The typical application does not use the RS232 selector.

The software is available in Modbus RTU and DNP versions. The Modbus is available only for 2 terminal systems. The DNP version is available for 2 and 3 terminal systems.

Table 27-1 lists the versions currently available: Special versions may be available. Contact RFL for more information.

Table 27-1. Protocol Converters currently available

Part Number	Protocol	Terminals	RS232 Selector	Application
106785-1-1	DNP 3.0	2	No	93B
106785-1-2	DNP 3.0	3	No	93B
106785-1-3	DNP 3.0	2	No	93A
106785-1-4	Modbus	2	No	93B
106785-1-5	Modbus	2	No	93A
106785-3-1	DNP 3.0	2	Yes	93B

27.3 CONVERTER OPERATION

When the converter is operating, all access is via the appropriate protocol interrogation software. The user should consult the software supplier for information on its operation.

The 9300 communicates with the converter autonomously on power up. The 9300 shares a common port between the converter and the front RS232 connector. If a PC is connected to the front port the converter will be disconnected. When the PC is disconnected, the converter will resume its connection with the 9300. However, if the PC is connected, the variables in the converter will not update since it cannot communicate with the 9300.

A number of settings in the 9300 facilitate some of the features of the converter. These settings are called print triggers and are used to tell the converter that something of note has taken place in the relay.

27.4 9300 SETUP

The 9300 must be set for 9600 baud, without hardware handshaking in order to communicate with the converter. In the APRIL menu of the 9300 the following parameters must also be enabled when using a protocol converter.

123 Alarm Trigger
124 Trip Trigger
125 Param Trigger

27.5 CONVERTER ADDRESS SELECTION

In order to connect to a network, unique addresses must be programmed into each converter. Failure to do this could result in multiple converters responding to a single request, thereby corrupting all responses from that address. Not only do the addresses need to be unique amongst 9300s, they must also be unique from every other device on the network.

Modbus - The slave address is always set prior to leaving RFL to 0B hex (11 decimal) and is located at point number 04A0 Hex. Using the Modbus master software the user must write the desired address value into this location. Addresses from 1 to FF Hex (1 to 255 decimal) are acceptable.

DNP – The slave address is always set prior to leaving RFL to 5 and is located at location 0000. It is treated as an object 40, variation 2 variable type. A two byte value from 1 to 65,535 must be written to this location.

27.6 SPECIFICATIONS

Operating Temperature	-20 to +55 degrees C
Operating Humidity	90% Relative Humidity non-condensing @ 40 degrees C

27.7 CONNECTIONS

The converters have three basic connection points. The rear external terminal block is used for connections to the Modbus or DNP network. The on board MOLEX connectors are used for connecting to the 9300 serial port. The 64 pin DIN connector provides power to the module. In applications using the RS232 selector, the 64 pin connector also transfers serial signals to that module.

One version of the converter is available with an external connection to the rear RS232 port of the 9300. This allows connection to the 9300 with the standard Relay I/O assembly. In this application, the RS232 cable is attached to the screw terminals on the converter module.

27.8 CABLES

Two different cable assemblies may be supplied with the converter, depending on the application.

105807 – This cable goes from the Relay I/O to the converter along the tray below the other rear mount I/O boards. It can be identified by the 3 pin connector on one end and the 4 pin connector on the other. This cable is used for all applications that use the 106385-0-11 relay I/O and no RS232 selector board.

106723 – This cable goes from the Relay I/O to the converter along the tray below the other rear mount I/O boards. It can be identified by the fact that it has two connectors on each end. It is used in all applications that use the
106385-1 Relay I/O and the RS232 selector board.

27.9 TERMINAL BLOCK PINOUTS

+485	(+RS485 connection)
-485	(-RS485 connection)
GND	(signal ground)
1	(no connection)
2	(no connection)
3	(no connection)

27.10 BLOCK DIAGRAM

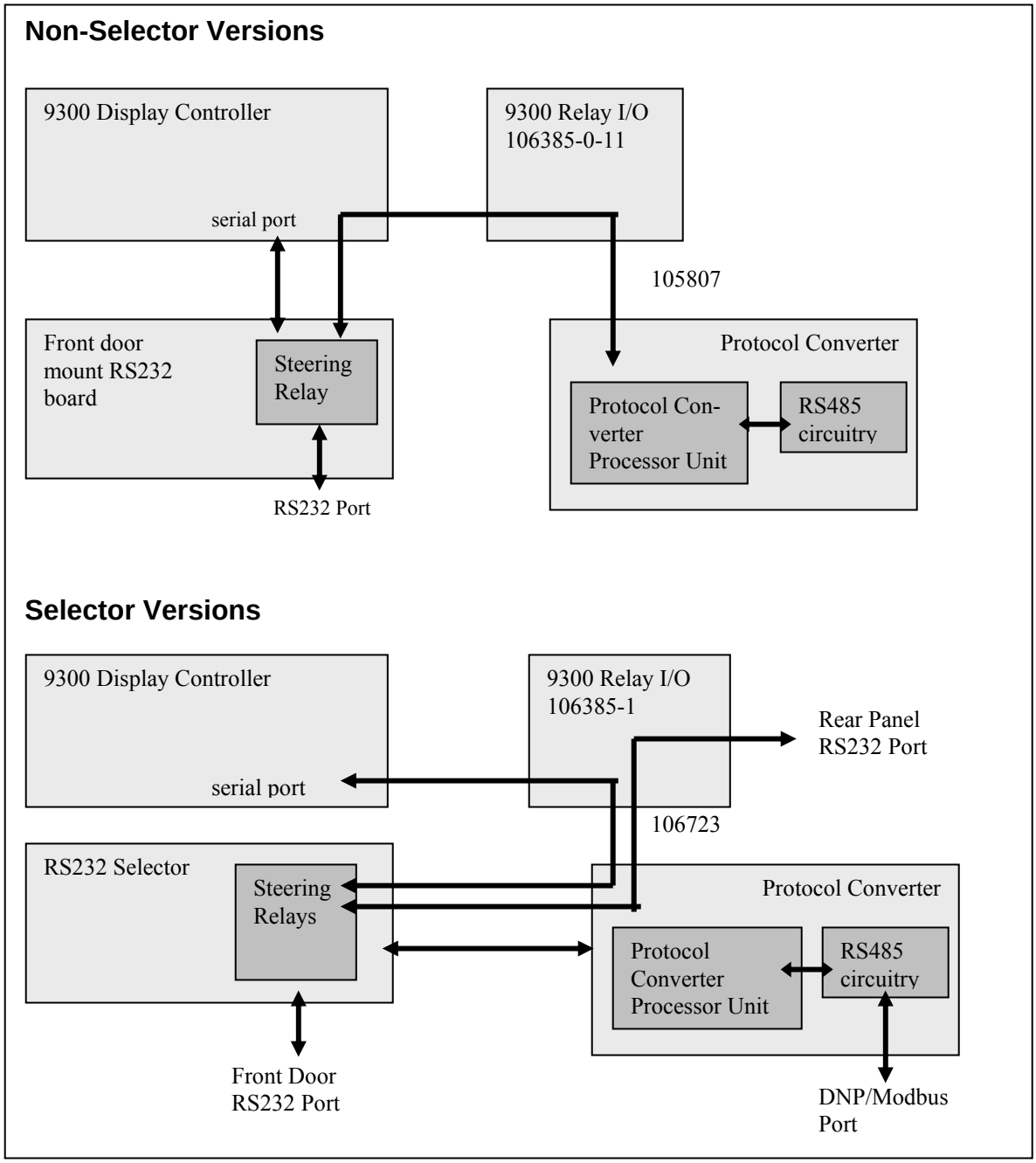


Figure 27-1. Protocol converter block diagram

27.11 MODBUS MAP (Version A3, M13, 9/12/01)

All of the following points are accessible via Modbus RTU. All of the points are type 03 holding registers.

Table 27-2. Modbus Map

Index	Index (Hex)	Description	Units	Format	Write?
1	0000	130 Terminals (2 or 3)	-	F3	No
2	0001	132 CT Full Scale (1: 1 Amp/5 : 5 Amp)	A	F4	No
3	0002	133 Frequency (50 or 60 Hz)	Hz	F5	No
3	0003	140 Single Pole (Inactive:I=73 ascii Active:A=65 ascii)		F20	
4	0004	SW ID CC1	-	F1	No
6	0005	SW ID CC2	-	F1	No
7	0006	SW ID SV	-	F1	No
8	0007	SW ID PCA	-	F1	No
9	0008	SW ID PCB	-	F1	No
10	0009	SW ID PCC	-	F1	No
11	000A	SW ID PCG	-	F1	No
12	000B	SW ID DC	-	F1	No
13	000C	Phase Bias (Amps) value/1000	A	F2	No
14	000D	Ground Bias (Amps) value/1000	A	F2	No
15	000E	Bias Control (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No
16	000F	Ground Bias (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No
17	0010	Bias (seconds) value/100	Sec	F6	No
18	0011	Ground Dly (seconds) value/100	Sec	F6	No
19	0012	F.D. Phase (Amp.) value/10	A	F7	No
20	0013	F.D. Ground (Amp.)	A	F1	No
21	0014	Backup (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No
22	0015	Phase O/C Backup (Amp.) value/1000	A	F2	No
23	0016	Ground O/C Backup (Amp.) value/10000	A	F8	No
24	0017	Phase TOC (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No
25	0018	PH TOC Pickup (Amp.) value/10000	A	F8	No
26	0019	PH TOC Curve (IEC : I=73 Ascii USA : U=85 Ascii)	-	F20	No
27	001A	"PH TOC Curve (1,2,3 or 4)"		F1	No
28	001B	PH TOC Dial value/100	-	F6	No
29	001C	Ground TOC (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No
30	001D	Gd TOC Pickup value/10000	A	F8	No
31	001E	Gd TOC Curve (IEC : I=73 Ascii USA : U=85 Ascii)	-	F20	No
32	001F	"Gd TOC Curve (1,2,3,or 4)"		F1	
33	0020	Gd Toc Dial value/10	-	F7	No
34	0021	Overhd/ Undergd (U= 85 Ascii O=79 Ascii)	-	F20	No
35	0022	Open Conductor (T=84 Ascii A=65 Ascii)	-	F20	No

Table 27-2. Modbus Map - continued

Index	Index (Hex)	Description	Units	Format	Write?
36	0023	Stub Bus (Inactive I=73 Ascii Active A:65 Ascii)	-	F20	No
37	0024	Comms Alm Dly (DisableD=68 Ascii EnableE=69 Ascii)	-	F20	No
38	0025	DC Offset Filter (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No
39	0026	Beeper (DisableD=68 Ascii EnableE=69 Ascii)	-	F20	No
40	0027	Transmit Addr 1 (value/1000)	-	F2	No
41	0028	Comms Mode (A=65 Ascii M=77 Ascii)	-	F20	No
42	0029	Active Channel 1or 2	-	F1	No
43	002A	Guard/Trip (D=68 Ascii I=73 Ascii)	-	F20	No
44	002B	Resest Disp. Alrm (N=78 Ascii Y=89 Ascii)	-	F20	No
45	002C	Alarm Trigger (E=69 Ascii D=68 Ascii)	-	F20	No
46	002D	Single Pole (I=73 Ascii Ascii)	-	F20	No
47	002E	Trip Release Code (+100=1 +0=0 +CS=67 67=C Ascii)	-	F17	No
48	002F	System Label (only first character)	-	F20	No
49	0030	Alarm Number (0 No Alarm)	-	F16	No
71	0046	Trip Counter	-	-	No
72	0047	Fault Detector Counter	-	-	No
1185	04A0	Slave Address		F1	Yes
1351	0546	1 Trip Event? (1=Event Present)		F1	
1352	0547	Trip Code		F22	
1353	0548	Trip record time:Milliseconds in		F10	
1354	0549	six bytes from			
1355	054A	01/01/1970 and Trip			
1356	054B	2 Trip Event? (1=Event Present)		F1	
1357	054C	Trip Code		F22	
1358	054D	Trip record time:Milliseconds in		F10	
1359	054E	six bytes from			
1360	054F	01/01/1970 and Trip			
1361	0550	3 Trip Event? (1=Event Present)		F1	
1362	0551	Trip Code		F22	
1363	0552	Trip record time:Milliseconds in		F10	
1364	0553	six bytes from			
1365	0554	01/01/1970 and Trip			
1366	0555	4 Trip Event? (1=Event Present)		F1	
1367	0556	Trip Code		F22	
1368	0557	Trip record time:Milliseconds in		F10	
1369	0558	six bytes from			
1370	0559	01/01/1970 and Trip			
1371	055A	5 Trip Event? (1=Event Present)		F1	
1372	055B	Trip Code		F22	
1373	055C	Trip record time:Milliseconds in		F10	

Table 27-2. Modbus Map - continued

Index	Index (Hex)	Description	Units	Format	Write?
1374	055D	six bytes from			
1375	055E	01/01/1970 and Trip			
1376	055F	6 Trip Event? (1=Event Present)		F1	
1377	0560	Trip Code		F22	
1378	0561	Trip record time:Milliseconds in		F10	
1379	0562	six bytes from			
1380	0563	01/01/1970 and Trip			
1381	0564	7 Trip Event? (1=Event Present)		F1	
1382	0565	Trip Code		F22	
1383	0566	Trip record time:Milliseconds in		F10	
1384	0567	six bytes from			
1385	0568	01/01/1970 and Trip			
1386	0569	8 Trip Event? (1=Event Present)		F1	
1387	056A	Trip Code		F22	
1388	056B	Trip record time:Milliseconds in		F10	
1389	056C	six bytes from			
1390	056D	01/01/1970 and Trip			
1391	056E	9 Trip Event? (1=Event Present)		F1	
1392	056F	Trip Code		F22	
1393	0570	Trip record time:Milliseconds in		F10	
1394	0571	six bytes from			
1395	0572	01/01/1970 and Trip			
1396	0573	10 Trip Event? (1=Event Present)		F1	
1397	0574	Trip Code		F22	
1398	0575	Trip record time:Milliseconds in		F10	
1399	0576	six bytes from			
1400	0577	01/01/1970 and Trip			
1401	0578	11 Trip Event? (1=Event Present)		F1	-
1402	0579	Trip Code		F22	
1403	057A	Trip record time:Milliseconds in		F10	
1404	057B	six bytes from			
1405	057C	01/01/1970 and Trip			
1406	057D	12 Trip Event? (1=Event Present)		F1	
1407	057E	Trip Code		F22	
1408	057F	Trip record time:Milliseconds in		F10	
1409	0580	six bytes from			
1410	0581	01/01/1970 and Trip			
1411	0582	13 Trip Event? (1=Event Present)		F1	
1412	0583	Trip Code		F22	
1413	0584	Trip record time:Milliseconds in		F10	
1414	0585	six bytes from			
1415	0586	01/01/1970 and Trip			
1416	0587	14 Trip Event? (1=Event Present)		F1	
1417	0588	Trip Code		F22	
1418	0589	Trip record time:Milliseconds in		F10	

Table 27-2. Modbus Map - continued

Index	Index (Hex)	Description	Units	Format	Write?
1419	058A	six bytes from			
1420	058B	01/01/1970 and Trip			
1421	058C	15 Trip Event? (1=Event Present)		F1	
1422	058D	Trip Code		F22	
1423	058E	Trip record time:Milliseconds in		F10	
1424	058F	six bytes from			
1425	0590	01/01/1970 and Trip			

Table 27-3. Modbus RTU Format Table

Format	Description	Values Permitted and Examples
F1	Integer 2 Bytes	From 0 at 65535
F2	Integer 2 Bytes Decimal point (/1000)	From 0 at 6553.5 i.e. 1000 to be read as 1.0
F3	Integer 2 Bytes (Encoded)	2 for 2 terminal 3 for 3 terminal
F4	Integer 2 Bytes (Encoded)	1 for 1 Amp. 5 for 5 Amp.
F5	Integer 2 Bytes	50 for 50HZ 60 for 60HZ
F6	Integer Bytes Decimal point (/100)	0 at 655.35 i.e. 100 to be read as 1.00
F7	Integer Bytes Decimal point (/10)	0 at 6553.5 i.e. 10 to be read as 1.0
F8	Integer Bytes Decimal point (/10000)	0 at 6.5535 i.e. 10000 to be read as 1.0
F10	Event in ms From 01/01/1970	i.e. Dir Value 060EH 1 (data TRUE) 060FH 10123 0610H 48318 0611H 98 NUMBER IS 984831810123 ms From 01/01/1970, this event time is 17/03/2001 12:23:30.123
F16	Alarm Code 2 Byte integer	i.e. 34= SV Parallel Port 00= no alarm
F17	Code Trip Release	+100=1 +0=0 +CS=67 67=C Ascii
F20	Integer Bytes	ASCII
F22	2 Byte Integer	Trip Codes as Follows: 0 - A phase Trip 1 – B phase trip 2 - C phase Trip 3 – 3I0 phase trip 4 - A &B Trip 5 – A & C trip 6 - A & 3I0 Trip 7 – B & C trip 8 - B & 3I0 Trip 9 – C & 3I0 trip 10 - A&B&3I0 Trip 11 – B&C&3I0 trip 12 - A&C&3I0 Trip 13 – ABC&3I0 trip 14 - A&B&C Trip 16 - DTT Received 17 – DTT Transmitted

27.12 DNP PROFILE DOCUMENT

DNP V3.00
DEVICE PROFILE DOCUMENT

Vendor Name: RFL Electronics Inc.

Device Name: RFL 9300 DNP Converter version 106775 –x –1

Highest DNP Level Supported:	Device Function:
For Requests Level 2 For Responses Level 2	□ Master □ Slave

Notable objects, functions, and/or qualifiers supported in addition to the Highest DNP Levels Supported (the complete list is described in the attached table):

Maximum Data Link Frame Size (octets):	Maximum Application Fragment Size (octets):
Transmitted 249 Received 292	Transmitted 2048 Received 2048

Maximum Data Link Re-tries:	Maximum Application Layer Re-tries:
None	None

Requires Data Link Layer Confirmation:

Never

Requires Application Layer Confirmation:

When reporting Event Data (Slave devices only)

Timeouts while waiting for:

Data Link Confirm	None
Complete Appl. Fragment	None
Application Confirm	Fixed at 5000 ms
Complete Appl. Response	None

Sends/Executes Control Operations:

WRITE Binary Outputs	Never
SELECT/OPERATE	Never
DIRECT OPERATE	Never
DIRECT OPERATE - NO ACK	Never
Count > 1	Never
Pulse On	Never
Pulse Off	Never
Latch On	Never
Latch Off	Never
Queue	Never
Clear Queue	Never

Reports Binary Input Change Events when no specific variation requested: Never	Reports time-tagged Binary Input Change Events when no specific variation requested: Never
Sends Unsolicited Responses: Never	Sends Static Data in Unsolicited Responses: Never .
Default Counter Object/Variation: Default Object Default Variation Point-by-point list attached	Counters Roll Over at: 16 Bits 32 Bits

Sends Multi-Fragment Responses: No

27.13 DNP POINT LIST (Version A1,M13,8/3/01)

Table 27-4. POINT LIST FOR: 16 bit Analog without Flag (Object 30 Var 4)

Index	Description	Units	Format	Write?	Default
0000	130 Terminals (2 or 3)	-	F3	No	0
0001	132 CT Full Scale (1: 1 Amp/5: 5 Amp)	-	F4	No	0
0002	133 Frequency (50 or 60 Hz)	-	F5	No	0
0003	140 Single Pole (Inactive:I=73 ASCII Active: A=65 ASCIII)		F20		
0004	SW ID CC1	-	F1	No	0
0005	SW ID CC2	-	F1	No	0
0006	SW ID SV	-	F1	No	0
0007	SW ID PCA	-	F1	No	0
0008	SW ID PCB	-	F1	No	0
0009	SW ID PCC	-	F1	No	0
0010	SW ID PCG	-	F1	No	0
0011	SW ID DC	-	F1	No	0
0012	Phase Bias (Amp) value/1000	A	F2	No	0
0013	Ground Bias (Amp)	A	F1	No	0
0014	Bias Control (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No	0
0015	Ground Bias (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No	0
0016	Bias (seg.) value/10	Sec	F7	No	0
0017	Ground Dly (seg.)	Sec	F1	No	0
0018	F.D. Phase (Amp.) value/10	A	F7	No	0
0019	F.D. Ground (Amp.)	A	F1	No	0
0020	Backup (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No	0
0021	Phase O/C Backup (Amp.) value/10000	A	F8	No	0
0022	Ground O/C Backup (Amp.) value/10000	A	F8	No	0
0023	Phase TOC (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No	0
0024	PH TOC Pickup (Amp.) value/1000	-	F2	No	0
0025	PH TOC Curve (IEC: I=73 Ascii USA: U=85 Ascii)	-	F20	No	0
0026	PH TOC Curve (1,2,3 or 4)		F1	No	
0027	PH TOC Dial value/100	-	F6	No	0
0028	GroundTOC (Disable D=68 Ascii Enable E=69 Ascii)	-	F20	No	0
0029	Gd TOC Pickup value/1000	-	F2	No	0
0030	Gd TOC Curve (IEC: I=73 Ascii USA: U=85 Ascii)	-	F20	No	0
0031	Gd TOC Curve (1,2,3,or 4)		F1		
0032	Gd Toc Dial value/10	-	F7	No	0
0033	Overhd/ Undergd (U= 85 Ascii O=79 Ascii)	-	F20	No	0
0034	Open Conductor (T=84 Ascii A=65 Ascii)	-	F20	No	0
0035	Stub Bus (Inacctive I=73 Ascii Active A:65 Ascii)	-	F20	No	0
0036	Comms Alm Dly (DisableD=68 Ascii EnableE=69 Ascii)	-	F20	No	0
0037	DC Offset Filter (DisableD=68 Ascii EnableE=69 Ascii)	-	F20	No	0
0038	Beeper (DisableD=68 Ascii EnableE=69 Ascii)	D	F20	No	All 1s
0039	Transmit Addr 1 (value/1000)	D	F2	No	All 1s

Table 27-4. POINT LIST FOR: 16 bit Analog Without Flag (Object 30 Var 4) - continued

Index	Description	Units	Format	Write?	Default
0040	Comms Mode (A=65 Ascii M=77 Ascii)	T	F20	No	All 1s
0041	Active Channel 1or 2	-	F1	No	All 1s
0042	Guard/Trip (D=68 Ascii I=73 Ascii)	-	F20	No	0
0043	Resest Disp. Alrm (N=78 Ascii Y=89 Ascii)	-	F20	No	0
0044	Alarm Trigger (E=69 Ascii D=68 Ascii)	-	F20	No	0
0045	Single Pole (I=73 Ascii A=65 Ascii)	-	F20	No	0
0046	Trip Release (+100=1 +0=0 +CS=67 67=C Ascii)	-	F17	No	0
0047	System Label (only one char)	-	F20	No	0
0048	Alarm Status (0 No Alarm)	-	F16	No	0
0049	Osc. Phase A Data 1	-	-	No	0
0050	Osc. Phase B Data 1	-	-	No	0
0051	Osc. Phase C Data 1	-	-	No	0
0052	Osc. Phase 3IO Data 1	-	-	No	0
------	--------	-	-	No	0
------	--------	-	-	No	0
0845	Osc. Phase A Data 200	-	-	No	0
0846	Osc. Phase B Data 200	-	-	No	0
0847	Osc. Phase C Data 200	-	-	No	0
0848	Osc. Phase 3IO Data 200	-	-	No	0
0849	Osc. Algorith Code 1	-	-	No	0
0850	Osc. Algorith Code 2	-	-	No	0
0851	Osc. Algorith Code 3	-	-	No	0
------	--------				
------	--------				
1047	Osc. Algorith Code 199	-	-	No	0
1048	Osc. Algorith Code 200	-	-	No	0

Table 27-5. POINT LIST FOR: Binary Input Change with Tim (Object 02 Var 2)

Index	Description	Units	Format	Write?	Default
0000	Last Alarm	-	-	No	-
0001	Historic Alarm 1	-	-	No	-
0002	Historic Alarm 2	-	-	No	-
0003	Historic Alarm 3	-	-	No	-
0004	Historic Alarm 4	-	-	No	-
0005	Historic Alarm 5	-	-	No	-
0006	Historic Alarm 6	-	-	No	-
0007	Historic Alarm 7	-	-	No	-
0008	Historic Alarm 8	-	-	No	
0009	Historic Alarm 9	-	-	No	
0010	Oscillography Data Status (Osc. Date Time)	-	-	No	

Table 27-6. POINT LIST FOR: 16 bit Analog With Time (Object 32 Var 4)

Index	Description	Units	Format	Write?	Default
0000	Last Trip	-		No	
0001	Historic Trip 1			No	
0002	Historic Trip 2			No	
0003	Historic Trip 3			No	
0004	Historic Trip 4			No	
0005	Historic Trip 5			No	
0006	Historic Trip 6			No	
0007	Historic Trip 7			No	
0008	Historic Trip 8			No	
0009	Historic Trip 9			No	
0010	Historic Trip 10			No	
0011	Historic Trip 11			No	
0012	Historic Trip 12			No	
0013	Historic Trip 13			No	
0014	Historic Trip 14			No	

Table 27-7. POINT LIST FOR: 16 bit Analog Output Status (Object 40 Var 2)

Index	Description	Units	Format	Write?	Default
0000	DNP Slave Address		F1	Yes	05
0001	To Request Oscillography Data	-	-	-	-

Table 27-8. Format Table

Format	Description	Values Permitted and Examples
F1	Integer 2 Bytes	From 0 at 65535
F2	Integer 2 Bytes Decimal point (/1000)	From 0 at 6553.5 i.e. 1000 to be read as 1.0
F3	Integer 2 Bytes (Encoded)	2 for 2 terminal 3 for 3 terminal
F4	Integer 2 Bytes (Encoded)	1 for 1 Amp. 5 for 5 Amps.
F5	Integer 2 Bytes	50 for 50HZ 60 for 60HZ
F6	Integer Bytes Decimal point (/100)	0 at 655.35 i.e. 100 to be read as 1.00
F7	Integer Bytes Decimal point (/10)	0 at 6553.5 i.e. 10 to be read as 1.0
F8	Integer Bytes Decimal point (/10000)	0 at 6.5535 i.e. 10000 to be read as 1.0
F10	Event in ms From 01/01/1970	i.e. Dir Value 060EH 1 (data TRUE) 060FH 10123 0610H 48318 0611H 98 NUMBER IS 984831810123 ms From 01/01/1970, this event time is 17/03/2001 12:23:30.123
F16	Alarm Code 2 Byte integer	i.e. 34= SV Parallel Port 00= no alarm
F17	Code Trip Release	+100=1 +0=0 +CS=67 67=C Ascii
F20	Integer Bytes	ASCII
F22	2 Byte Integer	Trip Codes as Follows: 0 - A phase Trip 1 – B phase trip 2 - C phase Trip 3 – 3I0 phase trip 4 - A &B Trip 5 – A & C trip 6 - A & 3I0 Trip 7 – B & C trip 8 - B & 3I0 Trip 9 – C & 3I0 trip 10 - A&B&3I0 Trip 11 – B&C&3I0 trip 12 - A&C&3I0 Trip 13 – ABC&3I0 trip 14 - A&B&C Trip 16 - DTT Received 17 – DTT Transmitted

This page intentionally left blank

SECTION 28. MAINTENANCE

28.1 INTRODUCTION

This section provides maintenance instructions for the RFL 9300 Charge Comparison System. Topics discussed include alarm codes, removal and replacement procedures, fuse replacement, corrective maintenance information, and instructions for converting a 3-Terminal 9300 to a 2-Terminal 9300. Information is also provided on how to arrange for servicing by RFL personnel.

28.2 ALARM CODES

The RFL 9300 senses and detects many different conditions that will cause an alarm. If any of these conditions exists, the word "ALARM" appears on the top line of the display and one or more code numbers appears on the bottom line of the display. At the same time, a beeper will sound intermittently if the beeper has been enabled.

Alarm codes beginning with a "1" mean that a failure has been detected in the RFL 93B DISPLAY module. These alarms may only be reset by pressing the RESET switch on the front of the display module.

10 Local Display Controller Alarm: Nine seconds has elapsed without RFL 93B SV module communications taking place.

12 Local Display Controller Alarm: No acknowledgment has been received from the Supervisor Module for 200 ms.

13 Local Display Controller Alarm: Three non-acknowledgments (NAKs) from Supervisor Module.

14 Oscillography Controller Alarm: Display Controller has lost communication with Oscillography Board.

15 Local Display Controller Alarm: Non-volatile RAM failure on Display Controller.

16 Transmit Address 1: Verification of Local and Remote Address has failed.

17 Transmit Address 2: Verification of Local and Remote Address has failed. (This alarm code is not present in two terminal systems)

Alarm Codes beginning with a "2" mean that a failure has been detected in the trip relays' current sensors. These alarms may only be reset by pressing the RESET switch on the front of the display module.

20 Reserved for future use

21 Reserved for future use

22 Reserved for future use

23 Reserved for future use

24 Display Controller Trip Alarm: DTT dc trip current sensed for more than 500 ms.

25 Display Controller Trip Alarm: Current Sense circuit failure.

27 Display Controller Trip Alarm: DC trip current sensed for more than 500 ms.

Alarm codes beginning with a "3" or a "4" point out conditions detected in other modules in the RFL 9300. These can only be cleared when the condition causing the alarm has returned to normal.

30 Local Alarm From Supervisor Module: Local Charge Comparison Trip without fault detector - ground subsystem.

31 Local Alarm From Supervisor Module: Local Charge Comparison Trip without fault detector - Phase A.

32 Local Alarm From Supervisor Module: Local Charge Comparison Trip without fault detector - Phase B.

33 Local Alarm From Supervisor Module: Local Charge Comparison Trip without fault detector - Phase C.

34 Local Alarm From Supervisor Module: Parallel Port Alarm.

35 Local Alarm From Supervisor Module: Software Mismatch Alarm.

37 General Alarm: Remote #1 Configuration Mismatch.

40 Reserved for future use.

41 Reserved for future use.

42 Reserved for future use.

43 Reserved for future use.

44 Reserved for future use.

45 Local Alarm: Open Conductor Alarm.

46 General Alarm: Systems Communications Alarm.

47 General Alarm: Remote #2 Configuration Mismatch. (This alarm code is not present in two terminal systems)

54 Single-Pole Logic: General Alarm (This alarm code is only present in single-pole systems)

55 Single-Pole Trip Alarm: Phase A DC trip current sensed for more than 500ms (This alarm code is only present in single-pole systems)

56 Single-Pole Trip Alarm: Phase B DC trip current sensed for more than 500ms (This alarm code is only present in single-pole systems)

57 Single-Pole Trip Alarm: Phase C DC trip current sensed for more than 500ms (This alarm code is only present in single-pole systems)

60 Phase A Controller: General Alarm

61 Phase B Controller: General Alarm

62 Phase C Controller: General Alarm

63 3I0 Controller: General Alarm

When all alarms are cleared, the display will return to the moving dot pattern, and the beeper will stop sounding.

CAUTION

Make sure the power switch on the RFL 9300's power supply module is in the OFF position before attempting to remove or replace any circuit board module or I/O module. System performance cannot be guaranteed if modules are removed or replaced with the power supply energized.

28.3 REMOVAL AND REPLACEMENT

The following paragraphs provide procedures to be used when removing and replacing RFL 9300 circuit board modules and I/O modules.

28.3.1 CIRCUIT BOARD MODULES

RFL 9300 circuit board modules are mounted bookshelf-style at the front of the RFL 9300 chassis. Each module is held in place by card guides at the top and bottom of the chassis.

CAUTION

Each module position in the front of the RFL 9300 is keyed to accept a specific module type, as indicated by a label along the front of the chassis. Modules can be damaged if they are installed in the wrong chassis slot. When removing and replacing modules, use the label in the chassis as a guide to make sure each module is in the proper slot.

To remove any of these circuit board modules, proceed as follows:

1. Lower the front cover of the RFL 9300.
2. Place the POWER switch on the power supply module in the OFF position.
3. Lower the red lever at the front of the module until the module connector disengages with the motherboard connector.
4. Slide the module out of the chassis.

To replace a circuit board module, proceed as follows:

1. Using the label along the front of the chassis as a guide, determine the slot in the chassis where the module is to be installed.
2. Line up the edges of the module circuit board with the card guides in the chassis.
3. Place the red lever in the full up position.
4. Slide the module into the chassis and press firmly until its connector is fully engaged with the motherboard connector.
5. Place the POWER switch on the power supply module in the ON position.

WARNING

TO REDUCE THE POSSIBILITY OF ELECTRICAL SHOCK, ALL CURRENT TRANSFORMERS (CT'S) SHOULD BE SHORTED BEFORE ATTEMPTING TO REMOVE OR REPLACE ANY RFL 9300 I/O MODULES.

CAUTION

Each I/O module position in the rear of the RFL 9300 is dedicated to a specific I/O module type, though the module positions are not keyed. A label along the rear of the chassis specifies which I/O module goes in each position. I/O modules can be damaged if they are installed in the wrong chassis slot. When removing and replacing I/O modules, use the label in the chassis as a guide to make sure each I/O module is in the proper slot.

28.3.2 I/O MODULES

RFL 9300 I/O modules are mounted at the rear of the RFL 9300. Each I/O module is held in place by captive screws at the top and bottom of the I/O module. All I/O modules are grounded to a grounding bar that extends across the rear of the RFL 9300.

An I/O module removal tool is provided with each RFL 9300 to simplify removal and replacement of the I/O modules. The tool is stored in a clip on the protective cover that extends across the rear of the RFL 9300.

To use the I/O module removal tool to remove and replace an I/O module, proceed as follows:

1. Using a make-before-break switch, place a short across each CT, and open each CT circuit that is feeding the RFL 9300.

2. Using a Phillips screwdriver, loosen the two screws holding the protective cover in place across the rear of the RFL 9300, and slide the protective cover up and out of position.

3. Disconnect all wiring from the I/O module to be removed.
   Tag all wires before removal. This will simplify rewiring once the I/O module is replaced.

4. Using a flat-blade screwdriver, remove the screws that secure the grounding bar to each I/O module, and lift the grounding bar out of position.

5. Pull the I/O module removal tool out of its storage clip on the protective cover.

6. Insert the threaded end of the I/O module removal tool into the threaded hole on the I/O module to be removed, and turn the tool clockwise until it is tight.
   The RFL 93B RELAY I/O module has a threaded hole near the center of the panel. If you are replacing one of the other I/O modules, insert the removal tool into the threaded stand-doff for the grounding bar located at the top rear of the module.

7. Using a flat-blade screwdriver, loosen the captive screws holding the I/O module in place.

8. Using the I/O module removal tool as a handle, pull the I/O module out of the chassis.

9. Disconnect the I/O module removal tool from the I/O module by turning the tool counterclockwise until it is loose.

To replace an I/O module, proceed as follows:

1. Push the I/O module into the chassis until its edge connector engages its mating connector on the chassis motherboard.

2. Using a flat-blade screwdriver, tighten the captive screws to secure the I/O module in place.

3. Place the I/O module removal tool into its storage clip, and push the tool in until it its firmly seated.

4. Place the grounding bar in position across the rear of the RFL 9300. Using a flat-blade screwdriver, install and tighten the screws that secure the grounding bar to each I/O module.

5. Reconnect all wiring to the I/O module.
   Use the tags placed on the wires during removal as a reference.

6. Place the protective cover in position across the rear of the RFL 9300, and tighten the two screws that hold it in place.

7. Remove the shorts that were placed across each CT that is feeding the RFL 9300.

28.3.3 POWER SUPPLY MODULE

To remove a power supply module, proceed as follows:

1. Place the POWER switch on the power supply in the OFF position.

2. Lift the black locking lever to disengage the power supply from the internal heat sink.

3. Remove the power supply from the chassis by pulling on the ring at the top of the supply until the power supply connector disengages from the motherboard connector.

4. Slide the power supply module out of the chassis.

28.4 FUSE REPLACEMENT

The fuse for the 9300 power supply is located on the power supply module front panel. To check the fuse, proceed as follows:

1. Place the POWER switch on the power supply in the OFF position.

2. Remove the input fuse from the front panel using a flat-blade screwdriver and turning counter-clockwise until the cap is unscrewed. The fuse is pressed into the cap.

3. Remove the fuse from the fuse cap and inspect the fuse for damage.
   If a fuse is bad, it must be replaced. If the fuse is good, check for presence of input voltage at TB1-1 and TB1-2 on the RFL 93B RELAY I/O module. If voltage is present and the power supply does not function, the power supply module is defective and must be replaced.

4. Insert a fuse with the proper voltage and current ratings into the fuse cap and screw it into the fuse holder until it is firmly seated. Do not over tighten.
   For continued safe operation, always replace a fuse with one having the same voltage and current ratings. Refer to Table 28-1 for the proper fuse value.

Table 28-1. Fuse replacement data, RFL 9300 power supply module

Model	Assy. No.	Fuse Rating	Manufacturer's Type	Part Number
93 48/125 DC	106715-1	4A, 250V, SLO-BLO, 5x20mm	Littlefuse 218004 or equiv.	301122

5. Once the fuse has been checked or replaced, place the power switch in the ON position.
If all three green LED indicators on the power supply front panel light, the power supply is working properly. If all three indicators do not light or if the fuse blows again, the power supply is defective and should be replaced.

28.5 CORRECTIVE MAINTENANCE

The RFL 9300 Charge Comparison System has been designed for years of trouble-free service. Should a malfunction occur involving the RFL 9300, use standard troubleshooting techniques to determine if the problem is in the RFL 9300 or in some other connected equipment. If the problem lies within the RFL 9300, use the schematics in Sections 9 through 25 of this manual to determine which module is defective. Once this is done, replace the module. This should solve the problem.

Defective modules can be repaired locally, or they can be returned to RFL for repair as described below.

28.6 HOW TO ARRANGE FOR SERVICING

If necessary, RFL 9300 modules and subassemblies may be returned to RFL Electronics Inc. for repair. Contact our Customer Service Department using the telephone number at the bottom of this page. You will be given an authorization number and shipping instructions.

28.7 INSTRUCTIONS FOR CONVERTING A 3-TERMINAL 9300 TO A 2-TERMINAL 9300

While performing the required field upgrade please observe the following recommendations:

- *The RFL 9300's trip outputs should be isolated from the breaker coils to insure against accidental False Trips.*
- *Record all programmable parameters prior to turning off the RFL 9300 and performing upgrades. After the upgrades are completed, confirm that the programmable parameters did not change.*
- *Follow ESD procedures to insure against damage to modules while handling, during upgrades.*
- *Perform any standard testing required by your company prior to placing the RFL 9300 back into servce.*
- *After testing is completed, cycle power to all RFL 9300s off and on immediately prior to reconnecting trip outputs to the breaker coils. This will clear any trips that may have remained as a result of testing*.

1. Review Section 6, Familiarization. Table 6-3 indicates the RFL 9300 modules that must be installed. Notes 1 and 2 at the bottom of the table should be considered when converting from 3T to 2T.

2. Power down the relay.

3. Place the shorting jumper (J2) of the Supervisor Controller in position C.

Refer to Section 10, Supervisor Controller Module, of the RFL 9300 manual. Figure 10-2 indicates the jumpers and their respective positions. J2 is in the bottom position and has two settings, C and D. Setting C is for 2-Terminal (2T), and setting C is for 3-Terminal (3T).

4. As viewed from the front of the RFL 9300:

    - Remove the 93B Communications Controller module from the fourth slot from the left. (Position 4 of Figure 6-3 of the manual).
    - Remove the Transceiver module* (93 FT/FR module for fiber optic and 93 MO for modem. There are no modules in the front of the Direct Digital 9300.) from the second slot from the left. (See position 2 in Figure 6-3 of the manual.)
    - Store removed modules in static protective bags.
    - If the chassis has individual front panels attached to the removed modules, blank panels will have to be installed in the front of the chassis. (Qty 1 of RFL PN: 103970 and Qty 1 of RFL PN: 103975)
    - If the chassis has a swing down front door design, blank panels are not required.

5. As viewed from the rear of the RFL 9300:

   - Remove the ground bar from across the top of the chassis.
   - Remove the communications I/O module* located in the second slot from the right. (Position 18 in Figure 6-3 of the manual.)
   - Install a blank panel over the open slot. (RFL PN: 103982)
   - Reinstall the ground bar across the top of the chassis.

* For 2-terminal RFL 9300s with redundant communications, leave this module in place.

SECTION 29: MODEM APPLICATION INFORMATION

29.1 INTRODUCTION

The RFL 93B MO Modem Module and RFL 93 LC Line Coupler I/O Module form an analog, voice-grade, four-wire link to a remote RFL 9300. The RFL 93B MO operates over various grades of voice channels. The line could be as good as a back-to-back connection, or a Type 3002-conditioned line which is typical for voice-grade telephone channels. The RFL 93B MO modem module will "learn" the condition of the line when a training sequence is received from the remote terminal. The training signals are controlled by the RFL 93B CC Communications Controller Module (Section 13). The RFL 93B MO operates with the CCITT V.29 modulation standard at a 7.2-Kbps data rate. (See Section 14 of this manual for more information about these modules.)

29.2 TRANSMITTER LEVELS AND WIRING

The RFL 93B MO's transmitter output appears across terminals TB11-1 and TB11-2 on the RFL 93 LC Line Coupler I/O Module. The nominal output signal level is -3 dBm to +1 dBm, terminated into 600 ohms. The cable running from the RFL 93 LC module to the communication equipment must be a shielded twisted pair. The shield must be grounded at both the RFL 9300 and the communication equipment. The wires in the cable should be 24AWG or larger. Grounding is accomplished at the RFL 9300 by using the ground bus running along the top of the rear panel. An independent ground bus must also be connected between the communication equipment and the RFL 9300 to prevent large currents in the shield from melting the cable and disrupting communications. Protection is provided for signals fed back into the transmitter input; voltages in excess of 5 Vrms are clamped.

29.3 RECEIVER LEVELS AND WIRING

The RFL 93B MO's receiver input is accepted across terminals TB11-3 and TB11-4 on the RFL 93 LC Line Coupler I/O Module. The receiver's input impedance is 600 ohms, which will match most telephone circuits. The cable connecting the RFL 93 LC and the communication equipment must be a shielded twisted pair, grounded at both ends. The wires in the cable should be 24AWG or larger. The receiver has an AGC circuit that allows input signals from 0 dBm to -39 dBm to be accepted. It is recommended that the input level be set at about -16 dBm, which is the standard level for telephone circuits. Input protection is provided and signals over 5 Vrms are clamped before going into the modem circuits.

The AGC will accommodate a wide range of signal levels. However, noise is introduced by the modem's input amplifier at lower input signals. This could increase the S/N ratio to a point where modem performance is affected.

29.4 S/N RATIO VS DEPENDABILITY

The RFL 93B MO acts as an interface between the analog signals received over a voice channel and the digital signals accepted by the RFL 93B CC Communications Controller Module. The quality of the analog input is expressed as a signal-to-noise ratio (S/N), and the quality of a digital signal is expressed as a bit error rate (BER). The relation between S/N and BER depends on the conditioning of the line, the incoming signal level, and the definition of bandwidths. The RFL 93B CC monitors the validity of received digital messages by testing an attached security code that comes in with each data word. It will stop accepting digital signals if too many messages are corrupted over a period of time. For a Type 3002 line, a S/N ratio of +14 dB in will yield 100-percent dependability if the noise is pulsed for the same duration as a fault (60 ms maximum). If the noise on the line produces a continuous S/N of +16 dB, the RFL 93B CC module will squelch. The BER OK indicator module will turn off if the S/N is +19.5 dB. The dependability test results are shown in Figure 28-1.

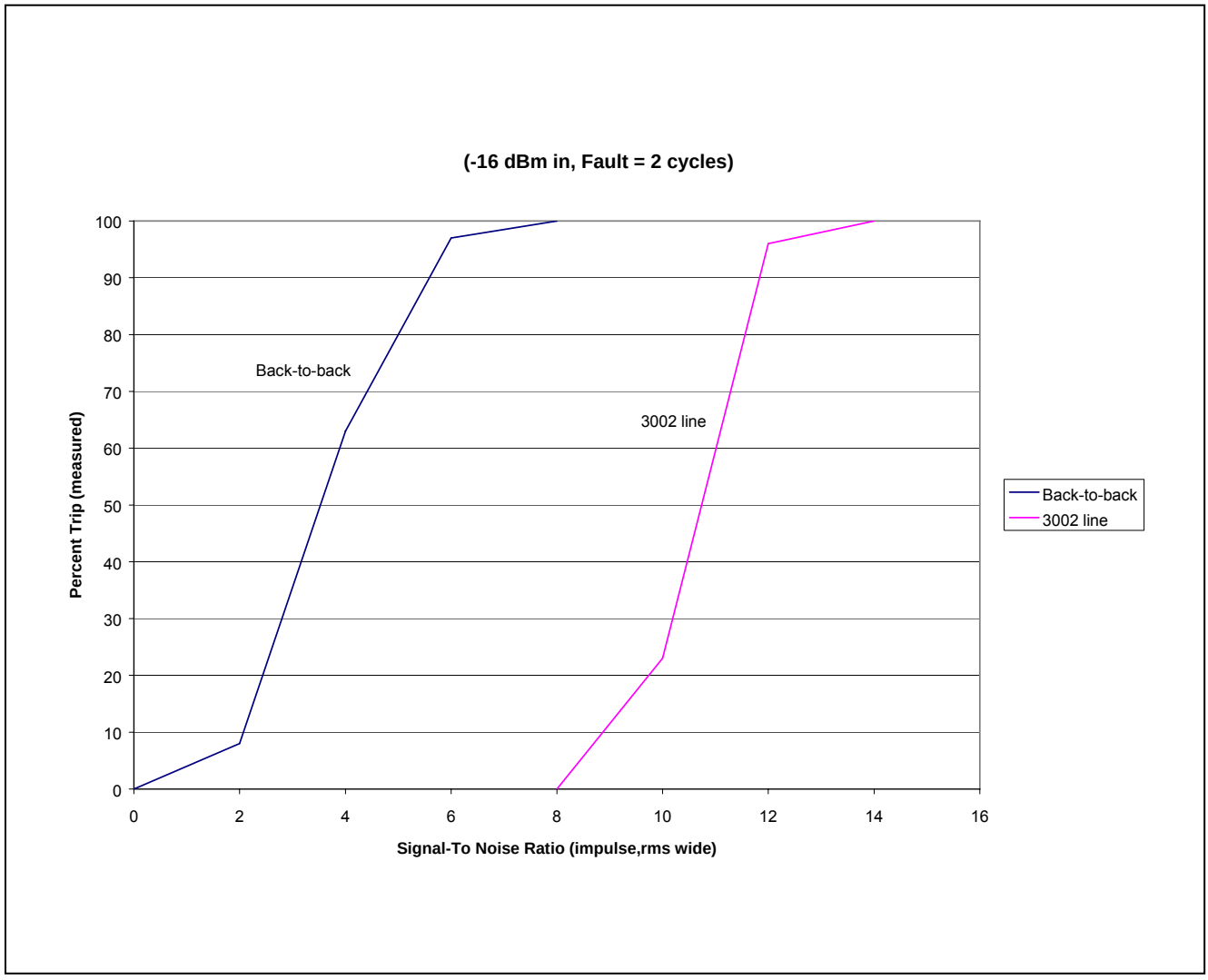


Figure 29-1. RFL 9300 modem dependability versus S/N ratio (measured)

29.5 TELEPHONE SERVICE REQUIREMENTS

The recommended four-wire leased telephone voice-grade service for communications with the RFL 93B MO is an "SPO-A" (Service Performance Objective Class A), as mentioned in IEEE Standard 487-1980, "Guide for the Protection of Wire-Line Communication Facilities Serving Electric Power Stations". The SPO-A line must provide reliable service before, **during**, and after a fault.

Appendix A is an example of a questionnaire form used by a telephone company which will give a feeling for the relevant information required to provide SPO-A service. The RFL 93B MO modem module does not require a dc connection to the remote terminal. The voice channel (300 Hz to 3300 Hz) is adequate.

29.6 MICROWAVE, RADIO, AND T1 ANALOG CHANNELS

If microwave, radio, or T1 communication is used, all equipment must be close together and on the same ground mat. The connection between the radio and the RFL 9300 relay must be shielded twisted pairs, with the shields grounded at both ends. There must be an independent solid ground bus connecting the chassis grounds of both the RFL 9300 and the radio.

The communications system is responsible for maintaining continuity though a fault. If the S/N drops below +15 dB during a fault, the RFL 9300 will not be dependable.

29.7 CHANNEL ROUTING VS DEPENDABILITY

Higher dependability can be obtained if the transmit and receive lines are routed differently. If communications in one direction is down, one terminal will trip during an internal fault. The second terminal will trip sequentially if the "Loss-Of-Load" feature is enabled. If both lines go down because of a common-mode failure, the relay can only function on overcurrent.

29.8 MODEM SECURITY

The RFL 93B CC module is programmed with the squelch rules that govern whether messages will be accepted. With the exception of a DTT input, incoming messages can not cause a trip unless the RFL 9300 locally detects a fault or system disturbance. Fault detector supervision prevents false trips due to random noise. The fault itself could cause common-mode noise; the squelch rules in the RFL 93B CC module filter and guard against accepting false messages in an impulse noise environment. Figures 28-2 and 28-3 contain the graphs for theoretical security.

29.9 SQUELCH RULES

The RFL 93B CC's microcontroller counts the number of good and bad words. It uses this information to decide if the channel is good or bad. The word segments are binary, and the errors that are counted yield a bit error rate (BER) which is a measure of communication quality. The noise on a channel may be long-term average noise, or the noise may come in pulses for a short duration.

The quality of the analog signal received by the modem is expressed as a signal-to-noise (S/N) ratio. If the line coming into the modem is 3002 conditioned, the spectrum is not flat and equalization is required. The link between S/N and BER (Bit Error Rate) changes slightly with added equalization (2 dB). If the S/N is better than 16 dB, the dependability of the relay is 100 percent with a 3002 conditioned line.

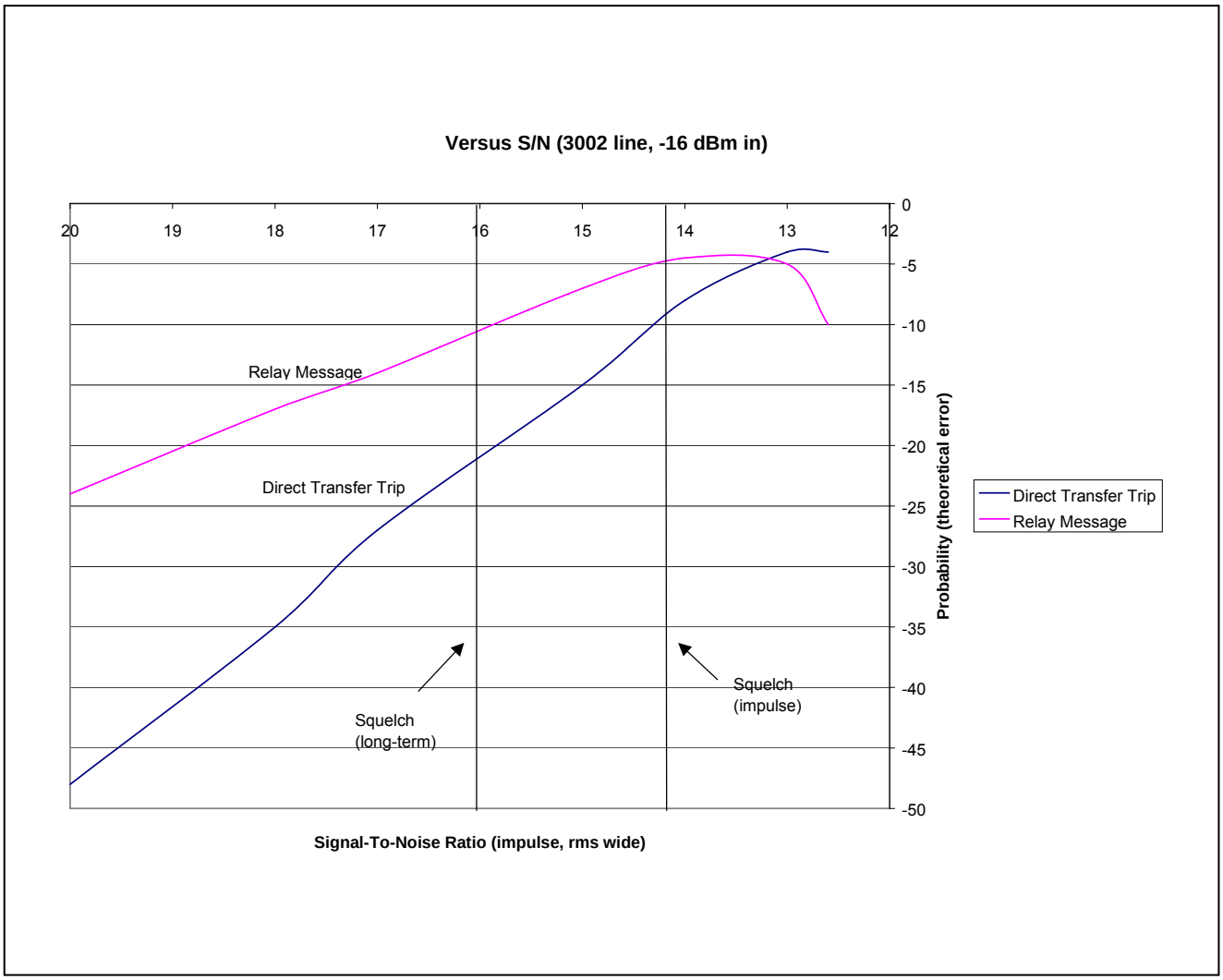


Figure 29-2. RFL 9300 probability of passing false words (theoretical)

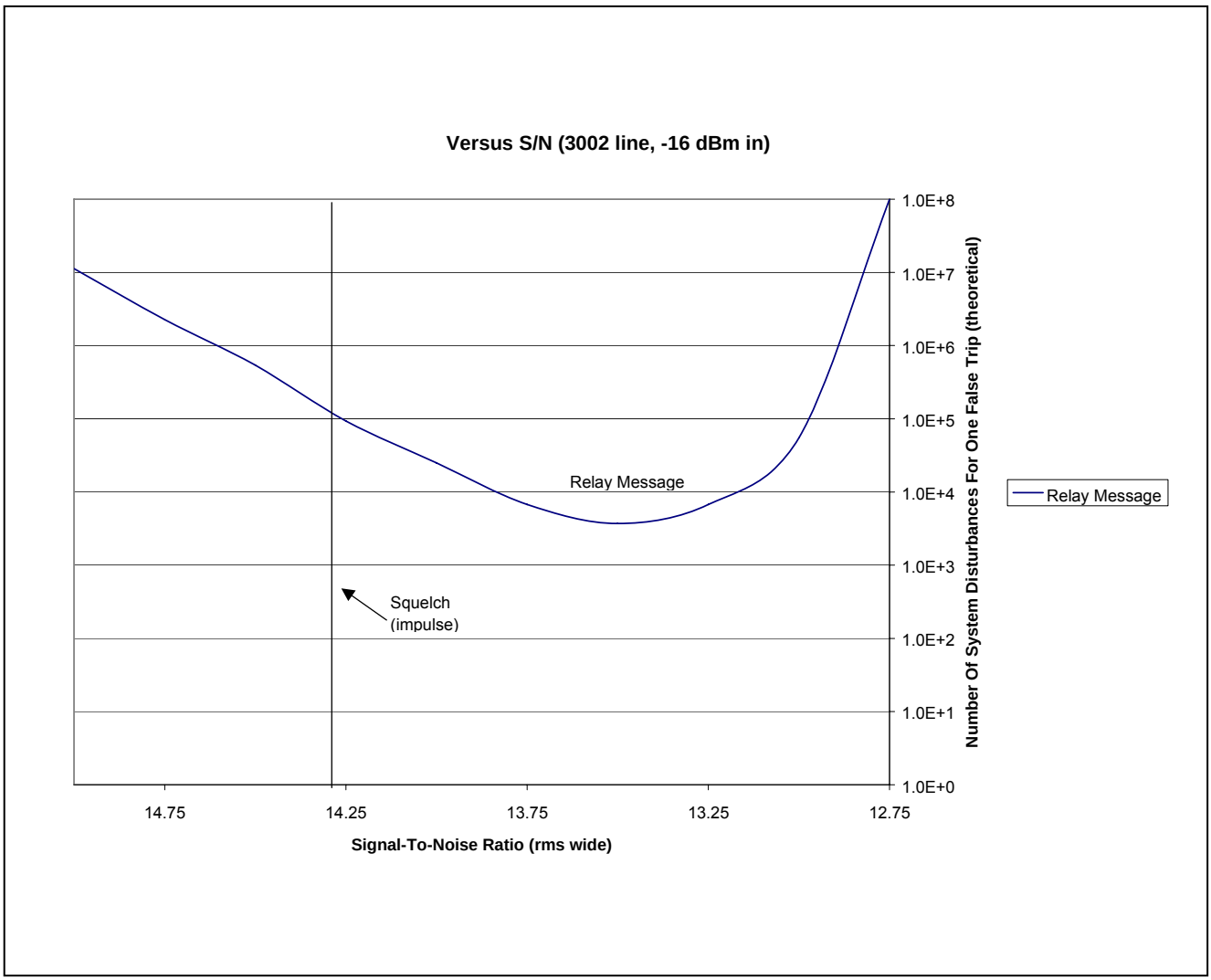


Figure 29-3. RFL 9300 modem security (theoretical)

The RFL 93B CC uses three squelch rules to determine whether communication quality is below that required by the RFL 9300. They are identified as Squelch Rule 1, Squelch Rule 2, and Squelch Rule 3 (SQ1, SQ2, and SQ3):

SQ3 Under Squelch Rule 3 (SQ3), the RFL 93B CC module will squelch the channel if the long-term noise produces a BER of -3 or worse. This represents one bad bit in one thousand bits, and is equivalent to an S/N ratio of about 16 dB. When SQ3 is on, the RFL 93B CC module alarms the RFL 93B SV module and blocks all communication messages from going to the RFL 93B SV module.

To come out of SQ3, 3 the BER must be better than -4 (one bad bit in ten thousand). This is equivalent to an S/N ratio of about 18 dB. It takes over 4 seconds to measure the 2000 word segments used to calculate SQ3; a fast exit from SQ3 occurs if 1000 error-free word segments in a row are received within 2 seconds. A fast exit can also occur if the EQM (Eye Quality Monitor) indicates that the S/N is better than 18 dB. The EQM value could return to normal in less than 100 ms if the average noise is not too great.

To enter SQ3, 30 bad word segments out of a total of 2000 word segments were measured. If 30 bad word segments are received in a row, SQ3 is entered without waiting for the full 2000 word segments. After the RFL 93B CC has entered SQ3, less than 3 bad segments out of 2000 segments are required to drop SQ3.

SQ2 SQ2 relates to short error pulses. It is the trigger that frames the local receiver hardware, and sends retrain request messages to the remote terminal. SQ2 will also alarm the RFL 93B SV module and block messages from being sent to the rest of the terminal. If eight bad words are received out of a total of 25, the RFL 93B CC enters SQ2. It takes ten good words in a row to exit SQ2.

If SQ2 is on for 100 ms and the EQM value indicates that the channel is good, the hardware receiver is initialized or framed. If the channel is bad for over 500 ms and SQ2 is on, a request is sent to the remote terminal and the remote terminal sends a training sequence. After the training sequence has been received, the hardware receiver is initialized for framing. For short noise bursts (less than 50 ms), the QAM reference vector is not lost and the channel recovers within 10 words after the noise turns off.

SQ1 SQ1 blocks messages from going to the RFL 93B SV module, but does not alarm the module. SQ1 is entered if two bad words in a row are received, and turned off if three good words in a row are received.

29.10 CHANNEL DELAY LIMITS

The maximum total delay that the supervisor module will accept is 25 ms. There are several delays other than the channel delay which must be accounted for in this 25-ms interval. The modem has a through delay of about 9 ms which changes slightly each time the modem module is trained. There are several messages in the shift queue, and there are interboard delays within the RFL 9300 itself.

Adding up all delays other than the channel delay equals about 19 ms, which leaves about 6 ms for channel delay. A reasonable upper limit on the channel delay would be 5 ms. The ping-pong delay displayed on the front panel is the total delay, and should be 24 ms or less.

29.11 TEST POINTS

The following test turrets on the RFL 93B MO modem module can only be accessed when the module is on a card extender.

TP1 RX IN - analog signal; should be -17 dBm nominal when J1 is in Position A.

TP2 Should be between +11.4 and +12.6 volts.

TP3 Should be between -11.4 and -12.6 volts.

TP4 RX CLOCK - digital signal; should vary between zero and 5 volts at a 7.2-kHz rate.

TP5 RX DATA - digital signal for recovered data; should vary between zero and 5 volts.

TP6 TX DATA - digital signal for outgoing data received from RFL 93B CC module. This should vary between zero and 5 volts.

TP7 TX CLOCK - digital signal; should vary between zero and 5 volts at a 7.2-kHz rate.

TP8 TX OUT - analog signal; should be –0 dBm nominal.

This page intentionally left blank

SECTION 30: GLOSSARY OF TERMS

ACT	Auxiliary Current Transformer	A small flux-cancellation toroid that transforms the main current transformer secondary current to an AC millivolt signal that is an exact replica of the secondary current. The 9300 contains four ACT's, one for each phase and one for $3I_0$ (ground).
A/D	Analog to digital	Analog to digital
ADD1	Address 1	Address 1
ADD2	Address 2	Address 2
AGC	Automatic Gain Control	Automatic Gain Control
Amp	Amp	Abbreviation for Ampere, a unit of electrical current.
APRIL	APRIL	Asynchronous Programming and Remote Interrogation Language.
Arms	Arms	Ampere(s) root mean square
AS	Arithmetic Sum	The absolute value of the sum of the local charge and remote charge (actually RMS current equivalent to charge), taking polarity into account.

Examples	Local Charge	Remote Charge	Arithmetic Sum
Ex. 1	-6A	+4A	2A
Ex. 2	-4A	+6A	2A
Ex. 3	+4A	+6A	10A

The arithmetic sum is equivalent to the "operate current" in a conventional current differential relay.

AUTO	Automatic	Automatic
AUX	Auxiliary	Auxiliary
AWG	American wire gauge	A standard measuring gauge for non-ferrous conductors. Gauge is a measure of the diameter of the conductor.
BC-G	BC-G fault	A fault where phase B and phase C are shorted to ground.
BER	Bit Error Rate	The number of received communication bits that are in error for a large number of received bits. For example, if the BER is given as 10^{-4} this means that on average, one bit is in error for every ten-thousand received bits.
BL	Blocking level	Blocking level
BNC	BNC	A bayonet-locking connector for coaxial cables.
bps	Bits per second	Bits per second

CC	Communications Controller	This is a front panel module on the 9300 that performs the logic and signal processing related to the relay-to-relay communications.
CCD	Charge Comparison Data	Charge Comparison Data
CCDWFD		Charge Comparison Data With Fault Detector
CCITT	CCITT	Consultative Committee on International Telegraphy and Telephony. The CCITT is one of four permanent parts of the International Telecommunications Union (ITU) based in Geneva Switzerland.
CCITT X.21		A CCITT standard for interfacing between data terminal equipment (DTE) and data circuit equipment (DCE) for synchronous operation on public switched telephone networks.
CCITT V.29		A CCITT standard for 9600 bits per second modem for use on point-to-point leased circuits
CCS	Charge Comparison System	The name given to the 9300 relay.
CCT	Charge Comparison Trip	Charge Comparison Trip
CCTU	CCTU	Charge Comparison Trip Ultimate
CDC	Channel Delay Compensation	This is the number of milliseconds that the 9300 relay assigns to the received channel path. For example, if the CDC is 4-ms, this means that the local relay thinks that the received communications signal took 4 milliseconds to get from the remote relay to the local relay. Ideally the CDC should be exactly equal to the CDT (defined below), but the concept of charge comparison is very tolerant of imprecise compensation (i.e., where CDC is not exactly equal to CDT).
CDT	Channel Delay Time (Actual)	This is the actual delay experienced by the communications message transmitted by the remote relay and received by the local relay. (See the previous discussion of CDC).
CRC	Cyclic Redundancy Check	Cyclic Redundancy Check
CT	Current Transformer	Current Transformer
DC	Display Controller	This is a front panel module on the 9300 that displays messages on the LED readout and has a key pad to enable an operator to enter commands. It also has LED's to indicate trips and DTT send and receive conditions.
DCE	DCE	Digital Communication Equipment
DD	Direct Digital	Direct Digital
DLG	Double Line to Ground	Double Line to Ground
DML	DML	Delay Measurement based on Load current
DTE	Data Terminal Equipment	Data Terminal Equipment

DTT	Direct Transfer Trip	This is a trip command initiated by an external contact closure, such as a breaker failure, and sent to the remote end. The received trip signal is not supervised by a local relay function, so this trip is called “direct”. DTT has nothing to do with the line protection (i.e., the charge comparison). It is totally separate.
EIA	EIA	Electronic Industries Association. A Washington D.C. trade organization of manufacturers which sets standards for use by its member companies.
EMTP	EMTP	Electromagnetic Transients Program
EN/DIS		Enable/Disable
ENT	ENT	Abbreviation of the “enter” key on a computer keyboard
EPROM		Erasable Programmable Read Only Memory. A read only memory device which can be erased and reprogrammed.
EQM	Eye Quality Monitor	Eye Quality Monitor
FD	Fault Detector	This function provides security by supervising the charge comparison tripping. It responds to any sudden changes in the power system such as load switching or faults.
F1	Fault 1	Fault 1
F2	Fault 2	Fault 2
IEC	IEC	International Electrotechnical Committee. An international technical standards organization.
IEEE	IEEE	Institute of Electrical and Electronics Engineers. A publishing and standards making organization responsible for telecom and computing standards.
IL	Current, Local	This is the current in secondary amperes AC produced by the local current transformer(s).
IR	Current, Remote	This is the current in secondary amperes AC produced by the remote current transformer(s).
IRIG	IRIG	Inter Range Instrumentation Group (IRIG) for standard instrumentation timing formats. In the IRIG family, individual time code formats are alphabetically designated A, B, D, E, G and H.
IRIG-B		IRIG standard code format B.
Kbps	Kilobytes per second	Kilobytes per second
L	Local Terminal	Local terminal.
LCCT	LCCT	Local Charge Comparison Trip
LED	Light Emitting Diode	Light Emitting Diode

OC/SLG		Open Conductor with one single line to ground
OC/2-SLG		Open Conductor with two single lines to ground
OVHD	Overhead	Overhead
PC	Phase Controller	This is a front panel module on the 9300 that contains the main logic of the charge comparison system. There is one PC for each phase (A, B, C) and one for $3I_0$ (ground).
PLD	Programmable Logic Device	Programmable Logic Device
PPI	Ping Pong Initiate	This is a special message that is transmitted once per second. PPI tells the receiving terminal to send back another message called PPR defined below. The PPI and PPR messages enable a round trip or “loop back” measurement of the channel delay time. This measurement is called “Ping-Pong” a term taken from the modem industry.
PPR	Ping Pong Response	PPR is a signal triggered by a received PPI. See the preceding definition of PPI.
QAM	QAM	Quadriture Amplitude Modulation
R	Remote Terminal	Remote Terminal.
RD	Read	Read
RMS	Root mean square	Root mean square
RX	Receiver	The 9300 receiver.
SFT	Strong Feed Trip	Strong Feed Trip
SIF	Switch Into Fault	Switch Into Fault
SIF W/O C		Switch Into Fault Without Communication
SLG	Single Line to Ground	Single Line to Ground
S/N	Signal to Noise Ratio	Signal to Noise Ratio
SPOA	SPOA	Service Performance Objective Class A
SQ1	Squelch Rule 1	Squelch Rule 1
SQ2	Squelch Rule 2	Squelch Rule 2
SQ3	Squelch Rule 3	Squelch Rule 3

SS	Scalar Sum	The sum of the absolute values of the local charge and the remote charge (actually RMS current equivalent to charge).

Examples	Local Charge	Remote Charge	Scalar Sum
Ex. 1	-6A	+4A	10A
Ex. 2	-4A	+6A	10A
Ex. 3	+4A	+6A	10A

The Scalar Sum is equivalent to the “restraint current” in a conventional current differential relay. The arithmetic sum defined earlier and the scalar sum taken together determine whether or not the RFL 9300 Relay Charge Comparison algorithm decides to trip.

SV	Supervisor Controller	This is a front panel module on the 9300 which controls the routing of messages between all other modules of the 9300. It also contains 9300 system logic.
SWID	Software Identification	The SWID is a software identification number which indicates the revision of the software in the 9300. There are up to eight SWID numbers for each 9300 as follows: 1 for each Communications Controller, 1 for the Supervisor Controller, 4 for the Phase Controllers, and 1 for the Display Controller. See paragraph 6.1 for more information.
TOC	Time Overcurrent	Time Overcurrent
TX	Transmitter	The 9300 transmitter.
TX/RX	Transmit/Receive	Transmit/Receive
UGD	Underground	Underground
UHS	Ultra-High Speed	The UHS is an algorithm which works in parallel with the charge comparison algorithm and weak feed trip algorithm defined below. The UHS operates whenever there is moderate or high current, above +12A peak for 2-ms or more. A message is sent to the remote terminal to command a trip unless there is high negative current. For high current faults, the UHS provides faster tripping than the charge comparison.
UHST	Ultra High Speed Trip	Ultra High Speed Trip
WCM	Weak Current Message	Weak Current Message
WFT	Weak Feed Trip	The WFT is an algorithm which supplements the charge comparison for internal faults where one terminal contributes very little or no fault current. There is not a significant half-cycle charge measured at the weak terminal for this condition. WFT works by detecting a low magnitude current at the local terminal, coincident with moderate or high current at the remote terminal.
WR	Write	Write

ZCM	Zero Current Message	This is a special message that is transmitted whenever the local breaker is open. If the remote terminal receives a ZCM and at the same time measures a moderate or large current at its own terminal, this indicates an internal fault.
ZL	Load impedance	Load impedance
ZS	Source Impedance	Source Impedance
ZTC	Zero True Current Signal	Zero True Current Signal

Section 31. INDEX

A

Acceptance tests, laboratory, 7-1
Accessing the RFL 9300 from a PC or terminal, 6-30
ACT I/O module
  component locator drawing, 11-6
  controls and indicators, 11-1
  description, 11-1
  hardware description, 2-10
  parts list, 11-4
  schematic, 11-7
  theory of operation, 11-2
Active channel selection, 4-12
Address code selection
  display controller, 9-4
Address decoding
  communications controller module, 13-9
  display controller, 9-4
Addressing, 6-54
Alarm I/O module
  component locator drawing, 21-5, 21-10
  controls and indicators, 21-1
  description, 21-1
  parts list, 21-4, 21-9
  schematic, 21-7, 21-11
  theory of operation, 21-2
Alarms
  clearing, 6-16
  codes, 6-15, 28-1
  delay, communications, 4-10
  display, viewing, 6-34
Application information
  modem, 29-1
  RFL 9300, 3-1
APRIL commands, 6-33
Auxiliary current transformer module, 11-1

B

Back-up, 2-21
  functions, system, 4-7
  ground overcurrent, 4-8
  phase overcurrent, 4-8
Backup tripping, 8-15
Baud rate selection, RS-232, 4-12
Beeper control, 4-11
Bias
  control, 4-5
  ground, 4-5
  phase, 4-1
Block diagrams
  fiber optic I/O modules, 18-6, 18-8, 18-10
  fiber optic transceiver module, 17-7
  power supply modules, 19-4
  RFL 9300, 2-2, 2-3

C

Cable, overhead or underground, 3-16, 4-9
Calculations for low-side faults, 3-22
Changing the password, 6-51
Channel impairment characteristics
  direct digital or fiber optic, 2-5
  single-channel modem, 2-7
Channel selection, active, 4-12
Characteristics, channel impairment
  direct digital or fiber optic, 2-5
  single-channel modem, 2-7
Chassis
  description, 24-1, 25-1
  dimensions, 1-10
  expansion chassis, 26-1
Chip enables, display controller, 9-3
Clearing an alarm, 6-16
Codes, alarm, 6-15, 28-1
Commands, APRIL, 6-33
Commissioning, field, 8-1
Commissioning, final, 8-35
Communication information, 6-30
Communications
  alarm delay, 4-10
  end-to-end, verification of, 8-16
  information, 6-30
  management, interboard, 10-3
  mode, 4-11
  phone line, 5-9
Communications controller module
  address decoder, 13-9
  controls and indicators, 13-1
  description, 13-1
  hardware description, 2-4
  hot standby two-channel modem operation, 13-5
  parts list, 13-11
  read and write circuits for RFL 93 MO, 13-9
  read and write circuits for RFL 93 SV, 13-9
  receiver circuit, 13-6
  receiver timing diagram, 13-8
  single-channel digital or fiber optic operation, 13-5
  single-channel modem operation, 13-5
  theory of operation, 13-3
  transmitter circuit, 13-6
  transmitter timing diagram, 13-7
  watchdog reset function, 13-6
Communications verification
  direct digital, 8-17
  fiber optic, 8-18
  modem, 8-16
Compensated lines, series, 3-1
Component locator drawings
  ACT I/O module, 11-6
  alarm I/O module, 21-5
  communications controller module, 13-13
  direct digital interface I/O module, 16-5
  display controller, 9-11
  display module front panel, 9-26
  display module, oscillography board, 9-19
  expansion chassis power supply, 26-2
  fiber optic I/O modules, singlewidth, 18-14, 18-19, 18-25
  fiber optic transceiver module, 17-3
  line coupler I/O module, 15-3
  modem module, 14-8
  motherboard, 25-2
  phase controller modules, 12-7
  power supply modules, 19-8
  relay I/O module, 20-7, 20-9, 20-11
  short haul fiber interface module, 22-6
  supervisor controller, 10-10
Conductor, open, 4-9
Configuration information, viewing, 6-39

Connections
direct digital, 5-10
electrical, 5-4
fiber optic, 5-10
fiber service unit, 22-14
I/O, modem, 5-9
IRIG-B clock, 5-10
modem, 5-9
Control
beeper, 4-11
bias, 4-5
display intensity, 4-11
modem output level, 5-9
Controller, supervisor
hardware description, 2-8
Controls and indicators
ACT I/O module, 11-1
alarm I/O module, 21-1
communications controller module, 13-1
direct digital interface I/O module, 16-1
display controller, 9-2, 9-5
fiber optic I/O modules, singlewidth, 18-3
fiber optic transceiver module, singlewidth, 17-4
fiber service unit, 22-10
line coupler I/O module, 15-1
modem module, 14-1
phase controller modules, 12-1
power/RS-232 board, 20-3
relay I/O module, 20-1
RFL 9300 front panel, 6-1
short haul fiber interface module, 22-3
supervisor controller, 10-1
Corrective maintenance, 28-6
Current transformers, main, saturated, 3-11

D

Default, factory, resetting to, 4-10
Delay
communications alarm, 4-10
ground, 4-5
time, 4-6
Detectors, ground and phase fault, 4-7
Diagnostics, 2-25
Diagram, block, 2-2
Differences between models
fiber optic I/O modules, singlewidth, 18-2
power supply modules, 19-2
Differential current test, 8-26
Differential current test overview, 8-19
Direct digital communications, verification, 8-17
Direct digital interface I/O module
component locator drawing, 16-5
connections, 5-10
controls and indicators, 16-1
description, 16-1
parts list, 16-4
schematic, 16-7
theory of operation, 16-3
Display
alarms, viewing, 6-34
intensity control, 4-11
modes, 6-14
parameters, 6-16
values, viewing, 6-36
Display controller
component locator drawing, 9-11, 9-19
controls and indicators, 9-2
description, 9-1
front panel interfacing, 9-5
hardware description, 2-23
microcontroller, 9-4
microcontroller supervisor, 9-4
parts list, 9-9, 9-17
RS-232 communications, 9-4
RS-485 communications, 9-4
schematic, 9-13, 9-21
theory of operation, 9-4, 9-7
Display module, 9-1
display controller, 9-1
front panel, 9-1
theory of operation, 9-7
Displaying parameters, 6-16, 6-23

E

Electrical connections, 5-4
End-to-end communications, verification of, 8-16
Entering the PROGRAM mode, 6-25
Entering the READ mode, 6-16
Entering the STARTUP mode, 6-23
Equipment requirements
field commissioning, 8-1
laboratory acceptance tests, 7-1
Events log, sequence of, viewing, 6-45
Exiting the PROGRAM mode, 6-29
Exiting the READ mode, 6-23
Exiting the STARTUP mode, 6-25
Expansion chassis, 26-1

F

Factory default, resetting to, 4-10
Fault detector, ground, 4-7
Fault detector, phase, 4-7
Faults
ground, high-resistance, 3-5
internal fault calculation, 3-11
external fault calculation, 3-12
three-phase, reclose blocking for, 3-16
Fiber optic communications, verification, 8-18
Fiber optic connections, 5-10
Fiber optic I/O module, singlewidth
component locator drawings, 18-14, 18-19, 18-25
controls and indicators, 18-3
description, 18-2
differences between modules, 18-2
introduction, 18-1
parts lists, 18-12, 18-17, 18-23
schematics, 18-15, 18-21, 18-27
specifications, 18-2
theory of operation, 18-6
Fiber optic transceiver module, singlewidth
component locator drawing, 17-13
controls and indicators, 17-4
description, 17-2
introduction, 17-1
parts list, 17-11
schematic, 17-15
specifications,17-2
theory of operation, 17-6
Fiber service unit
controls and indicators, 22-10
description, 22-9
fiber optic cable connections, 22-14
mounting dimensions, 22-11
power connections, 22-12
RS-449 connections, 22-14
specifications, 22-10
Field commissioning, 8-1

Final commissioning, 8-35
Framing, direct digital or fiber optic, 2-6
Frequencies, sub-normal, 3-1
Front panel, display module, 9-8
  component locator drawing, 9-26
  interfacing with display controller, 9-5
  parts list, 9-25
  schematic, 9-27
Functions
  keypad, 6-4
  system backup, 4-7
Fuse replacement, 28-5

G

G.703 interface I/O, 23-1
  description, 23-1
  controls and indicators, 23-1
  theory of operation, 23-3
Glossary of terms, 30-1
Ground
  bias, 4-5
  delay, 4-5
  fault detector, 4-7
  fault, high-resistance, 3-5
  overcurrent backup, 4-8
Guidelines, setting, 4-1

H

High-resistance ground fault, 3-4
High-speed tripping, ultra, 3-9
Hot standby signal routing diagram, 17-9
Hot standby two-channel 56/64-Kbps operation, 2-5
Hot standby two-channel direct digital operation, 13-5
Hot standby two-channel modem operation, 2-5, 13-5
How to arrange for servicing, 28-6

I

I/O connections, modem, 5-9
Impairment characteristics, channel
  direct digital or fiber optic, 2-5
  single-channel modem, 2-7
In-rush, transformer, 3-23
Indicators and controls, 6-3
Information, communication, 6-30
Initialization, system, 2-1
Installation, 5-1
Intensity control, display, 4-11
Interboard communications management, 10-3
Internal faults, 8-10
Interface, G.703, 23-1
Inversion, voltage, 3-1

K

Keypad functions, 6-4

L

Laboratory acceptance tests
  alarm conditions and transmit address alarm, 7-3
  backup tripping with high-set overcurrent, 7-17
  demonstration of CDC derived from DML, 7-23
  demonstration of rainbow characteristic, 7-18
  direct transfer trip, 7-4
  equipment requirements, 7-1
  external A-G faults, 7-5
  internal A-B faults, 7-12
  internal A-G faults with outfeed, 7-22
  internal A-G faults, 7-9
  internal A-G faults with remote breaker open, 7-16
  internal three-phase faults, 7-13
  oscillography test, 7-28
  other external fault types, 7-6
  other internal fault types, 7-13
  other internal fault types with rmt bkr open, 7-17
  other weak-feed internal fault types, 7-15
  system setup, 7-1
  test procedures, 7-2
  weak-feed internal A-G faults, 7-14
Leaving the programming mode, 6-53
Level control, modem output, 5-9
Line coupler I/O module
  component locator drawing, 15-3
  controls and indicators, 15-1
  description, 15-1
  parts list, 15-2
  schematic, 15-4
  theory of operation, 15-2
Lines
  series compensated, 3-1
  very short, 3-3
Load, tapped, 3-20
Log, sequence of events, viewing, 6-45
Low-side faults, calculations for, 3-22

M

Main current transformers, saturated, 3-11
Maintenance, 28-1
Maintenance, corrective, 28-6
Management, interboard communications, 10-3
Microcontroller, display controller, 9-4
Microcontroller supervisor, display controller, 9-4
Microwave, modem application, 29-3
Modem application information, 29-1
  channel delay limits, 29-6
  channel routing vs dependability, 29-3
  microwave, radio, and T1 analog channels, 29-3
  receiver levels and wiring, 29-1
  S/N ratio vs dependability, 29-1
  security, 29-3
  squelch rules, 29-3
  telephone service requirements, 29-3
  test turrets, 29-6
  transmitter levels and wiring, 29-1
Modem communications, verification, 8-16
Modem module
  component locator drawing, 14-8
  connections, 5-9
  controls and indicators, 14-1
  description, 14-1
  hot standby two-channel operation, 2-5, 13-5
  output level control, 5-9
  parts list, 14-6
  schematic, 14-9
  single-channel operation, 2-4, 13-5
  theory of operation, 14-3
Modem security, 29-3
Mode, programming, leaving, 6-53
Modes
  communications, 4-11
  display, 6-14
  PROGRAM, 6-14
  programming, leaving, 6-53
  READ, 6-14, 6-16

STANDBY, 6-14, 6-15
STARTUP, 6-14
Module, display, 9-1
Motherboard
component locator drawing, 25-2
parts list, 25-1
schematic, 25-3
Mounting, 1-10, 5-2
Mounting dimensions
fiber service unit, 22-11
horizontal chassis, 5-3

N

New settings, saving, 6-53
Normal RFL 9300 operation, returning to, 6-54

O

Open conductor, 4-9
with single line-to-ground fault, 3-25
without single line-to-ground fault, 3-29
Operation
backup mode, 2-21
normal RFL 9300, returning to, 6-54
principles of, 1-1
stub-bus, 4-10
system, 2-1
Ordering information, 1-8
Oscillography board, display module
component locator drawing, 9-19
controls and indicators, 9-5
description, 9-5
parts list, 9-17
schematic, 9-21
theory of operation, 9-7
Output level control, modem, 5-9
Overcurrent backup
ground, 4-8
phase, 4-8
Overhead or underground cable, 4-9

P

Panel, front, display module, 9-8
Parameter
programming, 6-29
settings, reading, 6-37
Parameters, 6-18 to 6-22, 6-24, 6-26 to 6-28
displaying, 6-23
programmable, 4-1 to 4-13
remote, display, 6-40
Parts lists
ACT I/O module, 11-4
alarm I/O module, 21-4, 21-9
chassis, 24-1
communications controller module, 13-11
direct digital interface I/O module, 16-4
display controller board, 9-9
expansion chassis, 25-2
front panel assembly, display, 9-25
line coupler I/O module, 15-2
modem module, 14-6
motherboard, 25-1
phase controller module, 12-5
power supply module, 19-5
relay I/O module, 20-6, 20-8, 20-10
short haul fiber interface module, 22-5
singlewidth transceiver module, 17-11
single width I/O modules, 18-12, 18-17, 18-23
supervisor controller, 10-8
Password, changing the, 6-51
Personal computer
accessing the RFL 9300 from, 6-30
programming the RFL 9300 with, 6-50
Phase
bias, 4-1
fault detector, 4-7
overcurrent backup, 4-8
unbalance, 3-2
Phase controller module
component locator drawing, 12-7
controls and indicators, 12-1
description, 12-1
hardware description, 2-10
parts list, 12-5
schematic, 12-9
theory of operation, 12-3
Phase sequence test, 8-23
Phase sequence test overview, 8-19
Phone line communications, 5-9
Power/RS-232 board
controls and indicators, 20-3
theory of operation, 20-4
Power supply module
block diagram, 19-4
component locator drawings, 19-8
description, 19-1
differences between models, 19-2
schematic, 19-9
specifications, 19-1
theory of operation, 19-3
Principles of operation, 1-1
Procedure
laboratory acceptance test, 7-2
start-up, 6-1
PROGRAM mode, 6-25
Programming mode, leaving, 6-53
Programming the RFL 9300 with PC or terminal, 6-50
Programming, parameter, 6-29
Protection, stub-bus, 3-18
Protocol selection, RS-232, 4-13

R

RS-232 communications, display controller, 9-4
RS-485 communications, display controller, 9-4
Radio, modem application, 29-3
READ mode, 6-16
Read mode parameters, 6-16 to 6-22
Reading parameter settings, 6-37
Rear view, 1-11
Receiver circuit, communications controller module, 13-6
Reclose blocking for three-phase faults, 3-16
Relay output board
controls and indicators, 20-1
theory of operation, 20-5
Relay I/O module
component locator drawings, 20-7, 20-9, 20-11
controls and indicators, 20-1
description, 20-1
parts list, 20-6, 20-8, 20-10
schematic, 20-13, 20-15, 20-17
theory of operation, 20-4
Relay output board theory of operation, 20-5
Removal and replacement, circuit boards, 28-3
Remote parameters display, 6-40
Replacement, fuse, 28-5

Resetting to factory default, 4-10
Returning to normal RFL 9300 operation, 6-54
RS-232 baud rate selection, 4-12
RS-232 protocol selection, 4-13
Rules, squelch
direct digital or fiber optic, 2-6
single-channel modem, 2-7, 29-3

S

Saving new settings, 6-53
Schematics
ACT I/O module, 11-7
alarm I/O module, 21-7, 21-11
chassis, 25-3
communications controller, 13-5
direct digital interface I/O module, 16-7
display controller, 9-13
display module front panel, 9-27
display module oscillography board, 9-21
expansion chassis, 26-3
line coupler I/O module, 15-4
modem module, 14-9
motherboard, 25-3
phase controller modules, 12-9
power supply modules, 19-9
relay I/O module, 20-13
short haul fiber interface module, 22-7
singlewidth fiber optic I/O modules, 18-15, 18-21, 18-27
singlewidth fiber optic transceiver module, 17-15
supervisor controller, 10-11
Selection
active channel, 4-12
RS-232 baud rate, 4-12
RS-232 protocol, 4-13
Sequence of events log, viewing, 6-45
Serial communications link with display controller, 10-5
Series compensated lines, 3-1
Servicing, how to arrange for, 28-6
Setting guidelines, 4-1
Settings
new, saving, 6-53
parameter, reading, 6-37
Short haul fiber interface module
component locator drawing, 22-6
controls and indicators, 22-3
introduction, 22-1
parts list, 22-5
schematic, 22-7
specifications, 22-2
theory of operation, 22-4
Short lines, very, 3-3
Single-channel operation
56-Kbps or 64-Kbps digital or fiber optic, 2-5, 13-5
modem, 2-4, 13-5
Single pole chassis
controls and indicators, 24-1
description, 24-1
theory of operation, 24-6
Single-relay tests
alarm conditions, 8-8
backup tripping, high-set overcurrent, 8-15
direct transfer trip, 8-9
equipment requirements, 8-3
familiarization, 8-4
internal faults, 8-10
introduction, 8-2
procedures, 8-3
Software information, viewing, 6-1, 6-39
Specifications
fiber service unit, 22-10
power supply modules, 19-1
RFL 9300, 1-12
short haul fiber interface module, 22-2
singlewidth I/O modules, 18-2
singlewidth transceiver module, 17-2
Squelch rules
direct digital or fiber optic, 2-6
single-channel modem, 2-7, 29 -3
STANDBY mode, 6-15
Start-up procedures
two-terminal, 6-1
three-terminal, 6-10
Startup mode, 6-23, 8-20, 8-21
Startup mode parameters, 6-23, 6-24
Stub-bus
operation, 4-10
protection, 3-18
Sub-normal frequencies, 3-1
Supervisor controller
component locator drawing, 10-10
controls and indicators, 10-1
description, 10-1
hardware description, 2-8
jumpers, alarms, watchdog timer, and power supply supervisor, 10-6
other microcontroller I/O port signals, 10-6
output latch control, 10-5
parts list, 10-8
schematic, 10-11
serial communications with display controller, 10-5
system clock, 10-3
theory of operation, 10-3
System
backup functions, 4-7
clock, 10-3
initialization, 2-1
operation, 2-1
System operation, verification of, 8-16

T

T1 analog channels, modem application, 29-3
Tapped load, 3-20
Terminal
accessing the RFL 9300 from, 6-30
programming the RFL 9300 with, 6-27
Tests
field commissioning, 8-1
laboratory acceptance, 7-1
Theories of operation
ACT I/O module, 11-2
alarm I/O module, 21-2
communications controller module, 13-3
direct digital interface I/O module, 16-3
display controller, 9-4
display module oscillography board, 9-7
line coupler I/O module, 15-2
modem module, 14-3
oscillography board, 9-7
phase controller modules, 12-3
power supply modules, 19-3
power/RS-232 board, 20-4
relay I/O module, 20-4
relay I/O, current sense board, 20-7
relay output board, 20-7
short haul fiber interface module,22-4
singlewidth fiber optic I/O modules, 18-6

singlewidth fiber optic transceiver module, 17-6
supervisor controller, 10-3
Three-phase faults, reclose blocking for, 3-16
Time delay, 4-6
Transceiver module
block diagram, 17-7
component locator drawing, 17-13
controls and indicators, 17-4
description, 17-2
hot standby signal routing, 17-9
parts list, 17-11
schematic, 17-15
specifications, 17-2
Transformer in-rush, 3-23
Transmitter circuit
communications controller module, 13-6
Transmitter timing diagram
communications controller module, 13-7
Tripping, ultra high-speed, 3-9
Two-channel operation
hot standby direct digital, 13-5
hot standby modem, 13-5

U

Ultra high-speed tripping, 3-9
Unbalance, phase, 3-2
Underground or overhead cable, 3-16, 4-9
Underground cables, 3-16
Unpacking, 5-1
Update mode, 6-44

V

Values display, viewing, 6-36
Ventilation, 5-4
Verification of end-to-end communications, 8-16
Viewing APRIL commands, 6-33
Very short lines, 3-3
Viewing configuration and software information, 6-39
Viewing oscillography data, 6-48
Viewing the alarms display, 6-34
Viewing the sequence of events log, 6-45
Viewing the values display, 6-36
Voltage inversion, 3-1

W

Watchdog reset function
communications controller module, 13-6
Weak infeed applications, 3-15

SECTION 32: SCHEMATICS

Table of Contents

Figure	Title	Assembly No.	Schematic No.	No. of Sheets	Page
9-7	Oscillography Board, part of RFL 9300 display module	106330, 106335, 106325	D-106764-A	5	32-1
10-4	Supervisor Controller module for Charge Comparison System	106300	D-106304-1-B	2	32-6
11-5	RFL 93B ACT-5, 5-Ampere Auxiliary Current Transformer I/O Module	106345	D-105814-E	1	32-8
12-4	Phase Controller modules for RFL 9300 Charge Comparison System	106370	D-103819-D	2	32-9
13-8	Communications Controller modules for RFL 9300 Charge Comparison System	106365	D-103824-E	2	32-11
14-4	Modem module for RFL 9300 Charge Comparison System	106355	D-103829-B	1	32-13
16-4	RFL 93 DD I/O Direct Digital I/O Module	103830-1	D-103834-1-A	1	32-14
17-4	**RFL 9300 Fiber Optics Hot Standby Signal Routing Diagram**	-	-	-	32-15
17-6	RFL 93 FT/FR Singlewidth Fiber Optic Transceiver Module	106360	D-105849-D	1	32-16
18-9	RFL 93 FT/FR Singlewidth Fiber Optic I/O Module – 8M	105850	D-105854-E	1	32-17
18-11	RFL 93 FT/FR Singlewidth Fiber Optic I/O Module – 13M	105855	D-105864-C	1	32-18
18-11	RFL 93 FT/FR Singlewidth Fiber Optic I/O Module – 13S	105860	D-105864-C	1	32-18
18-11	RFL 93 FT/FR Singlewidth Fiber Optic I/O Module – 13SL	105865	D-105869-B	1	32-19
18-11	RFL 93 FT/FR Singlewidth Fiber Optic I/O Module – 15SL	105870	D-105869-B	1	32-19
19-3	9300 PS 48/125 DC power supply module for RFL 9300 Charge Comparison System	106715-1	D-106719-E	1	32-20
20-7	RFL 93B RELAY I/O module,	106388-1, 106388-2, 106388-3	D-106389-D	3	32-21
21-4	RFL 93 ALARM I/O Input/Output module	104775-5	D-104779-5-D	1	32-24
21-5	RFL 93 ALARM I/O (24V) Input/Output module	104775-6	D-104779-6-A	1	32-25
22-5	RFL 93 Short Haul Fiber Module	107500	D-107504-D	3	32-26
23-5	RFL 93 G.703 module	106730	D-106734-D	1	32-29
24-7	9300 Single Pole Chassis	-	D-106714-C	2	32-30
24-9	9300 Single Pole Chassis, Rear Panel	-	D-106709-C	1	32-32
25-4	RFL 93 INTER Interconnect Motherboard	105855	D-103909-1-D	1	32-33
25-6	RS-232 Front Panel Interface	106755	C-106759-B	1	32-34
26-3	Power Converter I/O – 250 VDC for RFL 9300 Charge Comparison System	106350	C-106354-D	1	32-35

This page intentionally left blank

SECTION 32: SCHEMATICS

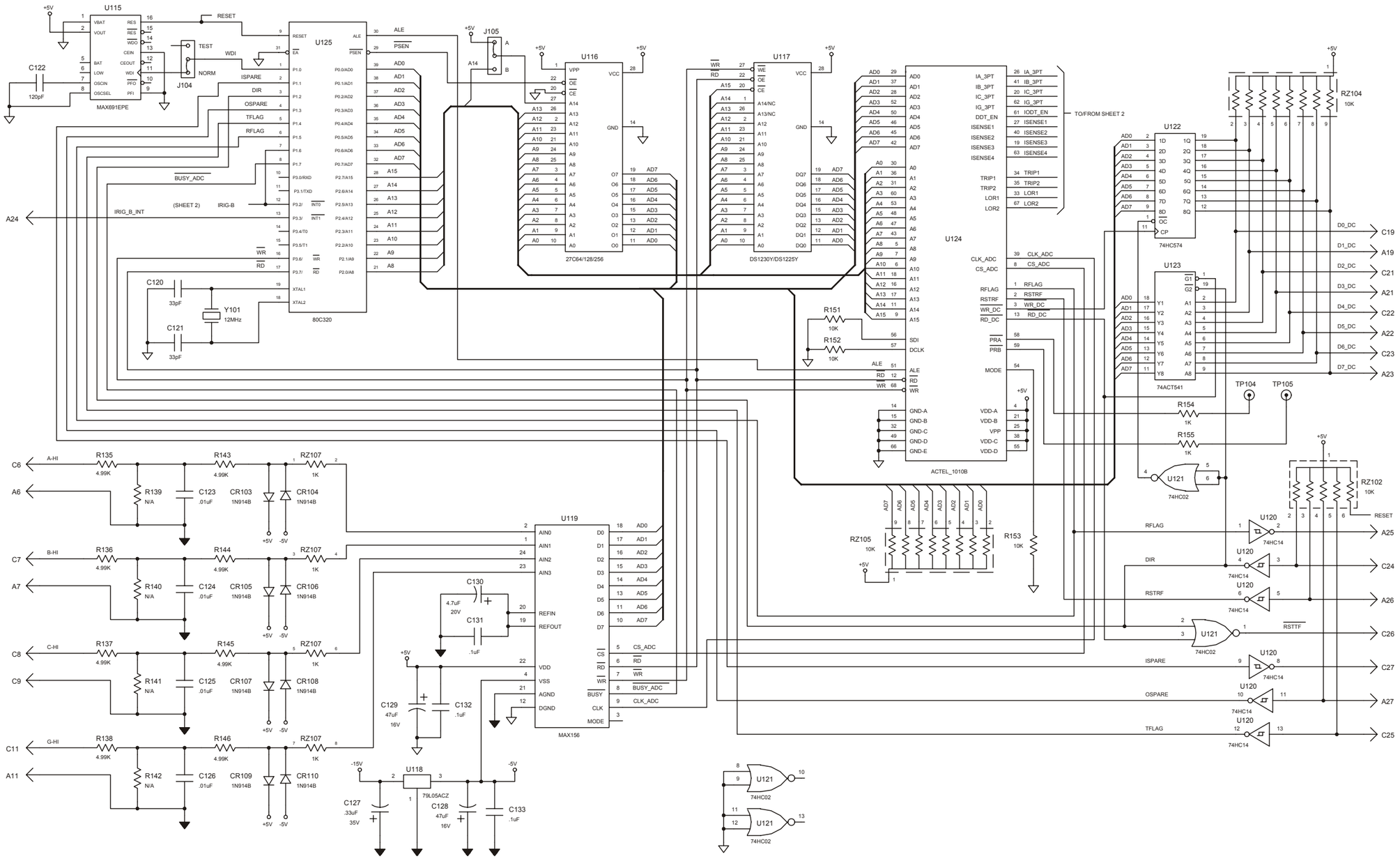


Figure 9- 7. Oscillography Board, part of RFL 9300 display module (Assembly No. 106330; Schematic No. D-106764-A) Sheet 1 of 5

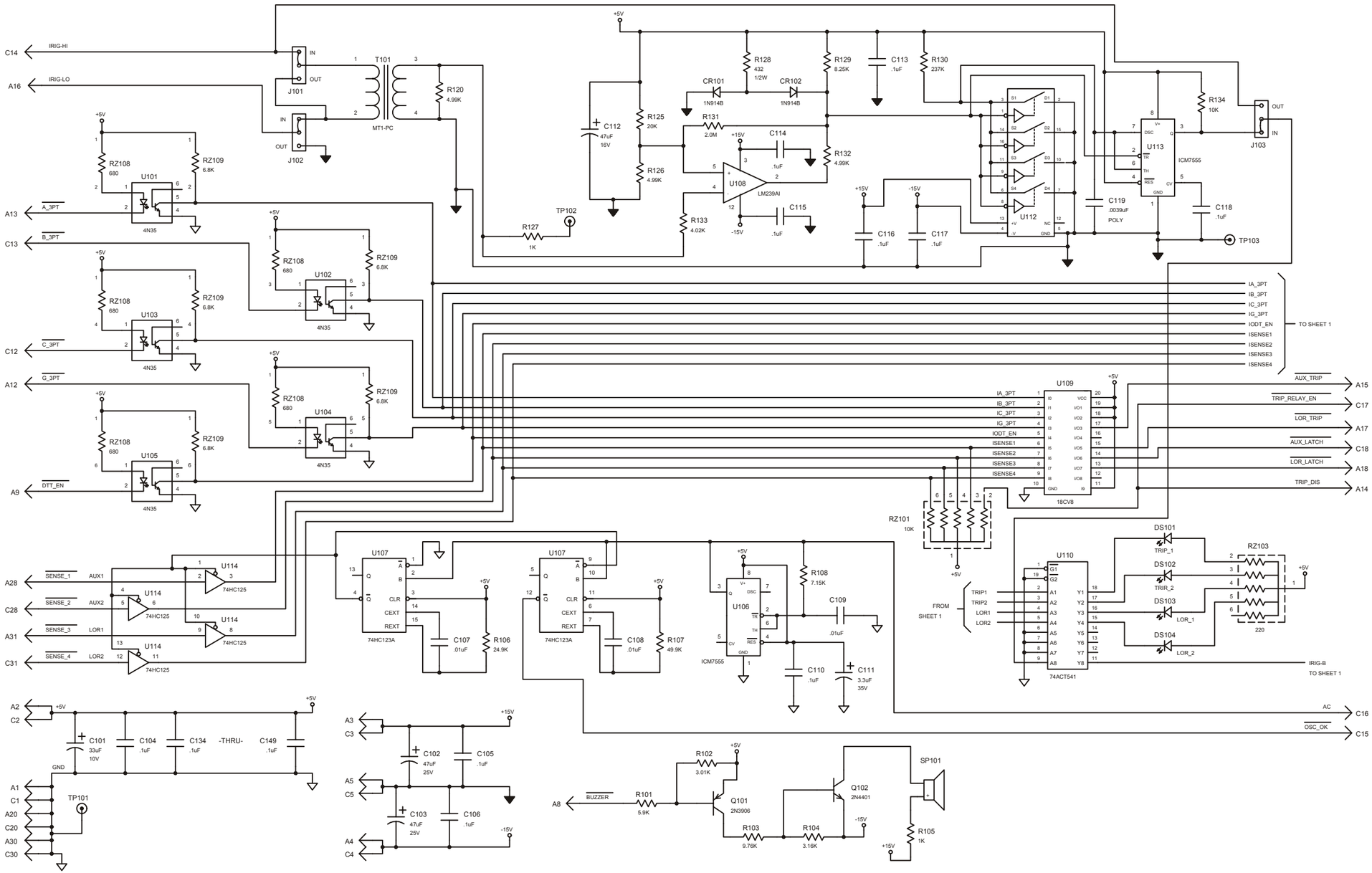


Figure 9- 7. Oscillography Board, part of RFL 9300 display module (Assembly No. 106330; Schematic No. D-106764-A) Sheet 2 of 5

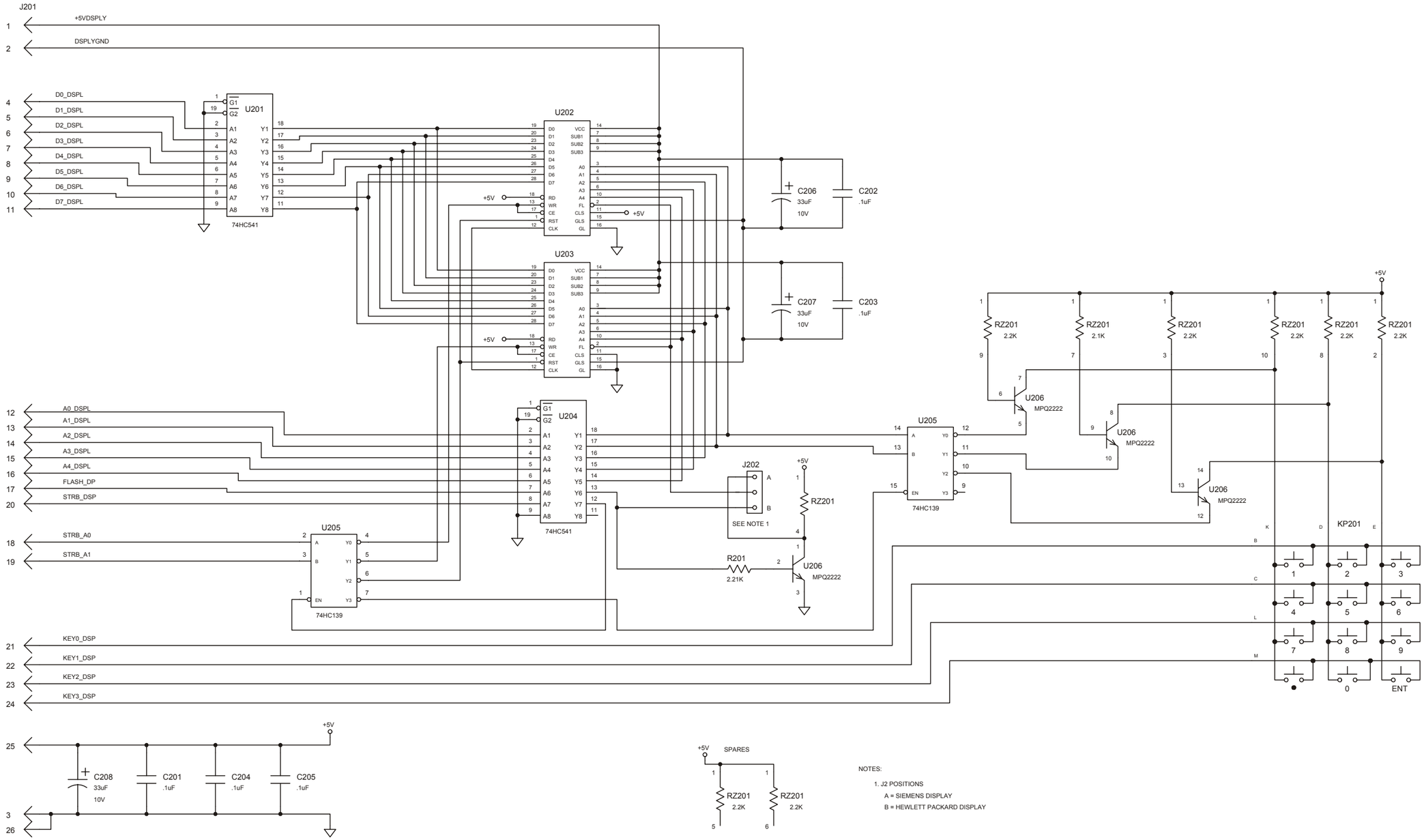


Figure 9- 7. Front Panel Display, part of RFL 9300 display module (Assembly No. 106335; Schematic No. D-106764-A) Sheet 3 of 5

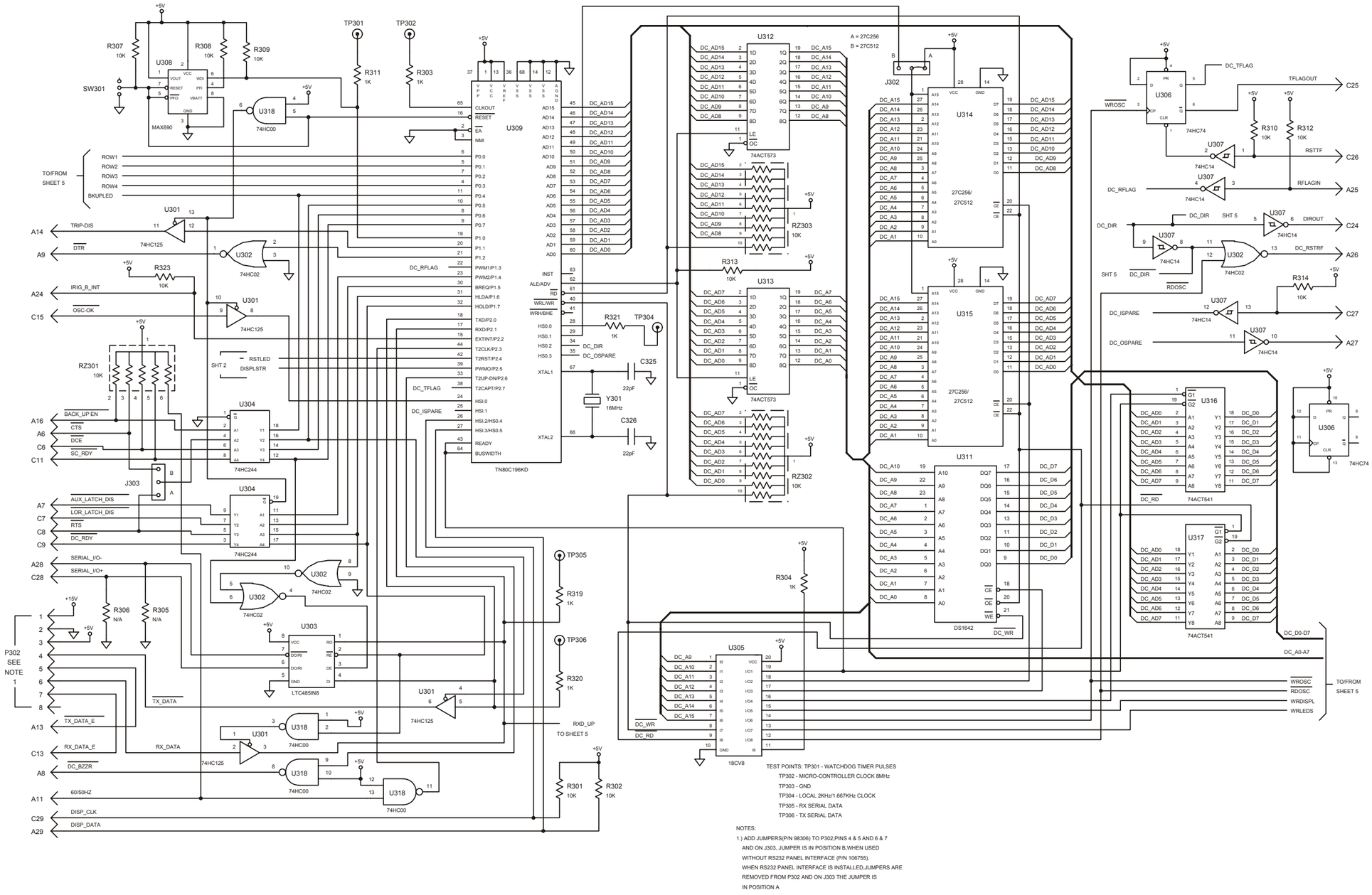


Figure 9- 7. Display Controller, part of 9300 display modules (Assembly No. 10625; Schematic No. D-106764-A) Sheet 4 of 5

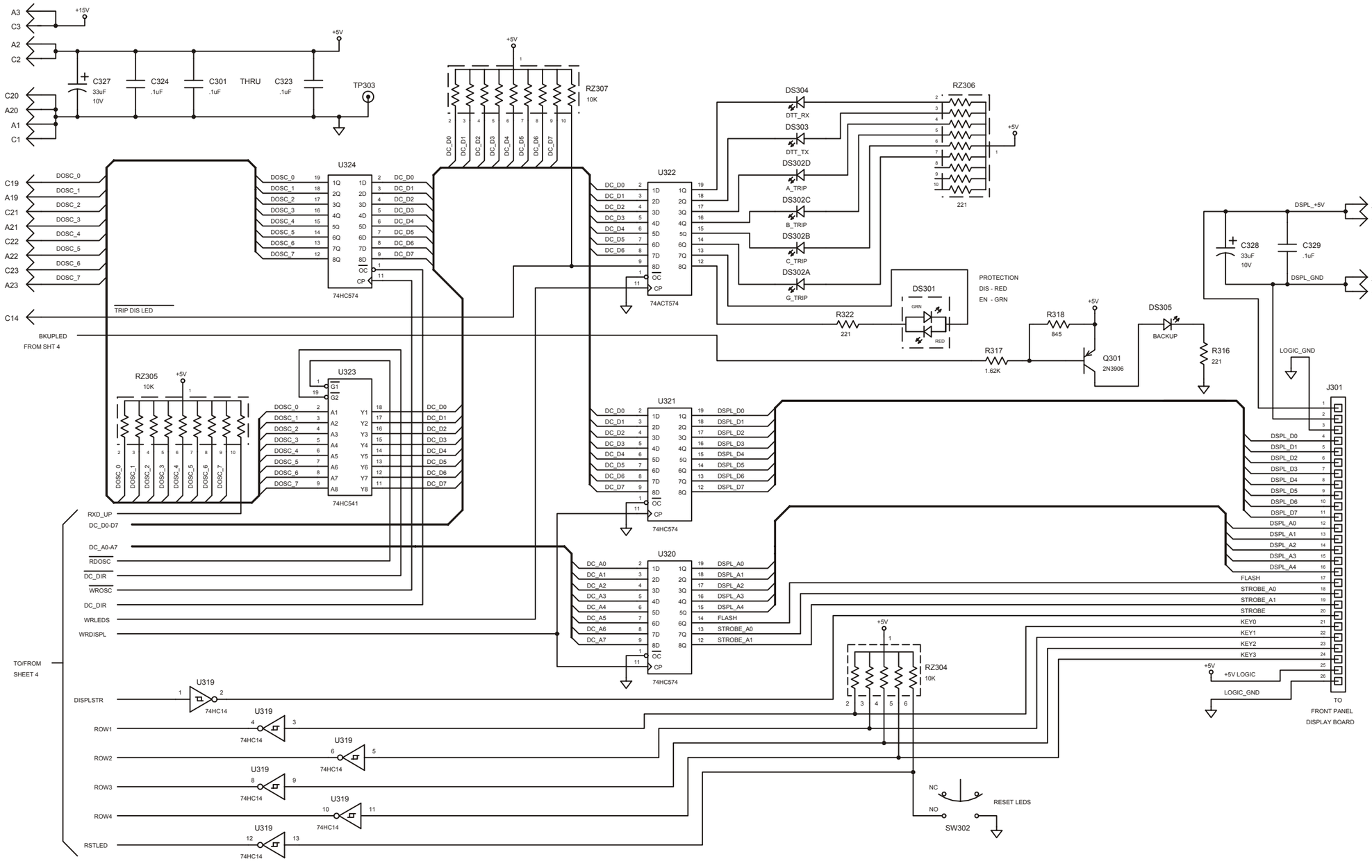


Figure 9- 7. Display Controller, part of 9300 display module (Assembly No. 106325; Schematic No. D-106764-A) Sheet 5 of 5

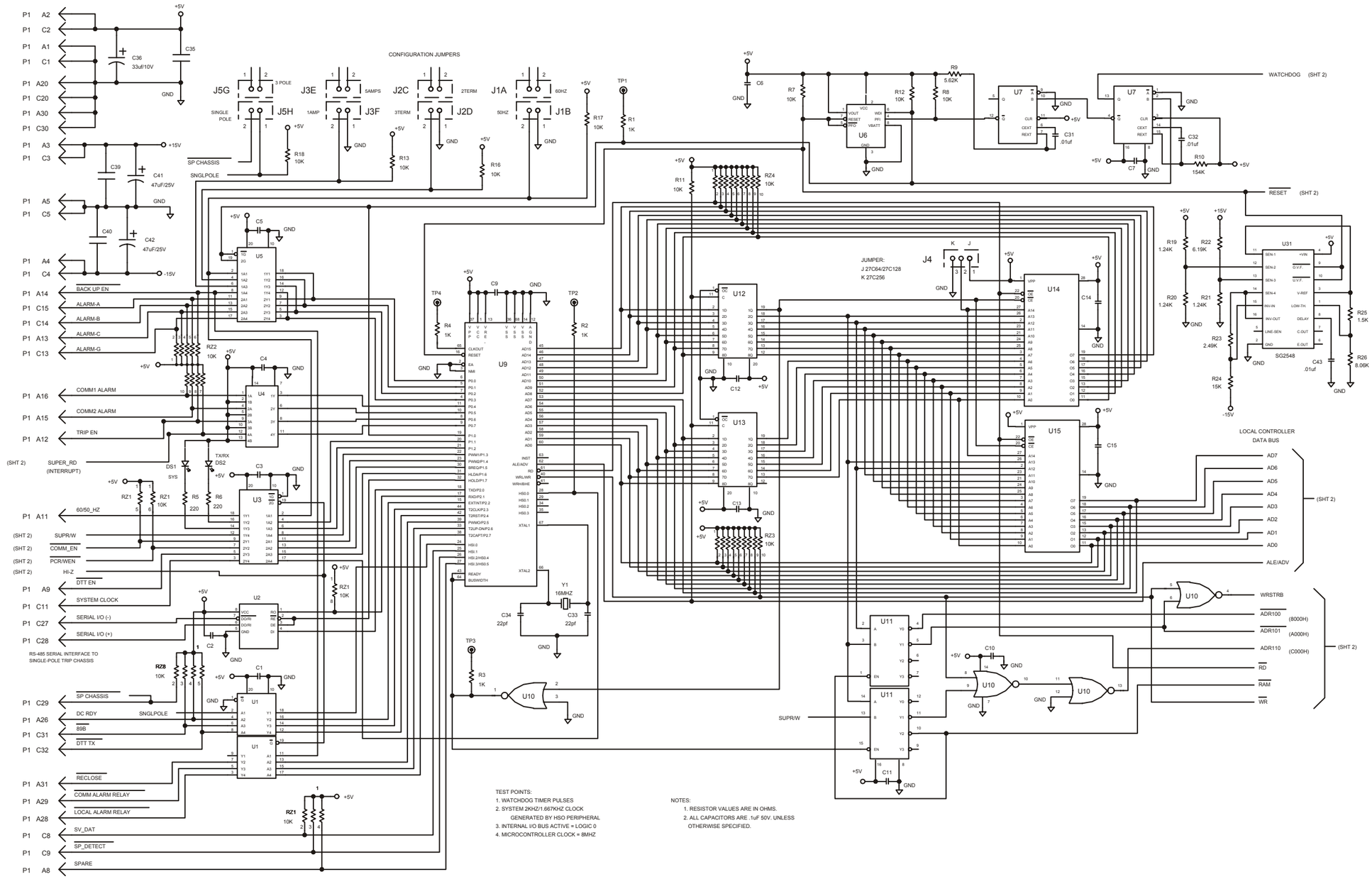


Figure 10- 4. Supervisor Controller module for RFL 9300 Charge Comparison System (Assembly No. 106300; Schematic No. D-106304-1-B) Sheet 1 of 2

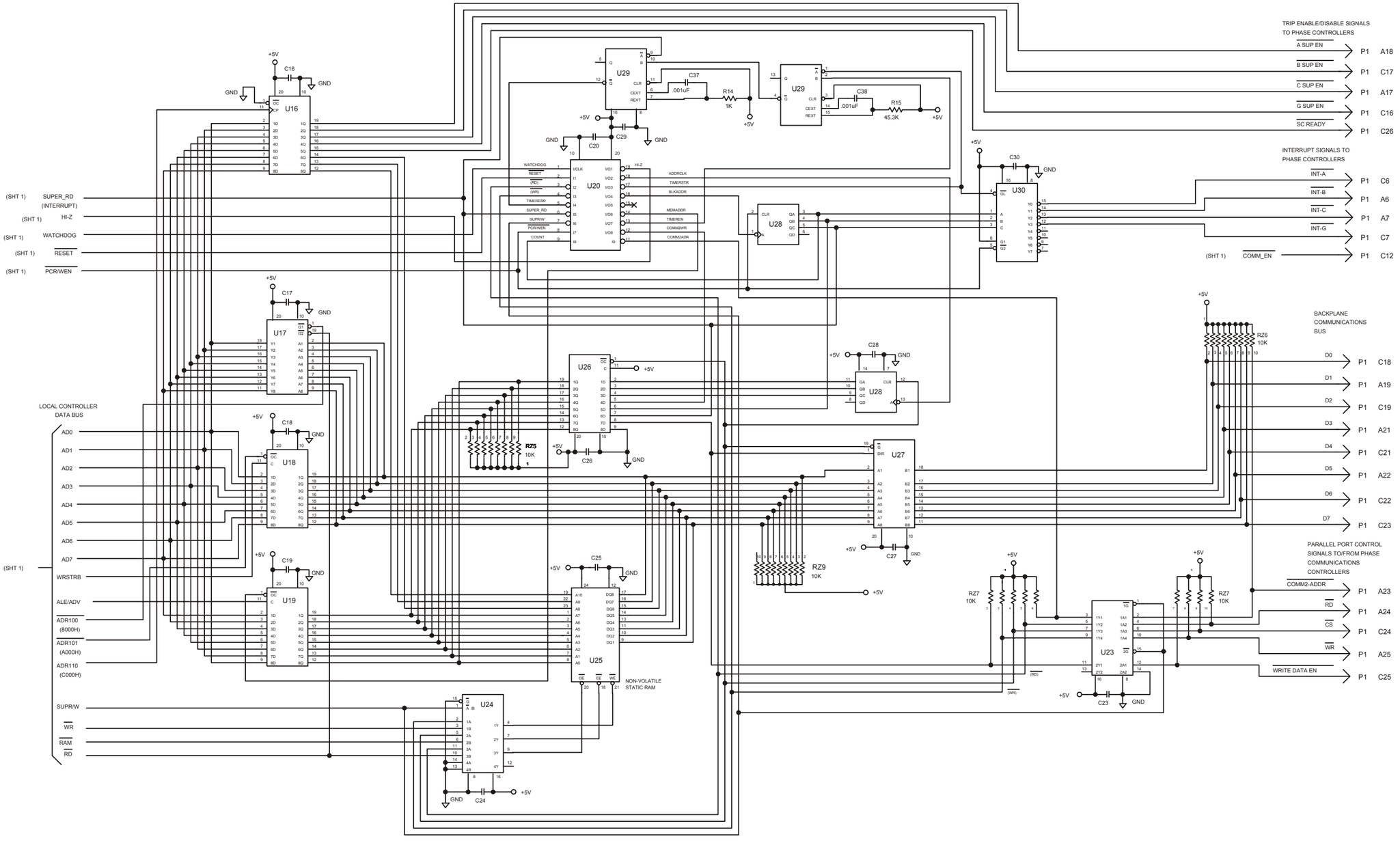
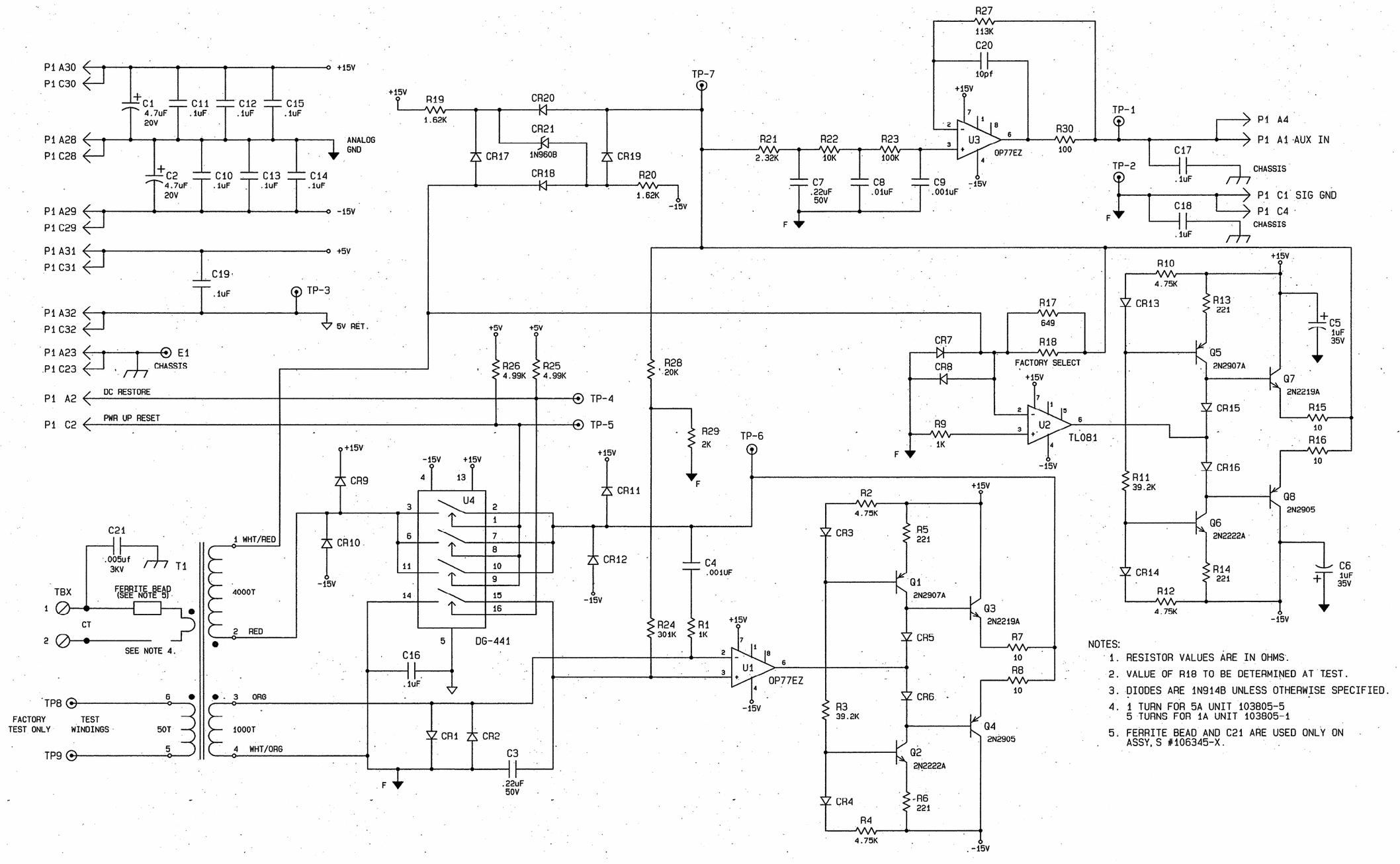


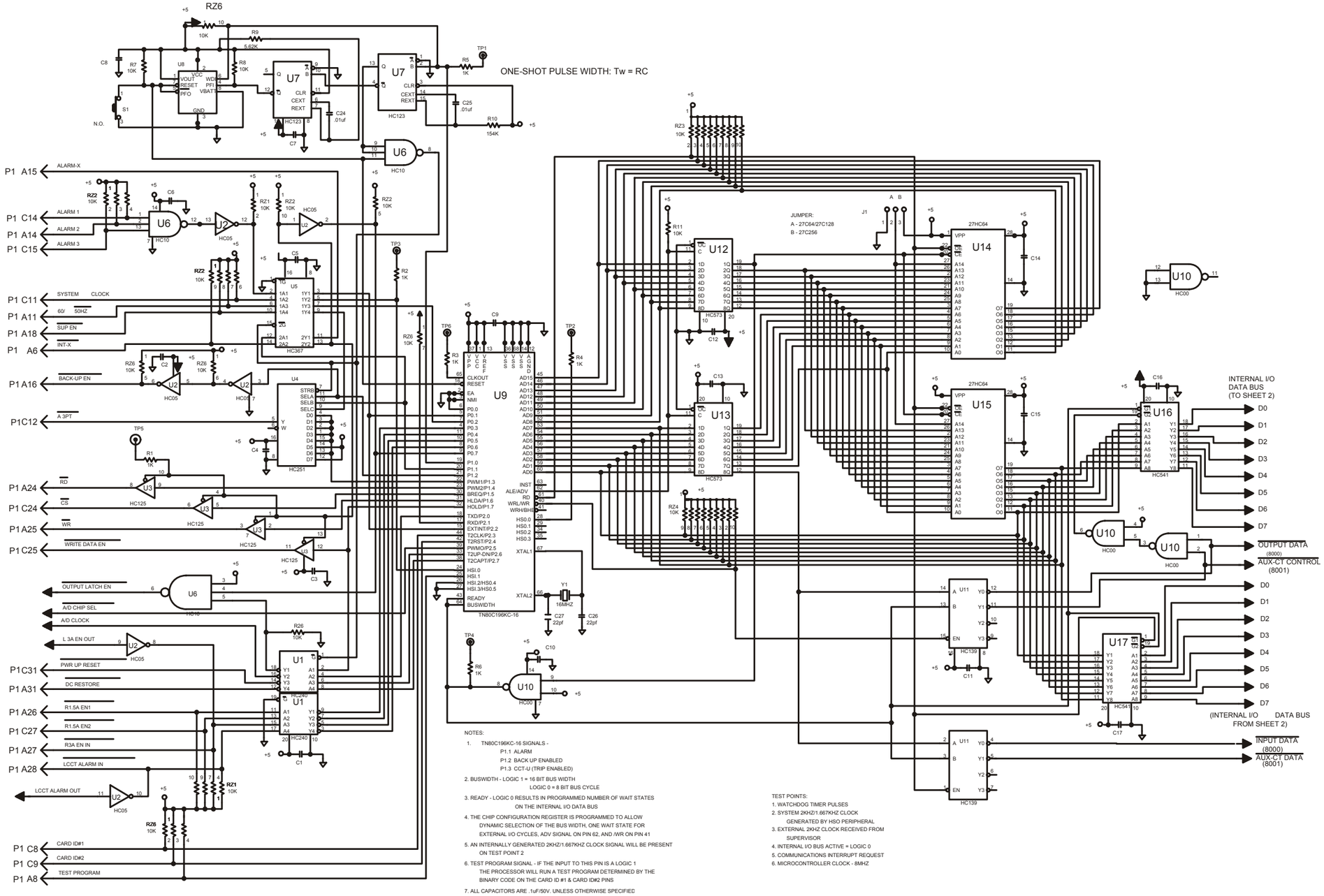
Figure 10- 4. Supervisor Controller module for RFL 9300 Charge Comparison System (Assembly No. 106300; Schematic No. D-106304-1-B) Sheet 2 of 2



NOTES:

1. RESISTOR VALUES ARE IN OHMS.
2. VALUE OF R18 TO BE DETERMINED AT TEST.
3. DIODES ARE 1N914B UNLESS OTHERWISE SPECIFIED.
4. 1 TURN FOR 5A UNIT 103805-5
   5 TURNS FOR 1A UNIT 103805-1
5. FERRITE BEAD AND C21 ARE USED ONLY ON ASSY, S #106345-X.

Figure 11- 5. RFL 93B ACT-5 5-Ampere Auxiliary Current Transformer I/O Module (Assembly No. 106345; Schematic No. D-105814, Rev. E)



NOTES:

1. TN80C196KC-16 SIGNALS -
   P1.1 ALARM
   P1.2 BACK UP ENABLED
   P1.3 CCT-U (TRIP ENABLED)
2. BUSWIDTH - LOGIC 1 = 16 BIT BUS WIDTH
   LOGIC 0 = 8 BIT BUS CYCLE
3. READY - LOGIC 0 RESULTS IN PROGRAMMED NUMBER OF WAIT STATES ON THE INTERNAL I/O DATA BUS
4. THE CHIP CONFIGURATION REGISTER IS PROGRAMMED TO ALLOW DYNAMIC SELECTION OF THE BUS WIDTH, ONE WAIT STATE FOR EXTERNAL I/O CYCLES, ADV SIGNAL ON PIN 62, AND /WR ON PIN 41
5. AN INTERNALLY GENERATED 2KHZ/1.667KHZ CLOCK SIGNAL WILL BE PRESENT ON TEST POINT 2
6. TEST PROGRAM SIGNAL - IF THE INPUT TO THIS PIN IS A LOGIC 1 THE PROCESSOR WILL RUN A TEST PROGRAM DETERMINED BY THE BINARY CODE ON THE CARD ID #1 & CARD ID#2 PINS
7. ALL CAPACITORS ARE .1uF/50V. UNLESS OTHERWISE SPECIFIED

TEST POINTS:

1. WATCHDOG TIMER PULSES
2. SYSTEM 2KHZ/1.667KHZ CLOCK GENERATED BY HSO PERIPHERAL
3. EXTERNAL 2KHZ CLOCK RECEIVED FROM SUPERVISOR
4. INTERNAL I/O BUS ACTIVE = LOGIC 0
5. COMMUNICATIONS INTERRUPT REQUEST
6. MICROCONTROLLER CLOCK - 8MHZ

Figure 12- 4. Phase Controller modules for RFL 9300 Charge Comparison System (Assembly No. 106370; Schematic No. D-103819, Rev. D) Sheet 1 of 2

P1

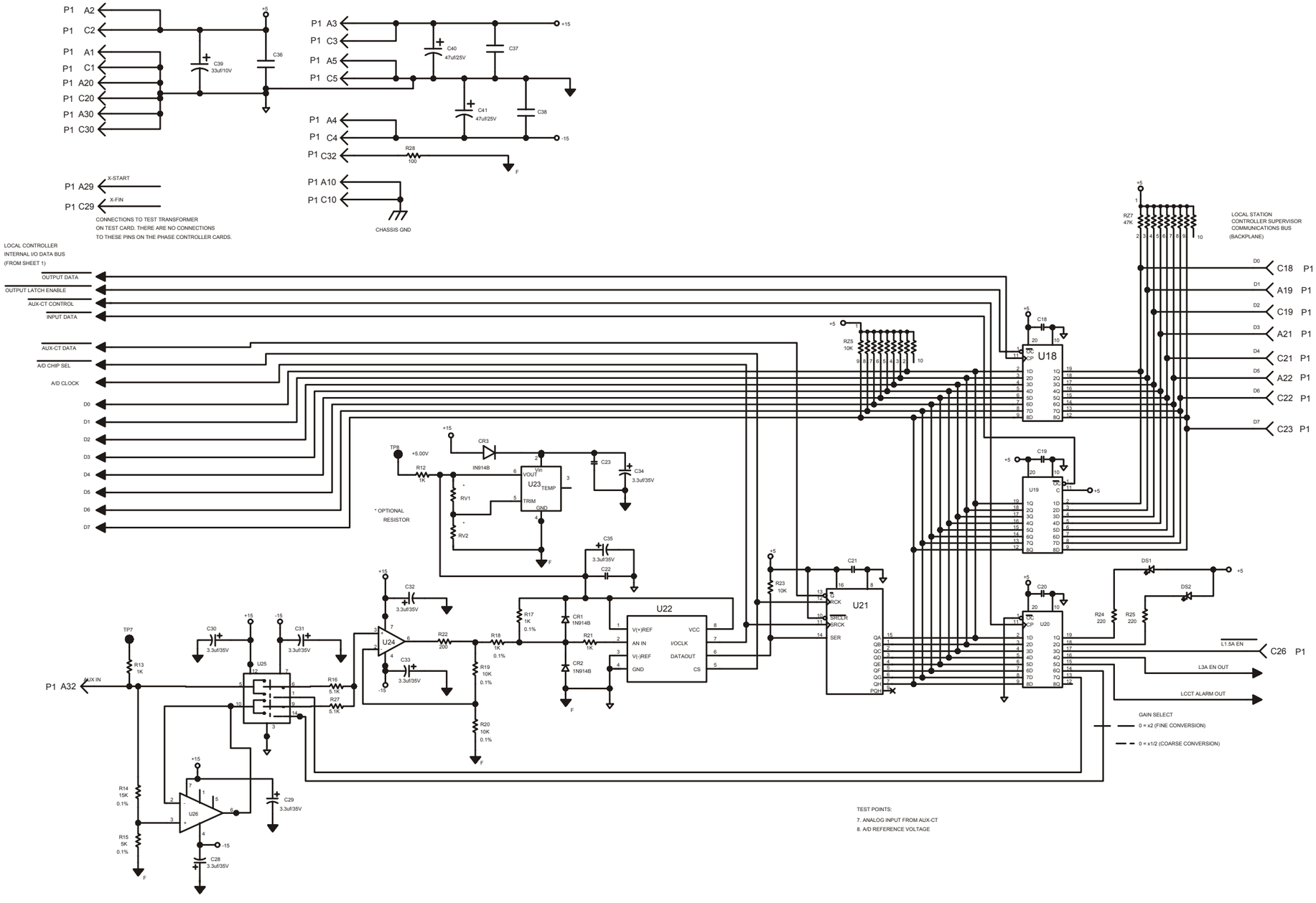


Figure 12- 4. Phase Controller module for RFL 9300 Charge Comparison System (Assembly No. 106370; Schematic No. D-103819, Rev. D) Sheet 2 of 2

IC POWER CHART				
IC	+5V	GND	N.C.	MANUFACTURER P/N
U10	14	7		74HCT86
U11	14	7	12	74HC04
U16	14	7		74HC32
U17	20	10		74HC573
U19, 20	20	10		74ACT573
U21, 22	28	14		27C256
U23	14	7		74ACT02
U25, 27	20	10		74HC245
U26	20	10		74HC541
U28	20	10	3, 9	74HC244
U29	14	7		74HC125

ALL CAP VALUES ARE .1UF 50V UNLESS OTHERWISE STATED
ALL RESISTOR VALUES ARE IN OHMS
J1 SELECTION : B 27C64/27C128 A 27C256

Figure 13- 8. Communications Controller modules for RFL 9300
Charge Comparison System (Assembly No. 106365; Schematic No. D-103824, Rev.E) Sheet 1 of 2

IC POWER CHART				
IC	+5V	GND	N.C.	MANUFACTURER P/N
U1	16	8	5	34C86
U2	16	8	10, 11, 13, 14	34C87
U3, 4	14	7		74HC164
U5	28	14		27C256
U6	20	10		74HC688
U7	20	10		74HC573
U8, 12, 15	14	7	6/6.9/	74HC74
U9	14	7		74HC393
U11	14	7	12	74HC04
U13, 14	16	8		74HC597

NOTES : ALL CAP VALUES ARE .1UF 50V UNLESS OTHERWISE STATED
ALL RESISTOR VALUES ARE IN OHMS
J2 SELECTION : B FOR 27C64/27C128 A FOR 27C256

Figure 13- 8. Communications controller module for RFL 9300 Charge Comparison System (Assembly No. 106365; Schematic No. D-103824, Rev. E) Sheet 2 of 2

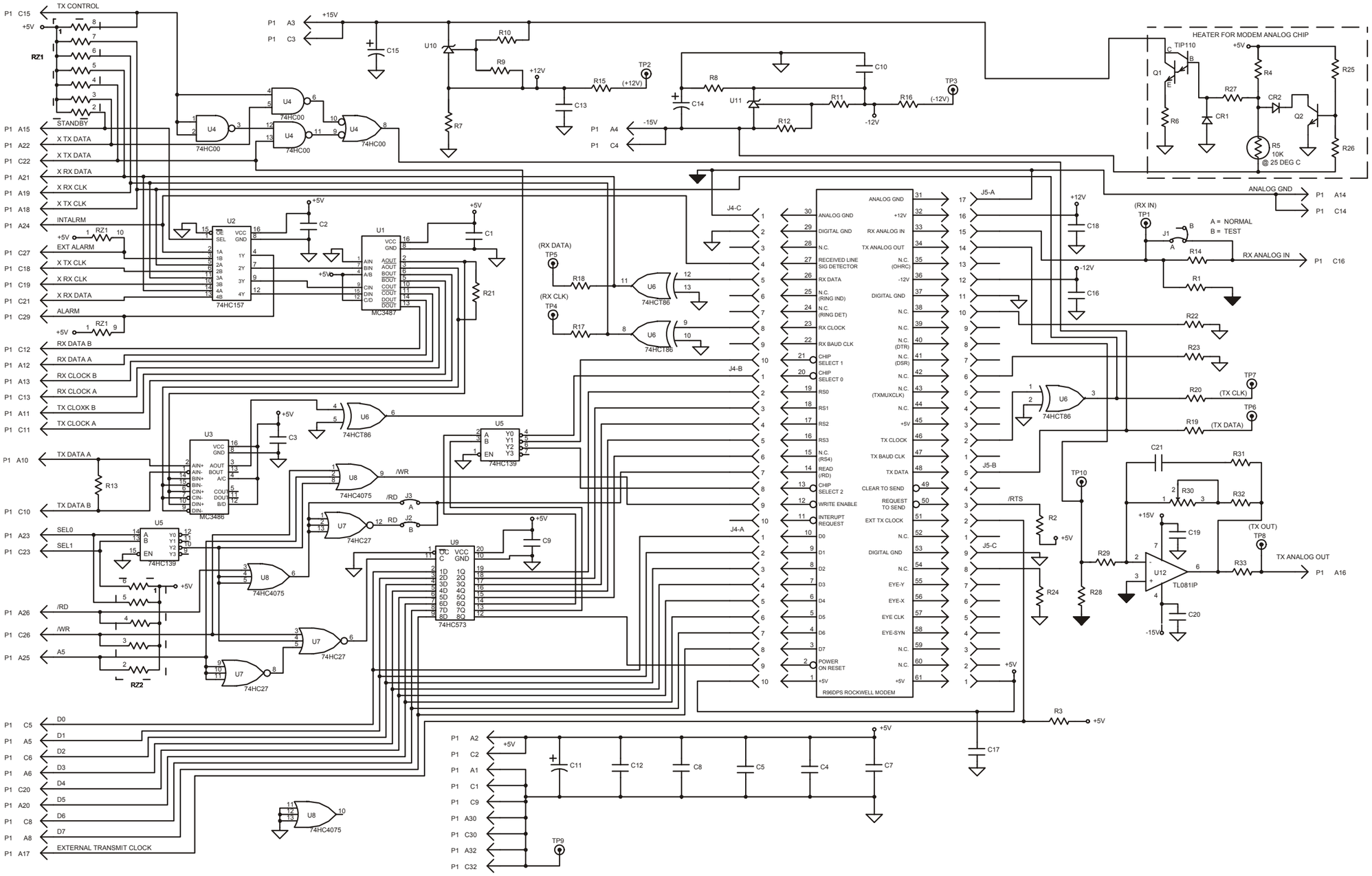
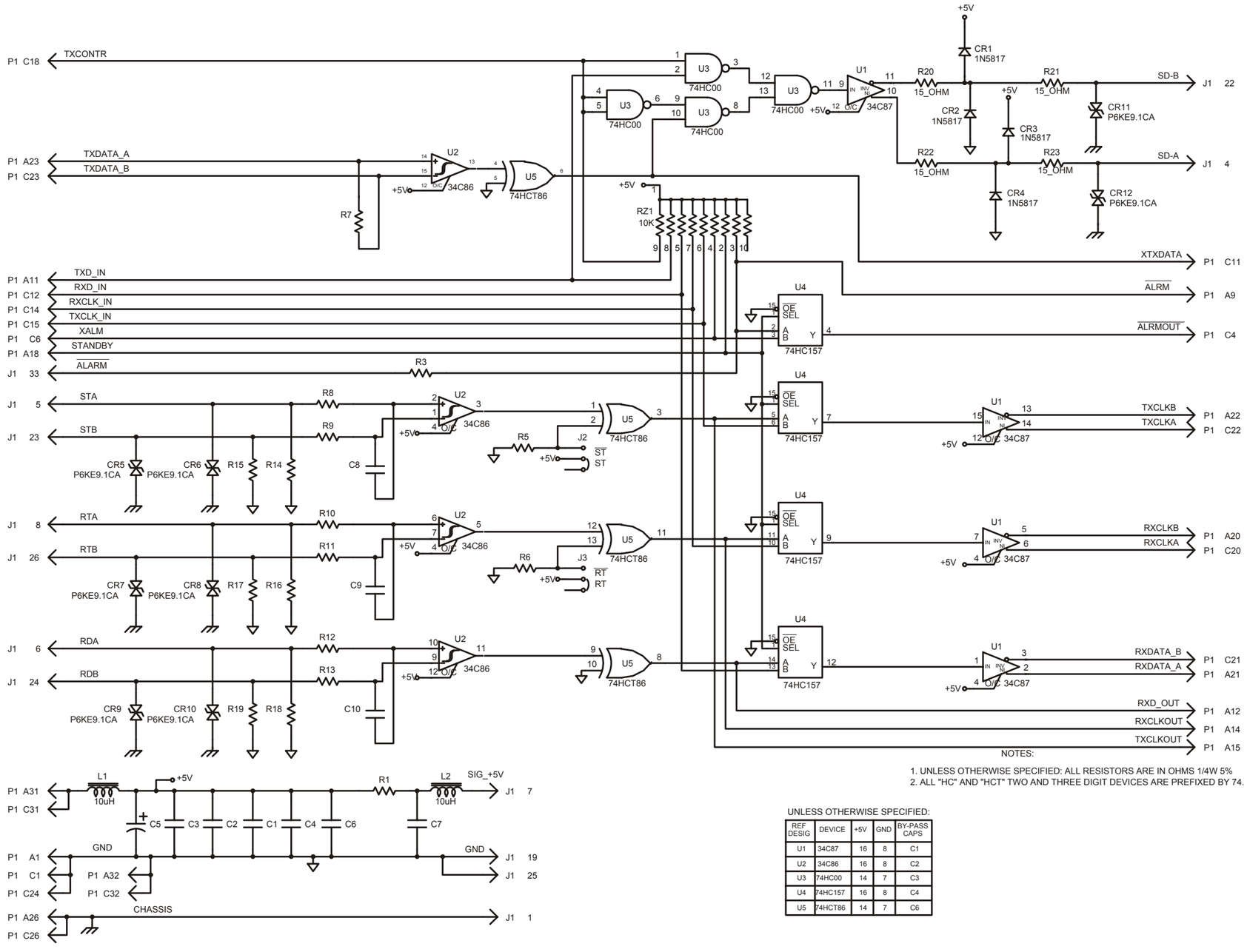


Figure 14- 4. Modem module for RFL 9300 Charge Comparison System (Assembly No. 106355; Schematic No. D-103829, Rev. B)



NOTES:

1. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL "HC" AND "HCT" TWO AND THREE DIGIT DEVICES ARE PREFIXED BY 74.

UNLESS OTHERWISE SPECIFIED:

REF DESIG	DEVICE	+5V	GND	BY-PASS CAPS
U1	34C87	16	8	C1
U2	34C86	16	8	C2
U3	74HC00	14	7	C3
U4	74HC157	16	8	C4
U5	74HCT86	14	7	C6

Figure 16- 4. RFL 93 DD I/O Direct Digital I/O Module (Assembly No. 103830-1; Schematic No. D-103834-1, Rev. A)

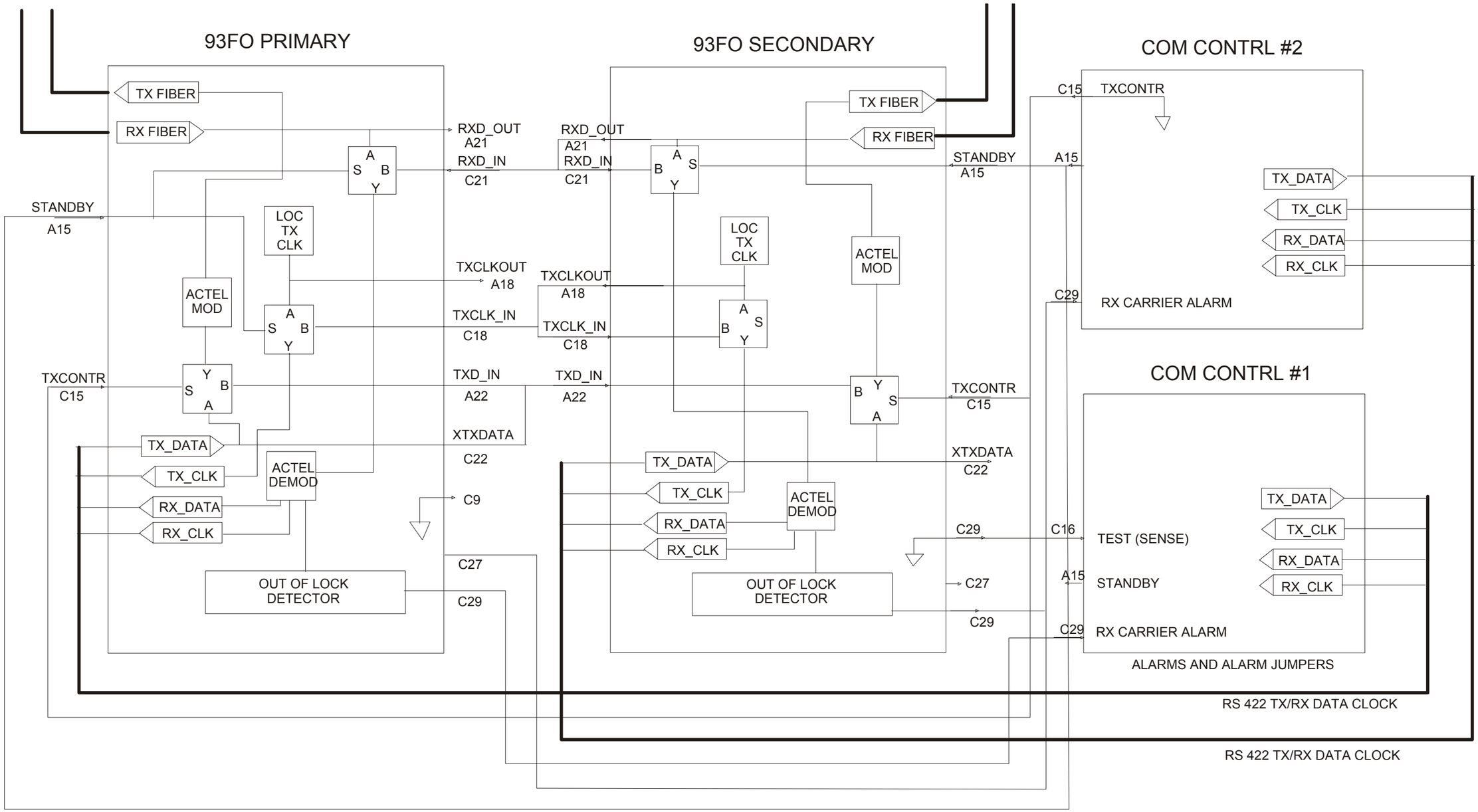


Figure 17- 4. RFL 9300 Fiber Optics Hot Standby Signal Routing Diagram

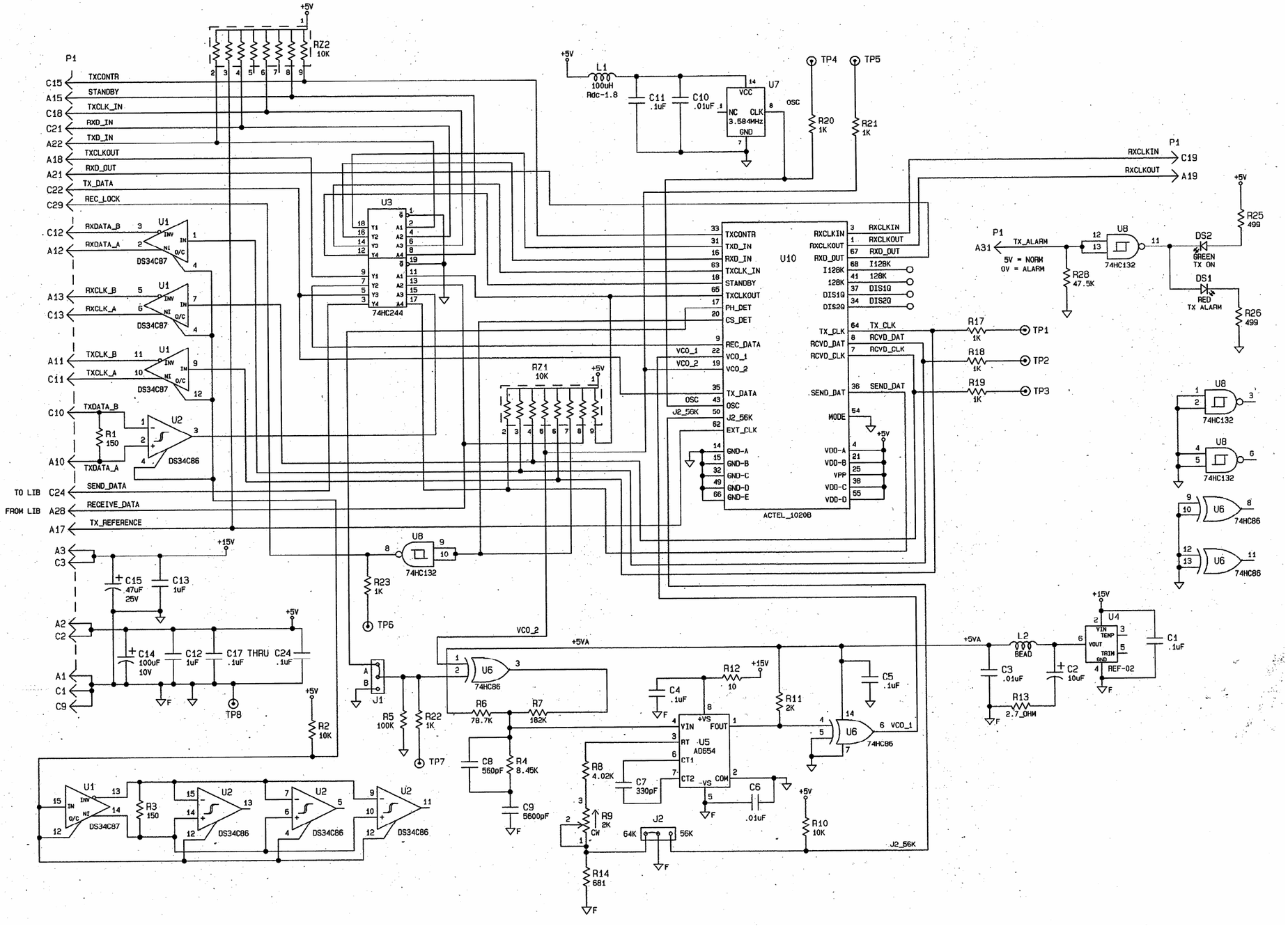


Figure 17-6. RFL 93 FT/FR Singlewidth Fiber Optic Transceiver Module (Assembly No. 106360; Schematic No. D-105849, Rev. D)

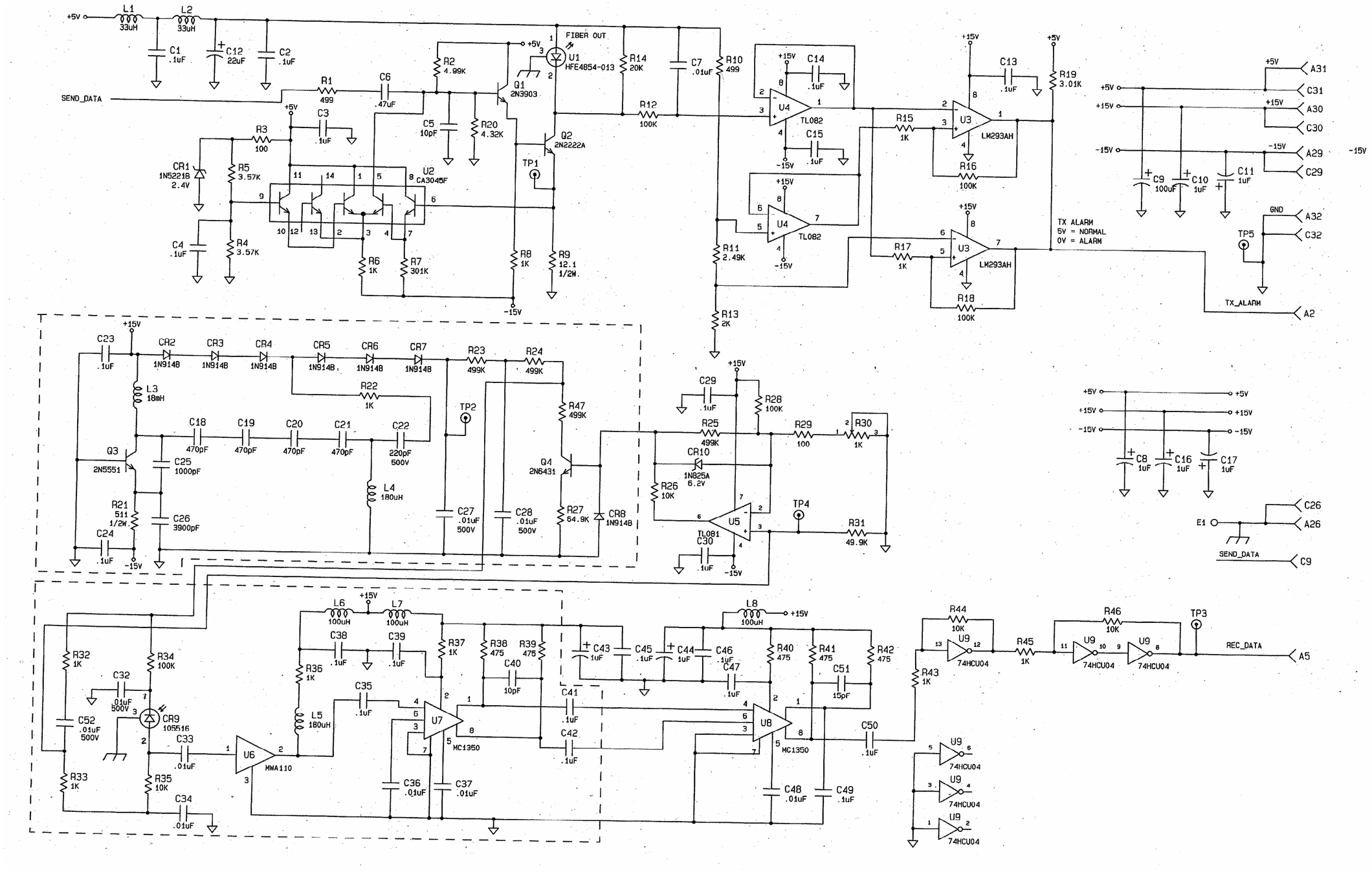


Figure 18- 9. RFL 93 FT/FR Singlewidth Fiber Optic I/O Module -8M (Assembly No. 105850; Schematic No. D-105854, Rev. E)

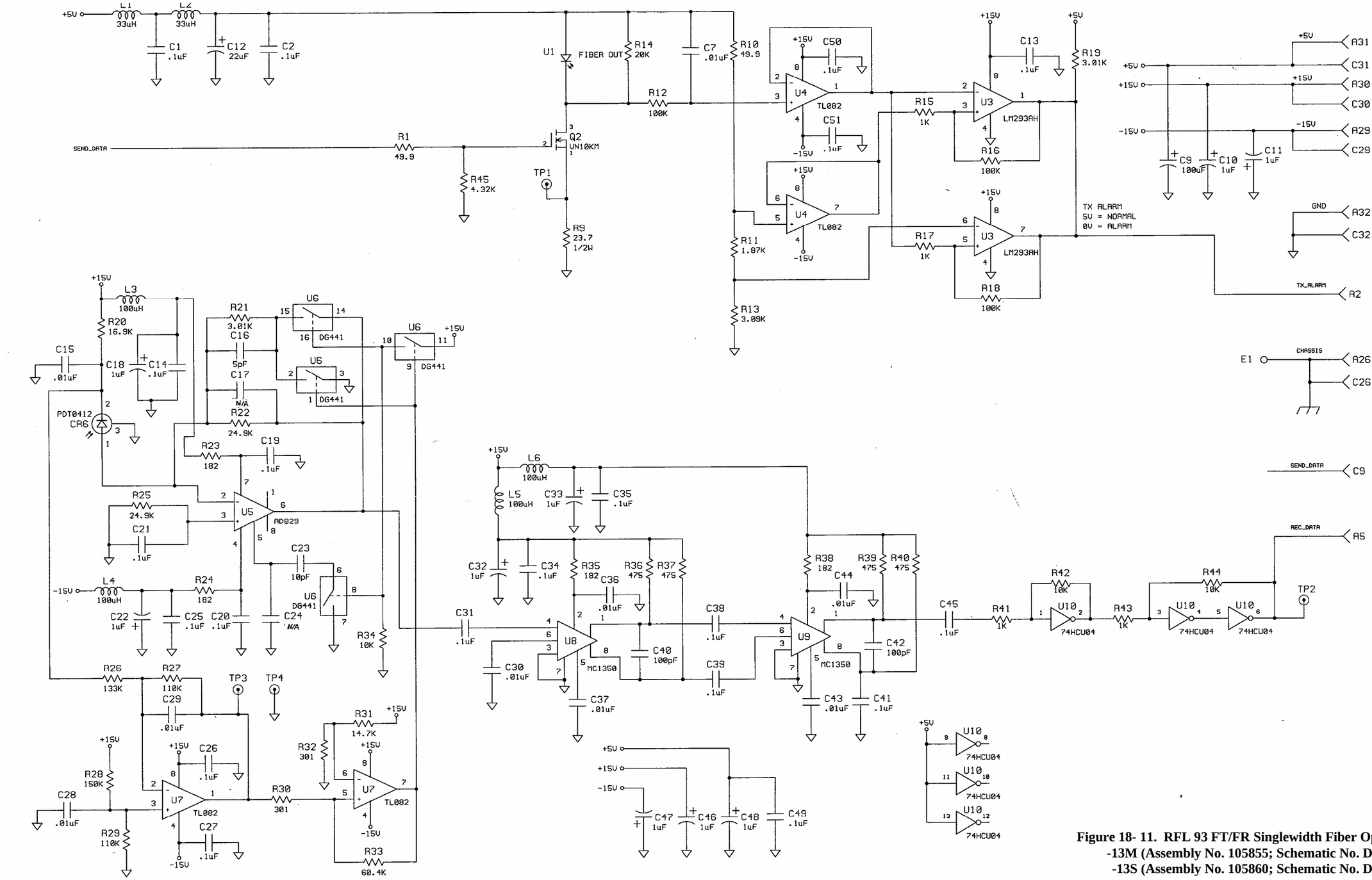


Figure 18- 11. RFL 93 FT/FR Singlewidth Fiber Optic I/O Modules
-13M (Assembly No. 105855; Schematic No. D-105864, Rev. C)
-13S (Assembly No. 105860; Schematic No. D-105864, Rev. C)

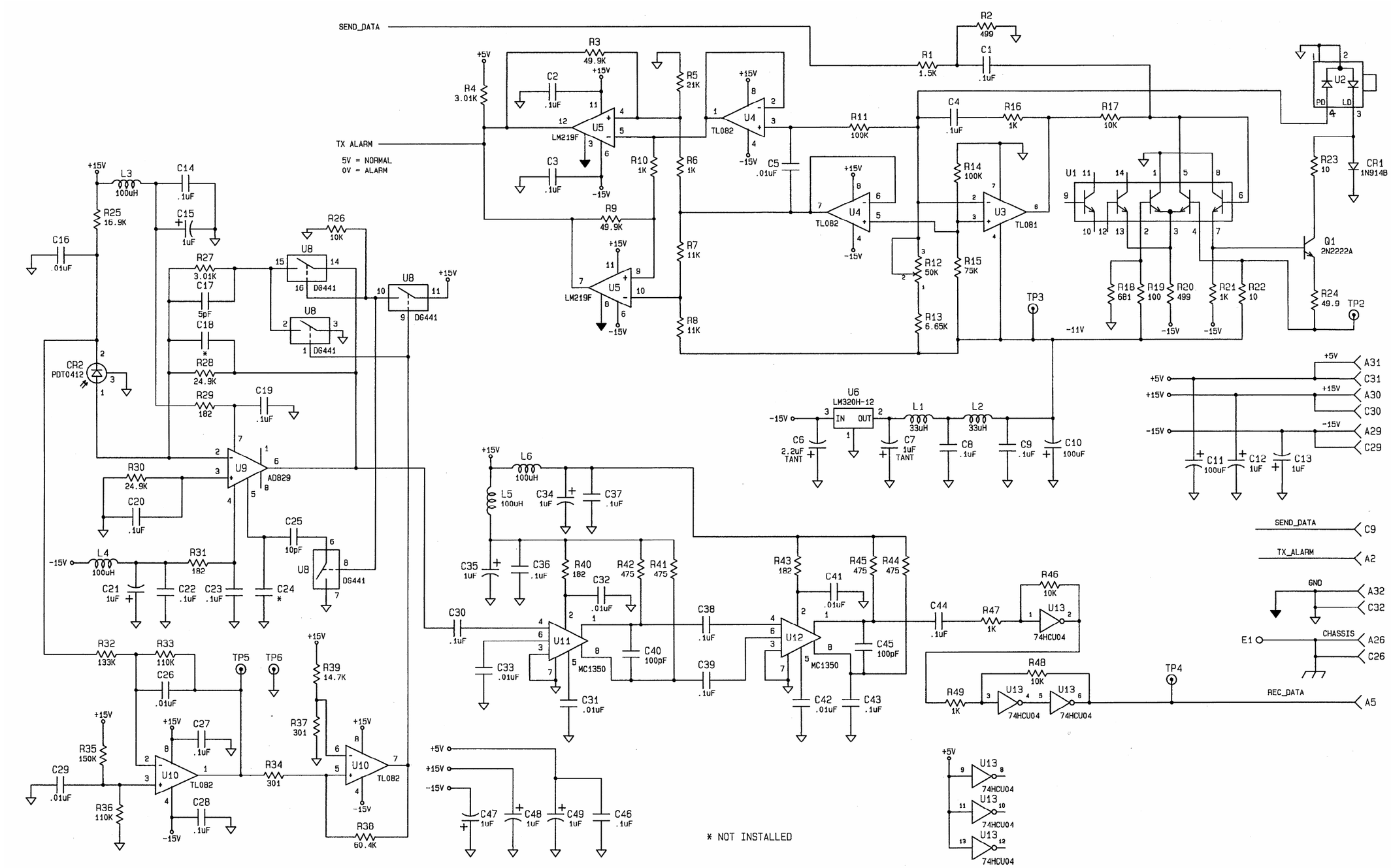


Figure 18- 13. RFL 93 FT/FR Singlewidth Fiber Optic I/O Modules
-13SL (Assembly No. 105865; Schematic No. D-105869, Rev. B)
15SL (Assembly No. 105870; Schematic No. D-105869, Rev. B)

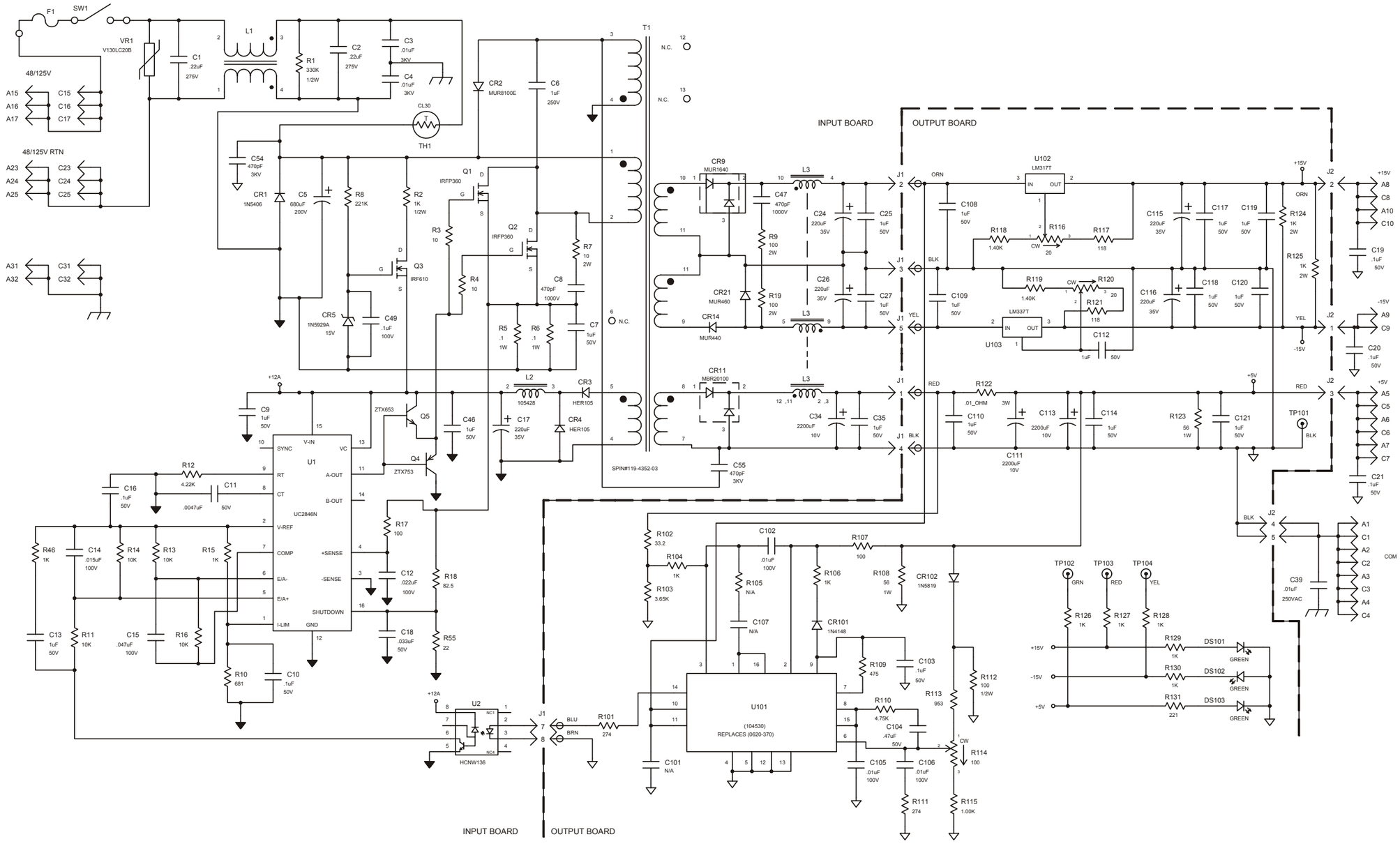


Figure 19-3. 9300 PS 48/125 DC power supply module for RFL 9300 Charge Comparison System (Assembly No. 106715-1; Schematic No. 106719-E)

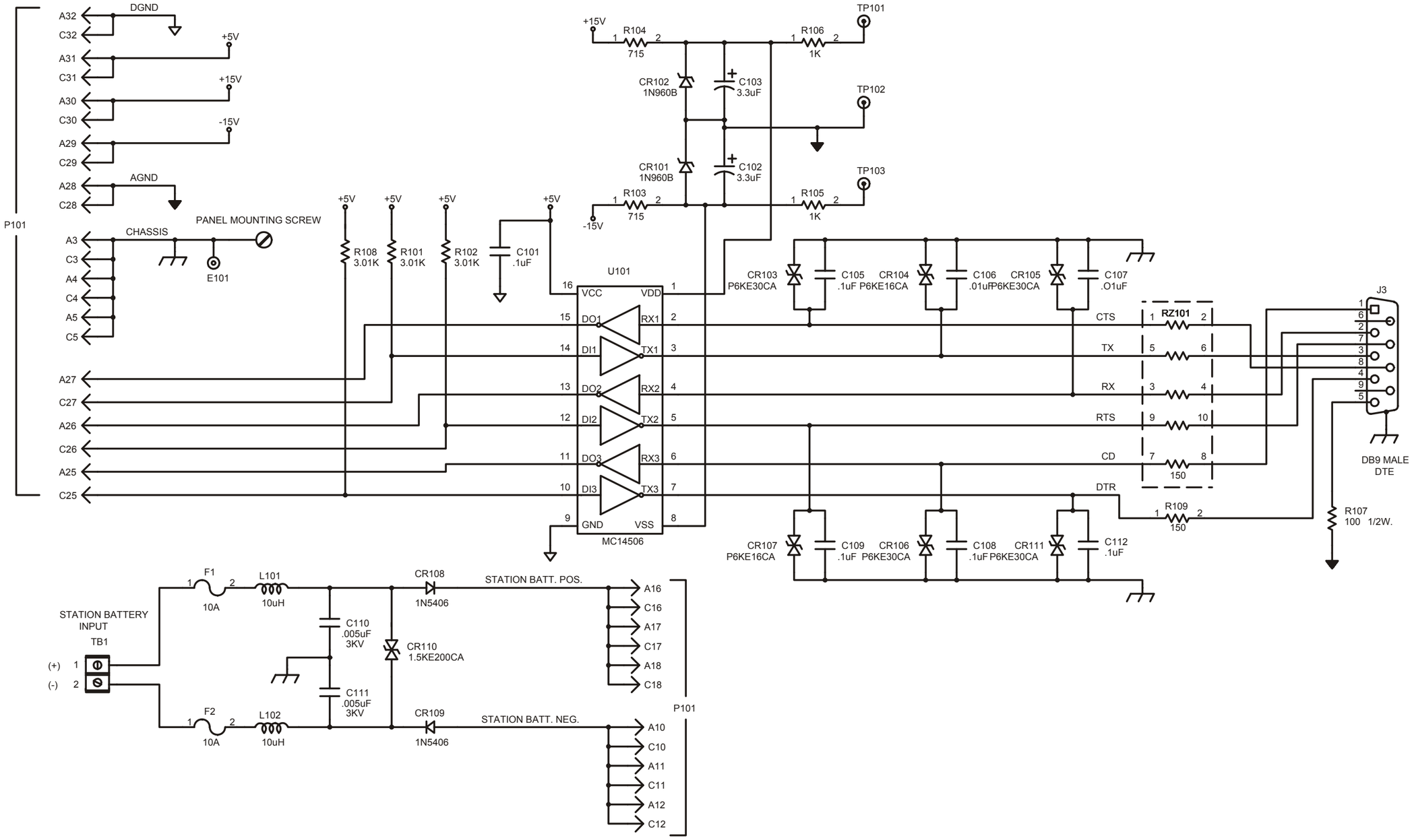


Figure 20- 7. RFL 93B RELAY I/O module, Power/RS-232 board (Assembly No. 106388-1; Schematic No. D-106389, Rev. D) Sheet 1 of 3

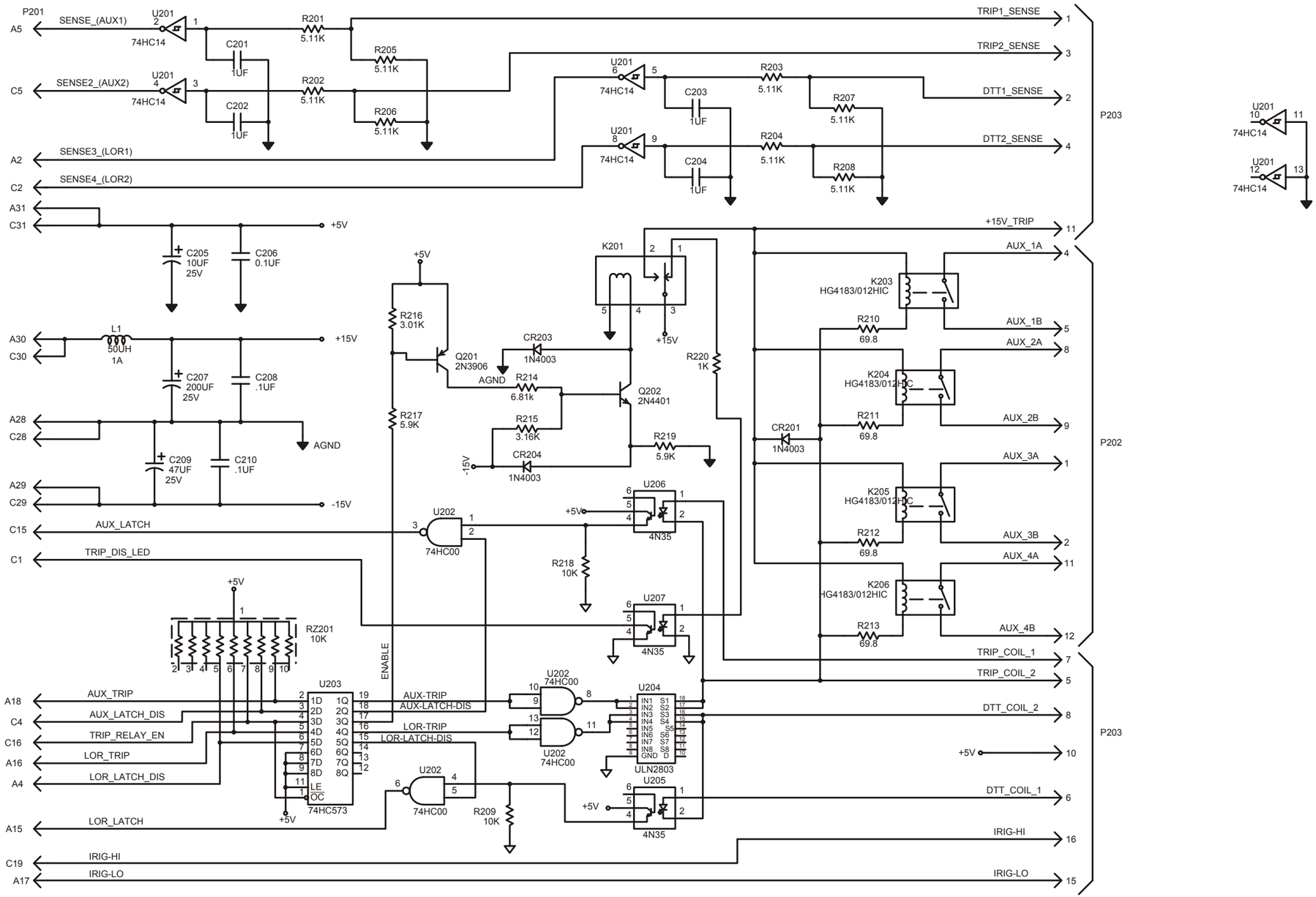


Figure 20- 7. RFL 93B RELAY I/O module, Current Sense board (Assembly No. 106388-2; Schematic No. D-106389, Rev. D) Sheet 2 of 3

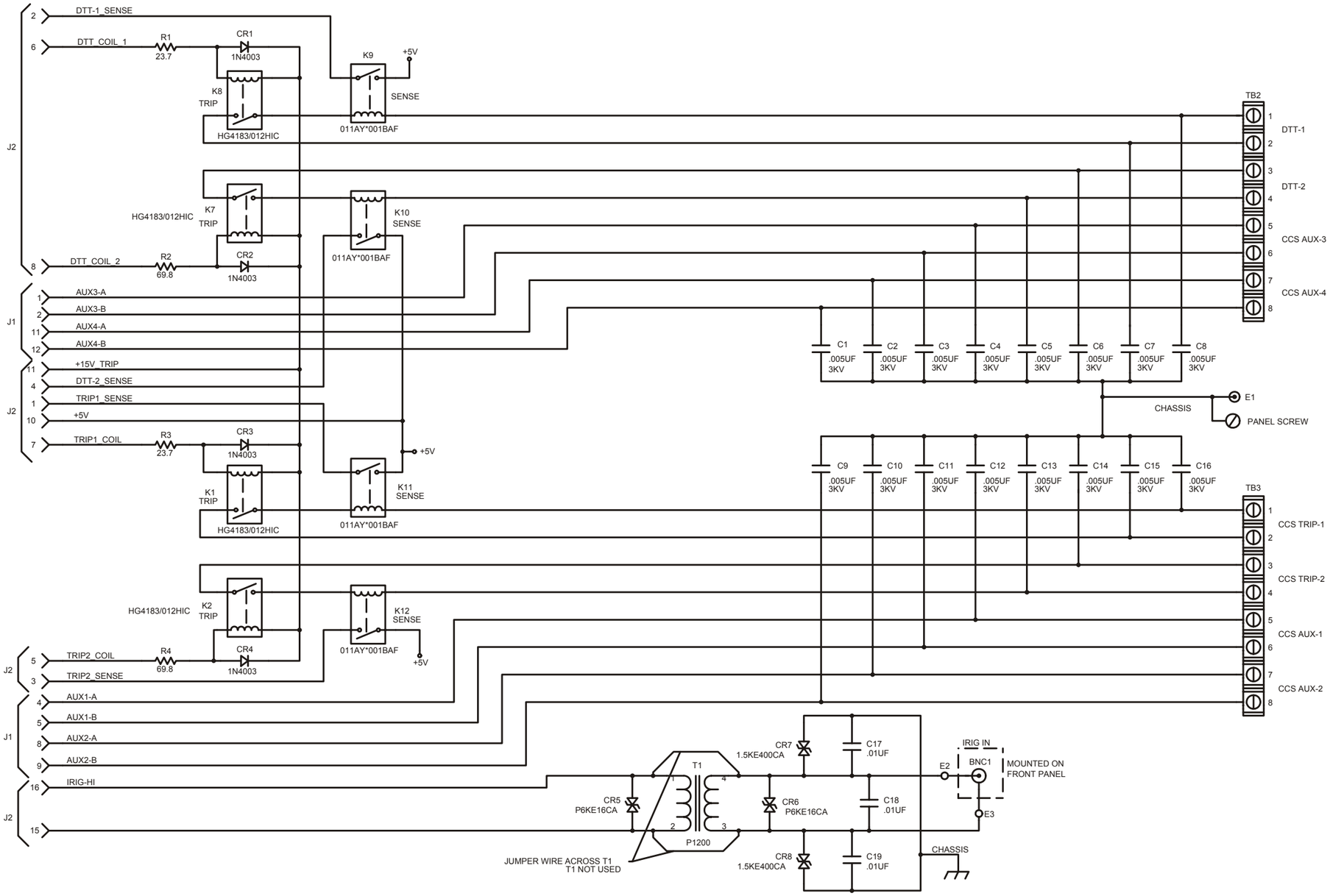


Figure 20- 7. RFL 93B RELAY I/O module, Relay Output board (Assembly No. 106388-3; Schematic No. D-106389, Rev. D) Sheet 3 of 3

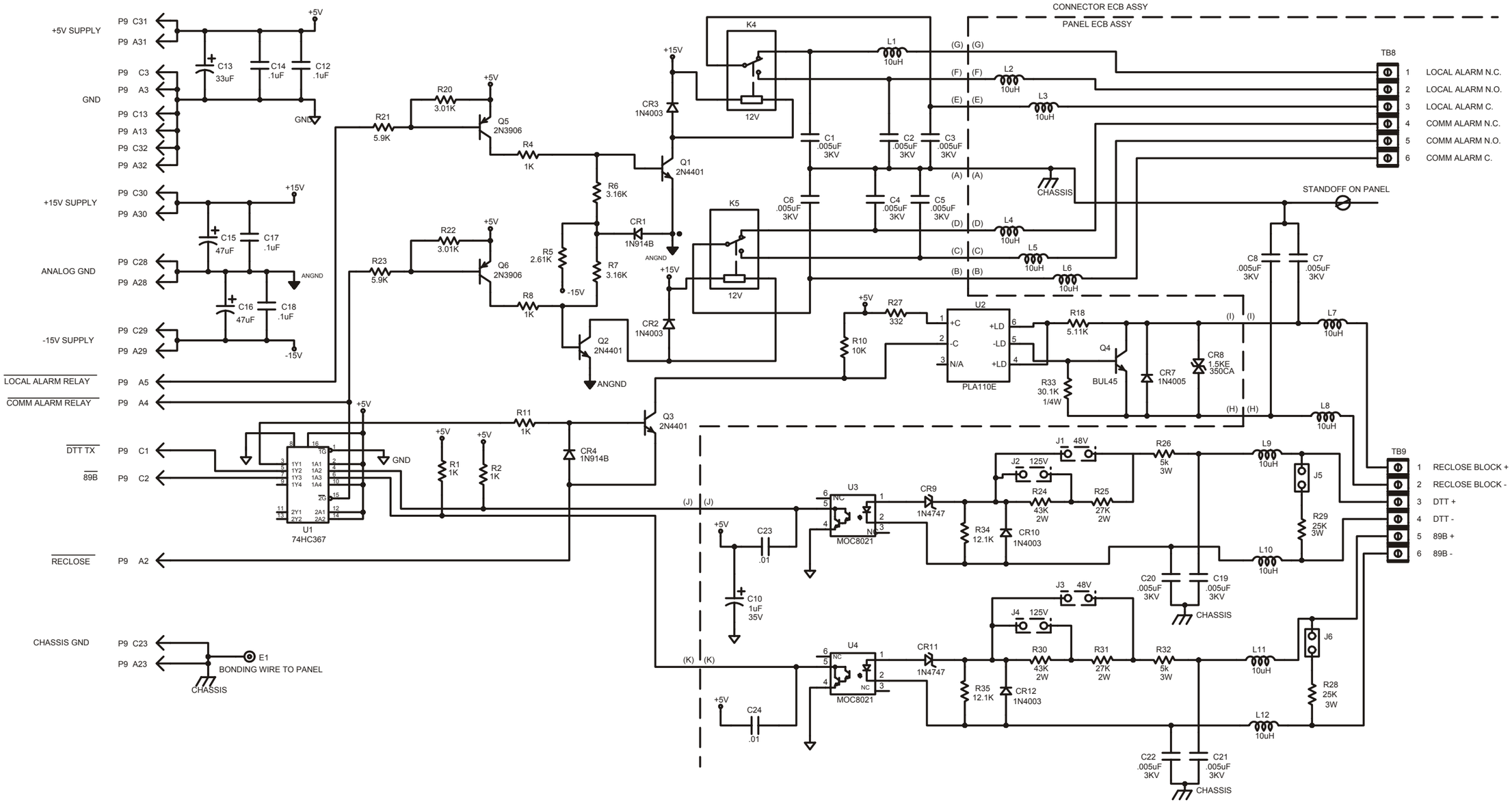


Figure 21- 4. RFL 93 ALARM I/O Input/Output module (Assembly No. 104775-5; Schematic No. 104779-5-D)

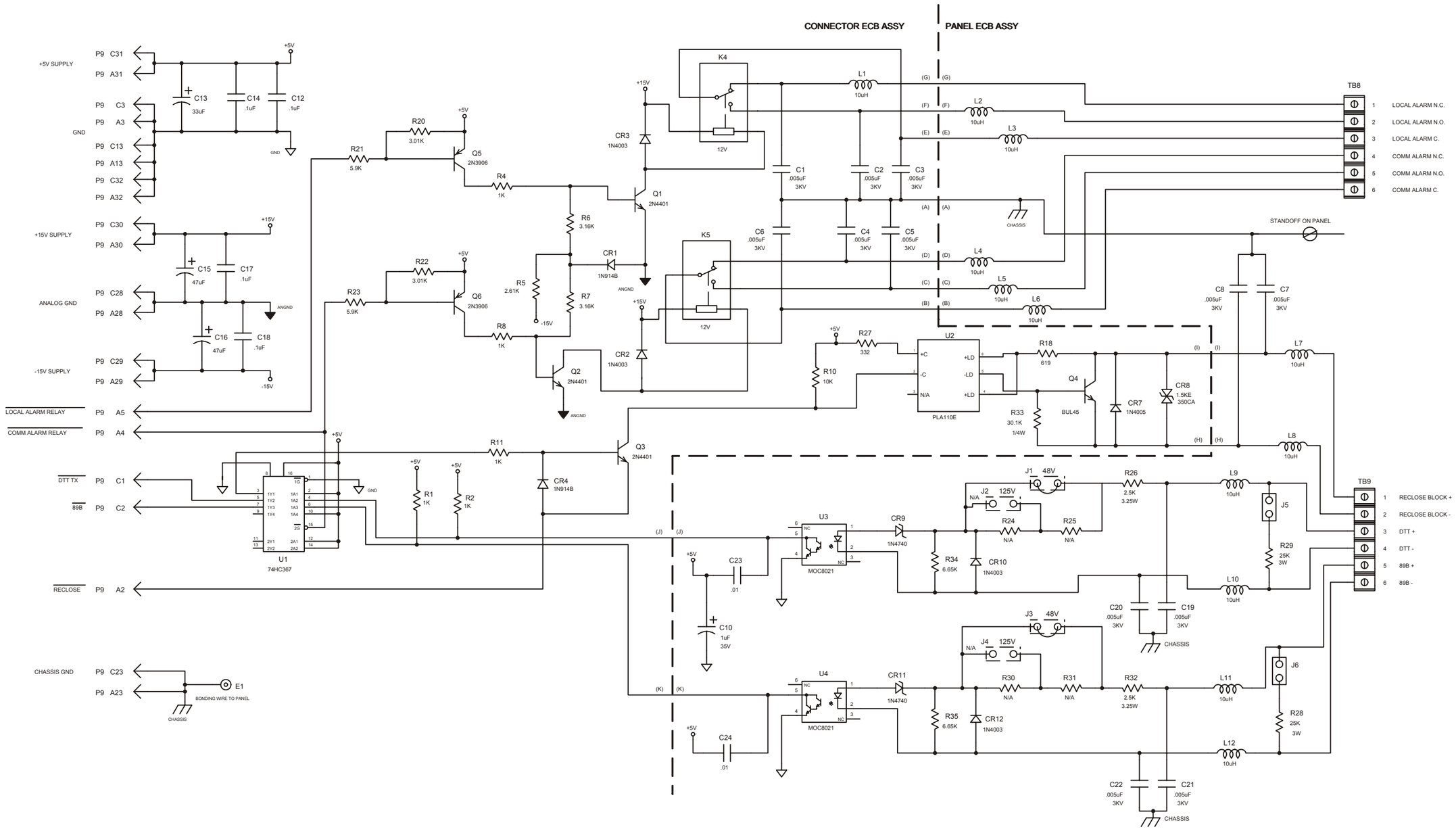


Figure 21-5. RFL 93 Alarm I/O (24V) Input/Output module (Assembly No. 104775-6; Schematic No. D-104779-6-A)

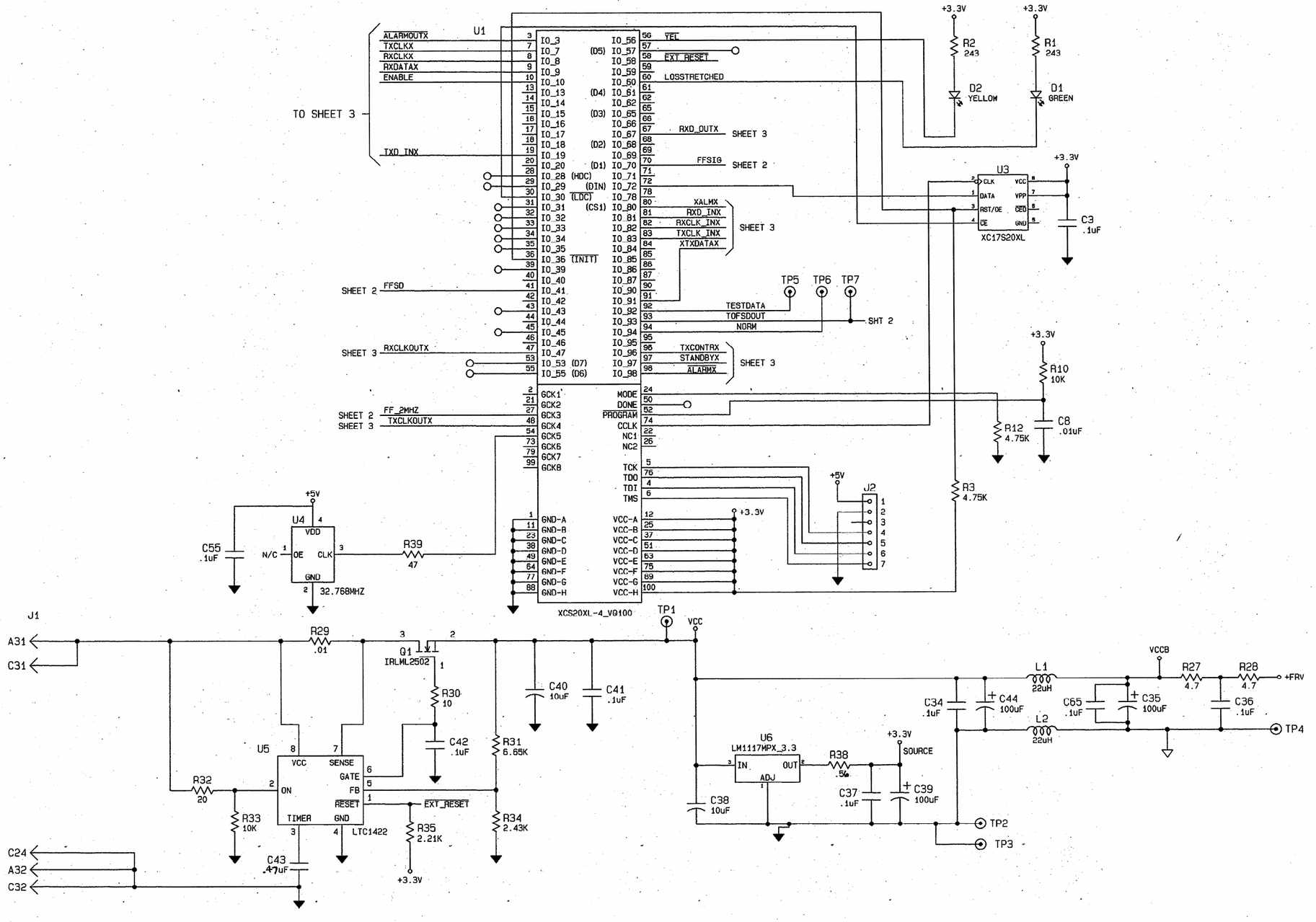


Figure 22-5. RFL 93 Short Haul Fiber Module (Assembly No. 107500; Schematic No. D-107504-D) Sheet 1 of 3

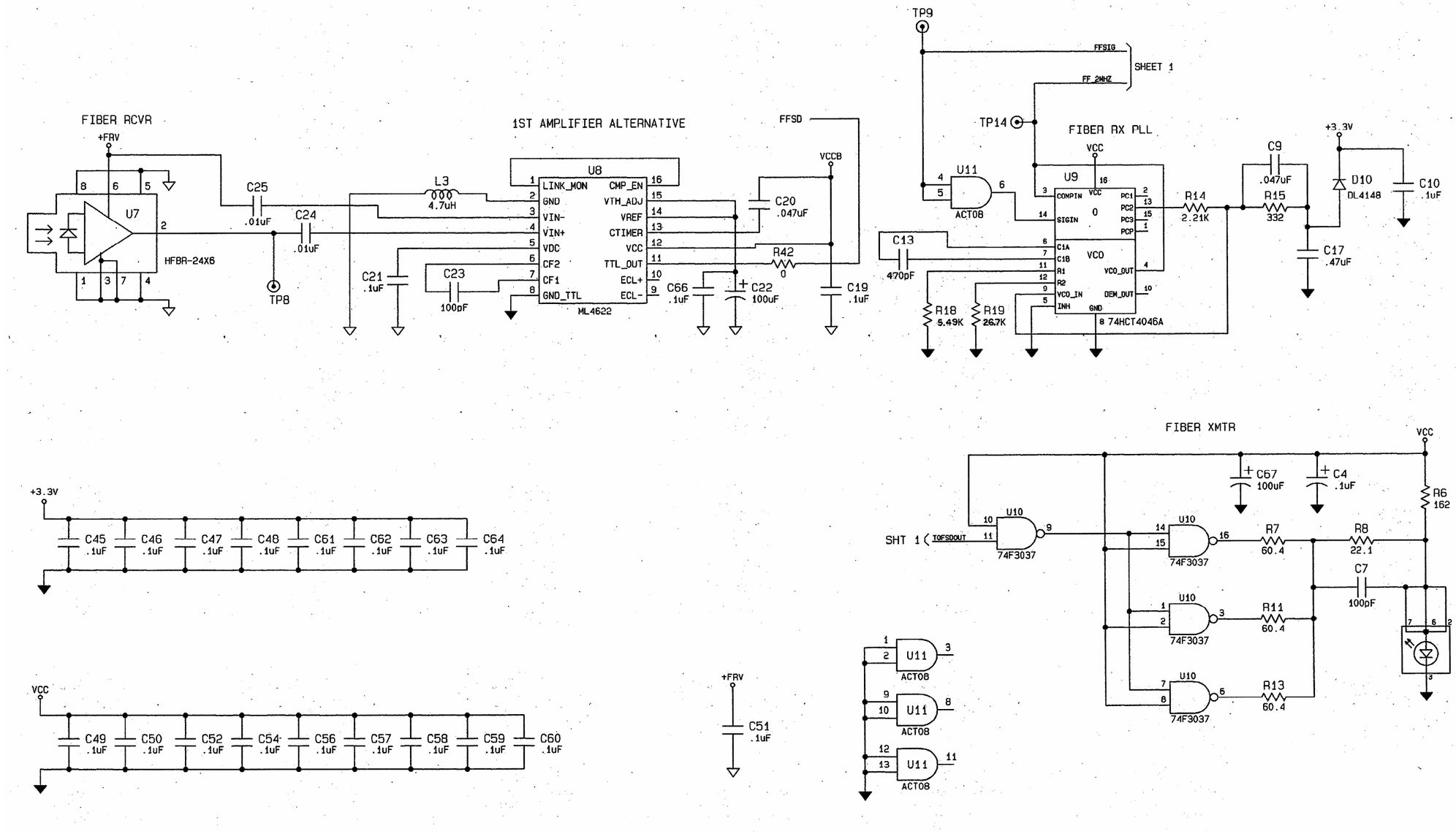


Figure 22- 5. RFL 93 Short Haul Fiber Module
(Assembly No. 107500; Schematic No. D-107504-D) Sheet 2 of 3

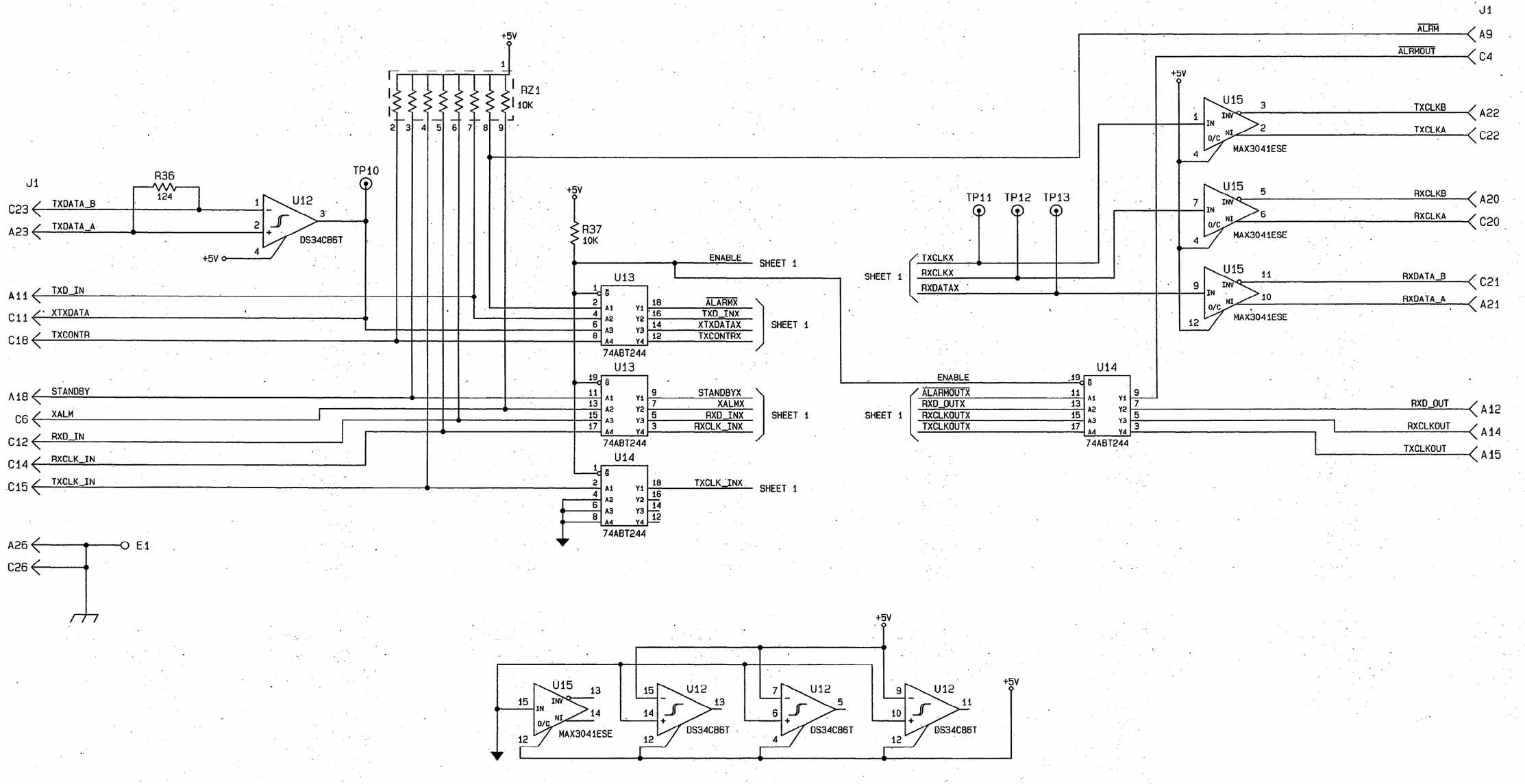


Figure 22- 5. RFL 93 Short Haul Fiber Module (Assembly No. 107500; Schematic No. D-107504-D) Sheet 3 of 3

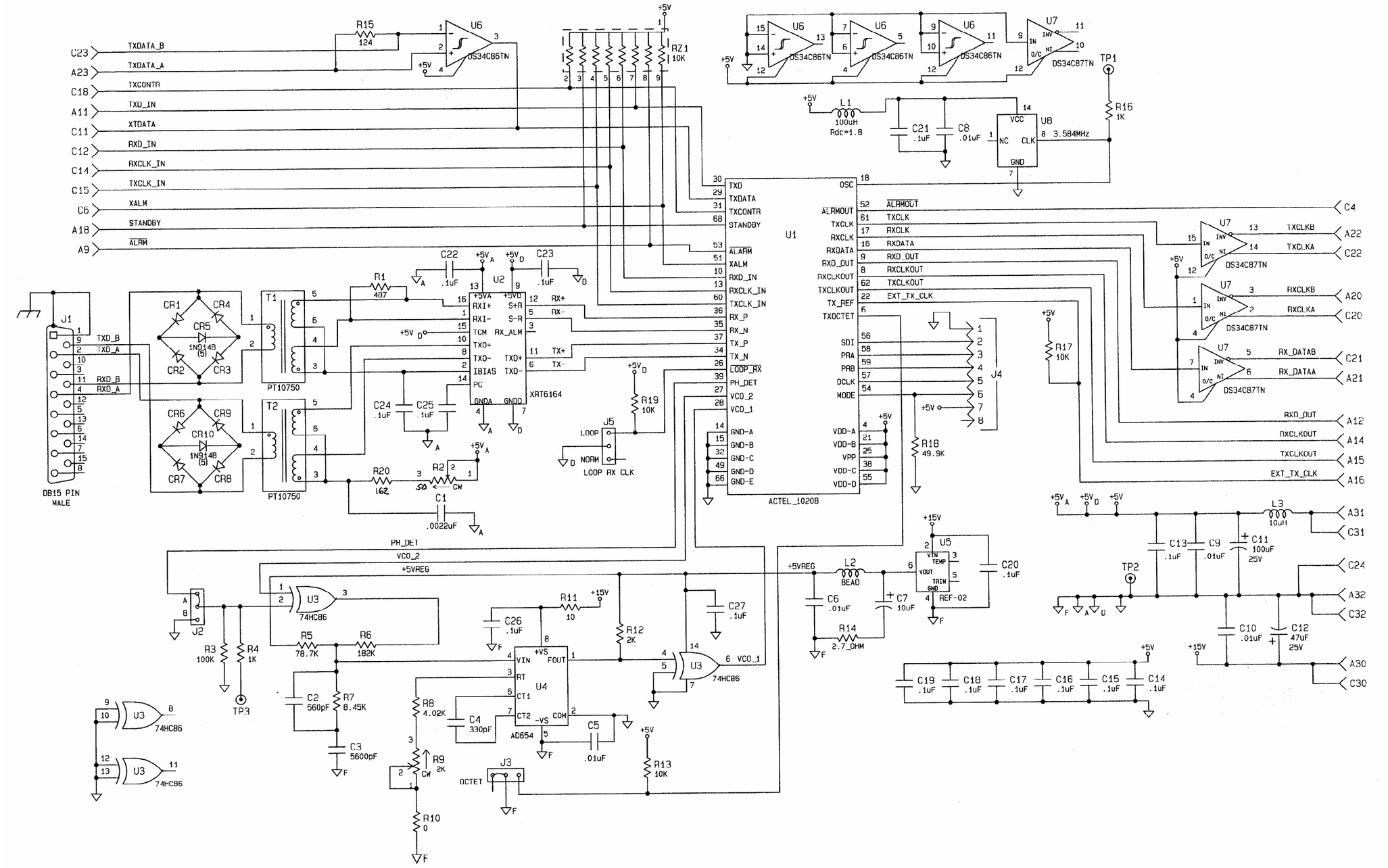


Figure 23-5. RFL 93 G.703 module
(Assembly No. 106730; Drawing No. D-106734-D)

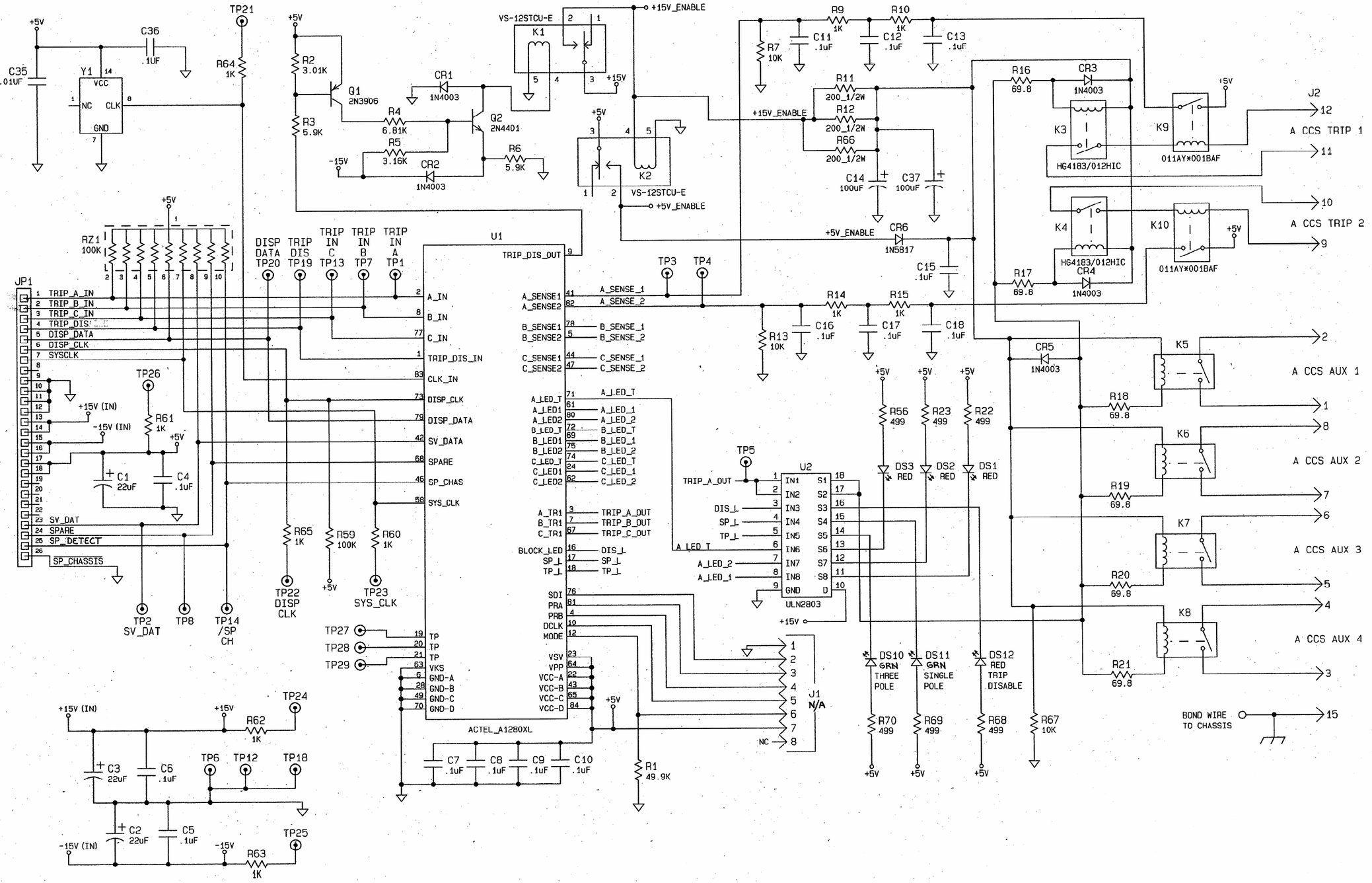


Figure 24- 7. 9300 Single Pole Chassis (Drawing No. D-106714-C) Sheet 1 of 2

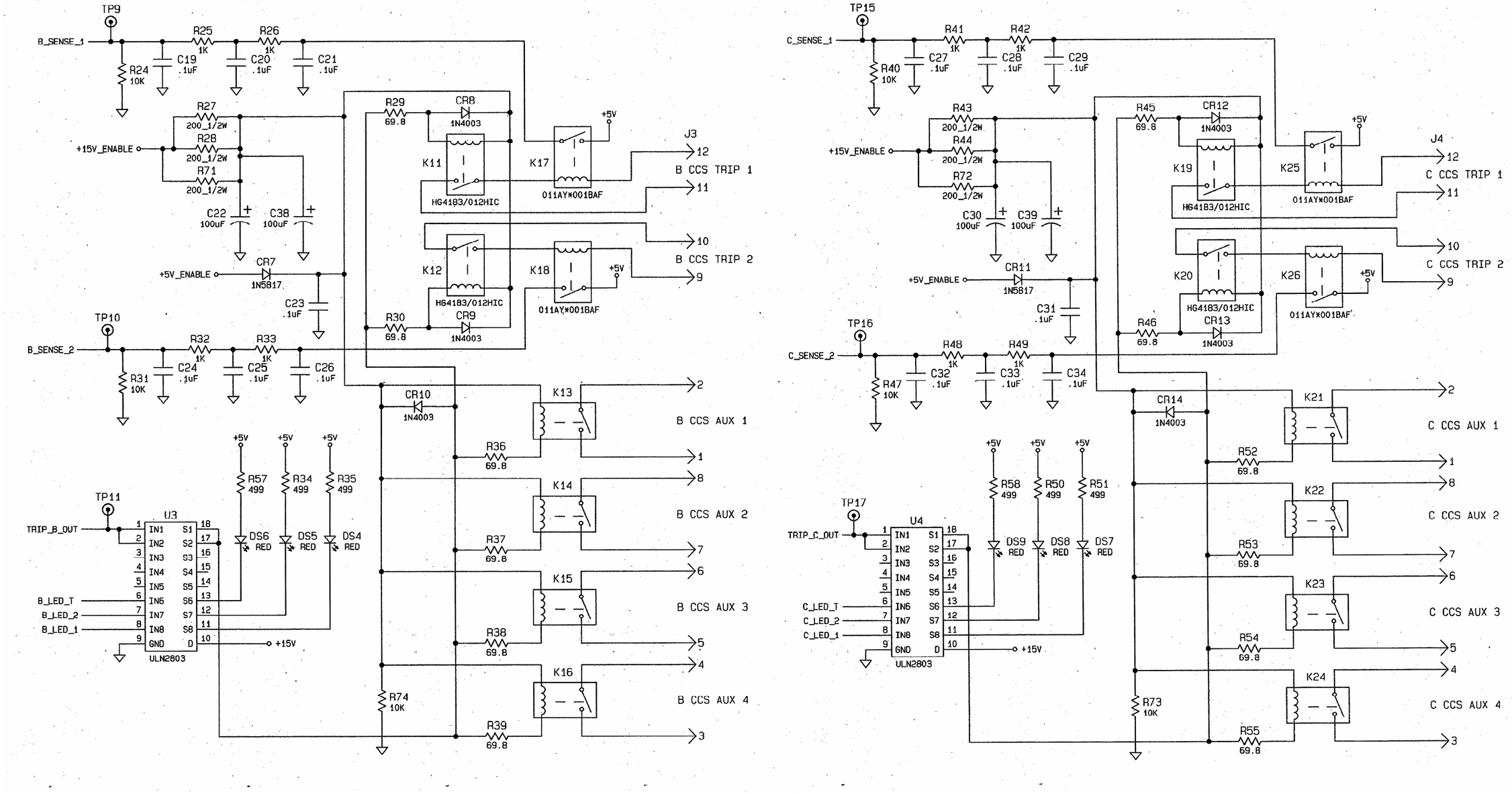
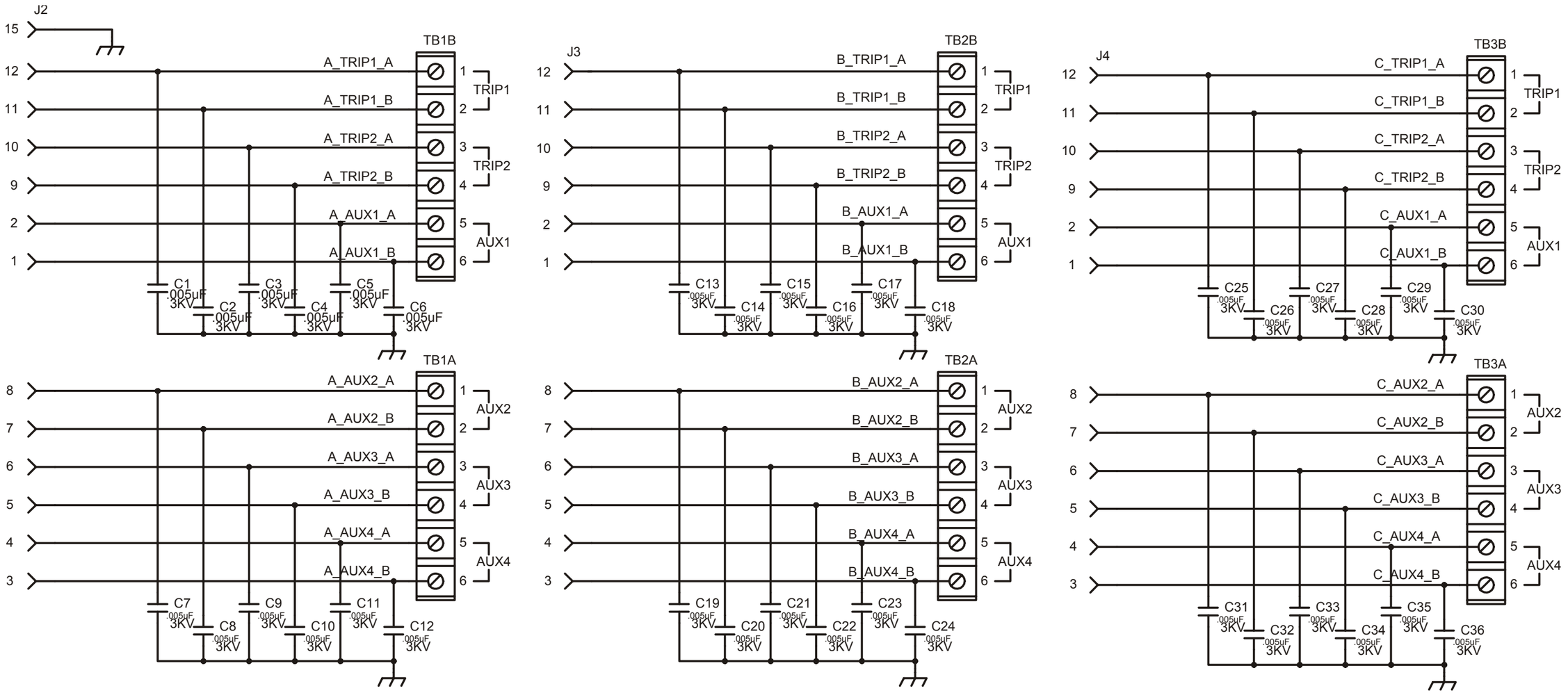


Figure 24- 7. 9300 Single Pole Chassis (Drawing No. D-106714-C) Sheet 2 of 2



PHASE "A"

PHASE "B"

PHASE "C"

Figure 24-9. 9300 Single Pole Chassis, Rear Panel (Drawing No. D-106709-C)

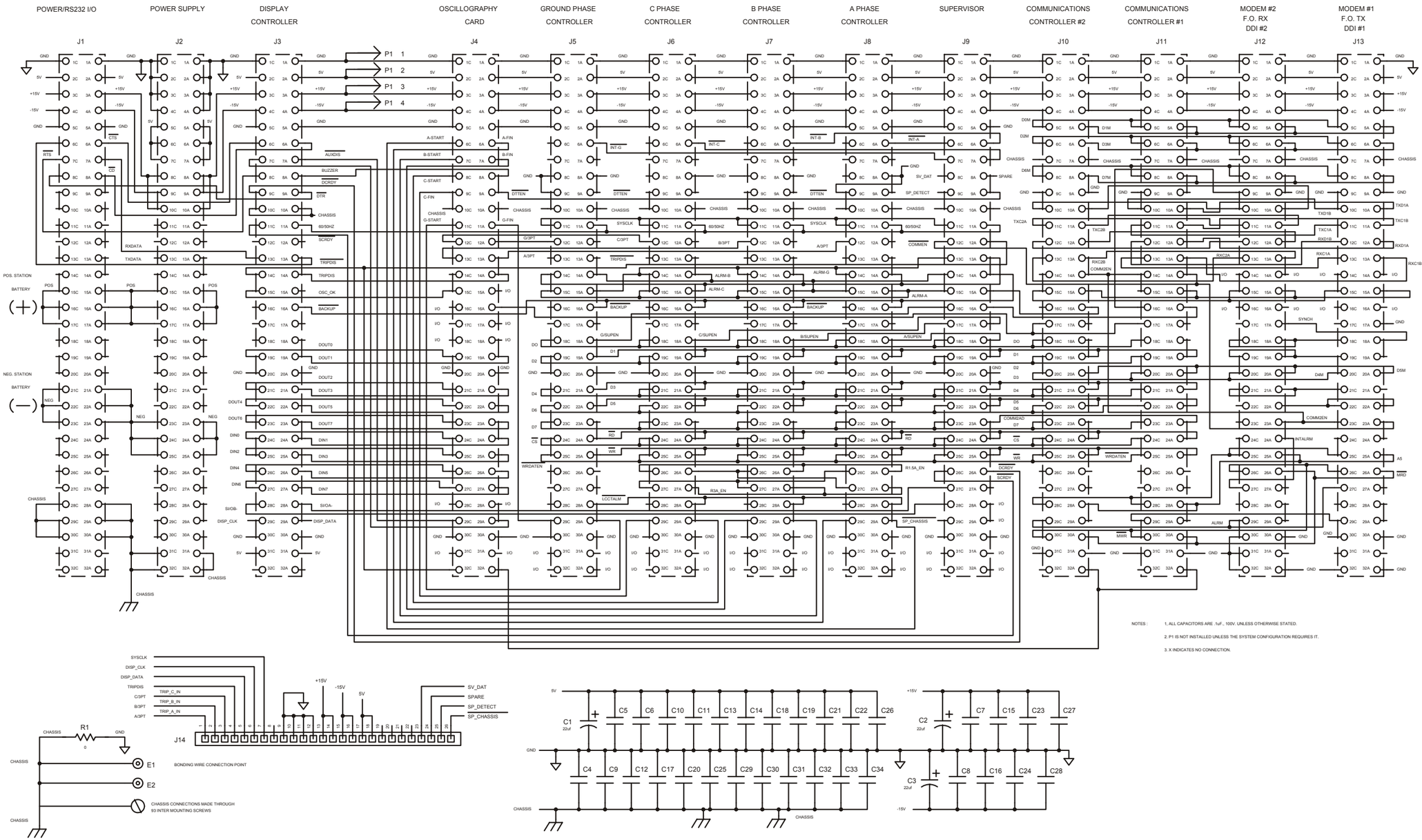


Figure 25- 4. RFL 93 INTER Interconnect Motherboard (Assembly No. 105855; Schematic No. D-103909-1-D)

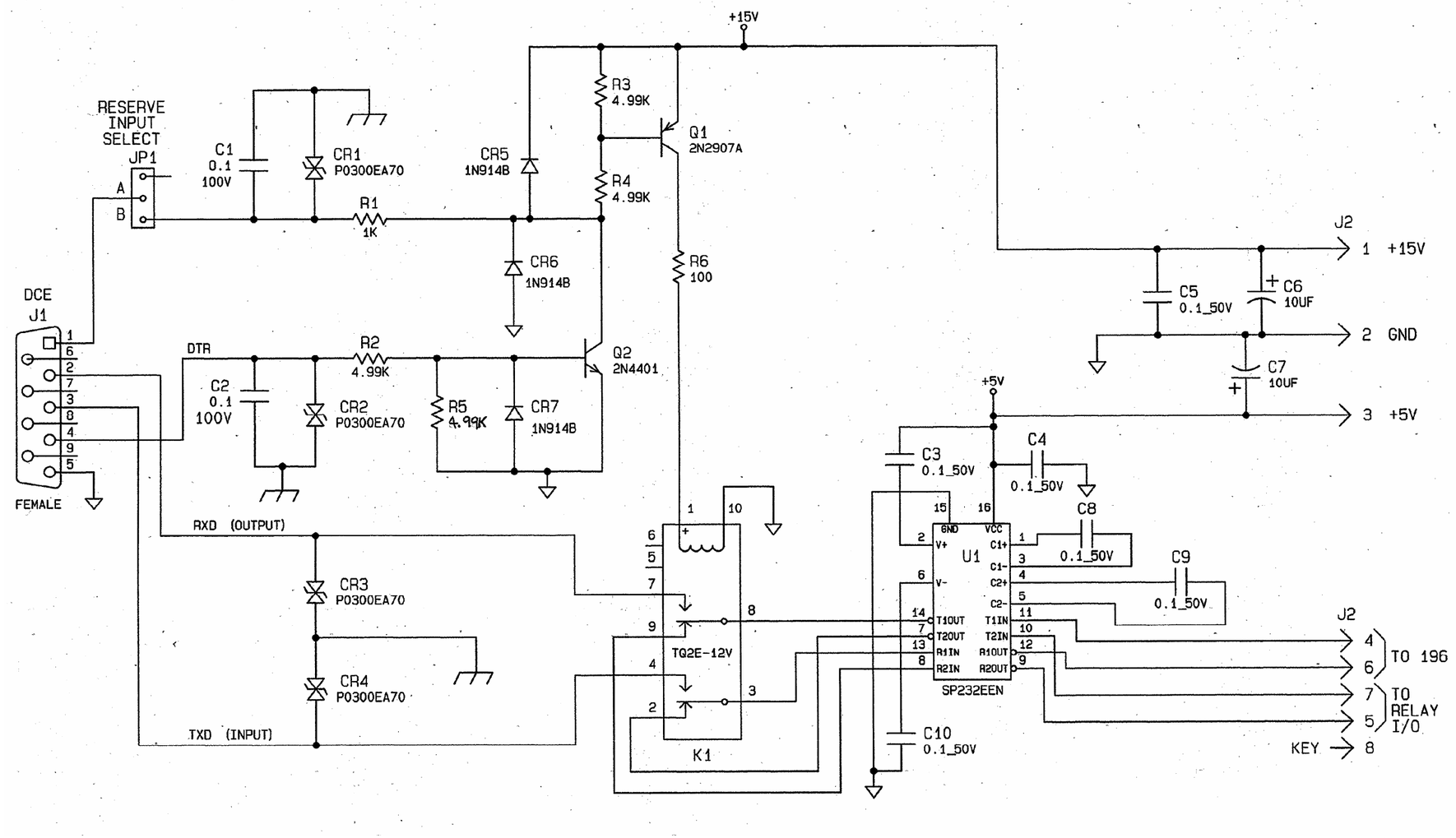


Figure 25- 6. RS-232 Front Panel Interface
(Assembly No. 106755; Schematic No. C-106759-B)

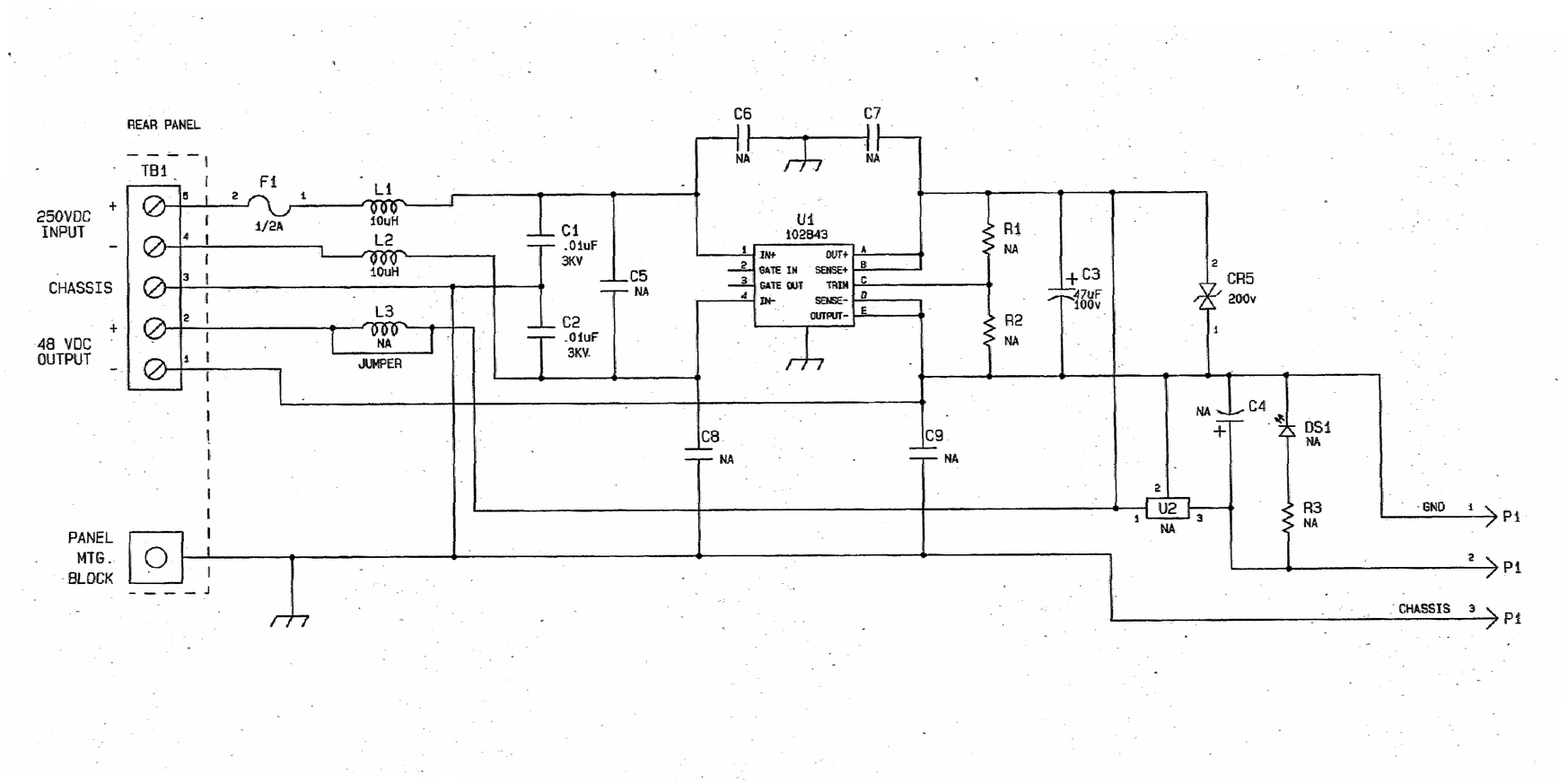


Figure 26-3. Power Converter I/O – 250 VDC for RFL 9300 Charge Comparison System (Assembly No. 106350; Schematic No. C-106354-D)

APPLICATION NOTE

Bias Setting Guidelines and Examples for RFL 9300

Application Note: AN 9300-001

Date: 9/15/2002

Scope

These guidelines and examples are a complement to the RFL 9300 instruction manual, Section 4.

Introduction

Over the ten years that the RFL 9300 has been in service, a Bias of 1.0 Amp or 1.5 Amps has been adopted by many users as a standard setting. The security provided by the RFL 9300's patented Charge Comparison technique has allowed a bias setting of 1.0 amp to be applied to most applications with minimal occurrences of undesired tripping.

There are three factors that are important for determining settings of a protective relay:

- Sensitivity
- Security
- Speed

These factors are inherently contradictory and the setting should therefore be selected so that optimum performance is achieved. Analysis of faults on the RFL 9300 concludes that a bias setting below 2.0 amps may be unnecessarily low, sacrificing security, while providing no advantageous increase in dependability.

For the RFL 9300 it is suggested that the operating threshold is set with a 200% margin in order to achieve high speed operation for the lowest internal fault current that may occur on the protected line. Higher sensitivity is not required nor recommended. Too high sensitivity may compromise security for CT errors during external fault with high fault current.

Minimum recommended setting for PH BIAS is 2.0 A. See Appendix 1.

This Application Note has been developed to provide the RFL 9300 user guidance in the proper application of the RFL 9300 and provide simple instructions to insure proper selection of the bias settings based on minimum available fault current in the system. Following these guidelines will insure that the RFL 9300 will provide the optimum level of security without sacrificing dependability.

Why is Bias Necessary?

The basic theory of a charge or current differential relay is that internal faults have huge differences in current at the two ends of a power line segment and external faults have no difference. In the theoretical world, the trip decision could be solely based on seeing any differential current. In the real world a number of factors make this impractical and selecting where the relays trip requires some consideration.

Any situation that causes the summation of current at the two ends to not equal zero needs to be considered. The differences come from either the protection system or the power system. Any current difference from ideal will be referred to as an error in this Application Note.

Errors from the protection system include unequal CT ratios, CT saturation, analog circuitry errors, resolution or communication errors and software limitations. In current differential systems, errors resulting from imprecise time alignment of the currents can be significant. These errors result from the inability to accurately compensate for channel delays. The patented charge comparison technique of the RFL 9300 is largely immune from these channel delay errors.

Power systems can create current differentials as well. Anytime a portion of the current flows through the CT on one end of a power line and not out through the other an error results. Power system errors can be either transient or steady state in nature. Steady state errors result from tapped loads or line charging current. Transient errors can occur as a result of faults on tapped loads, unequal DC offset due to inrush current, different burdens and capacitance on CT secondary circuits, unequal charging and discharging of CT's immediately following a heavy through load and other conditions.

The bias setting in the relay allows the user to set a trip point in the relay that prevents these errors from causing a loss in security while at the same time ensuring dependability.

The minimum bias setting of 1.0 amp has the following error budget:

- 0.5 amp for current transformer circuit errors and analog to digital conversion errors.
- 0.25 amp for false differential currents caused by net line charging or tapped load.
- 0.25 amp safety factor.

The RFL 9300 will issue a Strong-Feed Trip (SFT) for a value over the bias setting as long as the fault detector requirements described in section 2.7.2 of the RFL 9300 manual are satisfied. The SFT tripping time of the RFL 9300 does not have any delay associated with the magnitude of the differential current vs. the bias setting. Tripping times for differential current of 0.25 amp over the bias will be essentially the same as differentials 4 times the bias setting. The RFL 9300 utilizes an Ultra High-Speed (UHST) trip algorithm that provides faster tripping times based on large peak currents normally associated with internal faults, see section 2.7.5 of the RFL 9300 Instruction Manual.

APPLICATION NOTE

Bias and Bias Control

In most relays, the bias (trip point) is not a fixed value but calculated from a starting point with a curve that increases as current increases. This automatic increase in the trip point allows for errors in the relay system that is proportional to the current level. Such effects include CT ratio mismatch and analog circuitry errors.

The trip point, bias, in the 9300 is calculated based on the following formula:

For sum of currents < 4 amps	trip point = bias setting
For 12 amps > sum of currents > 4 amps	trip point = bias setting + 1/8th Amp
For 20 amps > sum of currents > 12 amps	trip point = bias setting + 1/4th Amp
For sum of currents > 20 amps	trip point = bias setting + 1/4th Amp + (sum of currents -20A)

RFL 9300 Bias Curve

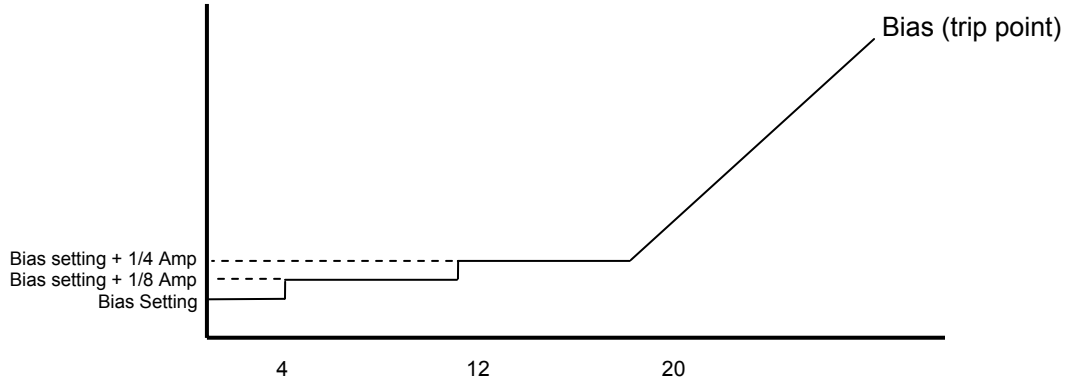


Figure 1: Scalar Sum of Currents

Bias control is a feature that raises the bias point for a certain amount of time after current starts to flow in a line. Typically, when breakers are closed, the line may experience a difference in current as the wire to ground capacitance of the line is charged or transformers / taps on the line are energized. Raising the bias helps add security in these circumstances.

The Bias Control setting raises the phase bias by 1.5 amps when an overhead line is energized. When underground cables are used the charging currents are greater and 3 amps are added to the phase bias. The overhead/underground setting controls this. This increase in bias lasts for the time selected in the bias control setting.

Please refer to section 4.2.3 of the RFL 9300 Instruction Manual for further details on the Bias and Bias Control features of the RFL 9300.

Setting Parameters

For an overhead line, there are generally only two settings that have to be determined, based on minimum internal fault current for the protected line:

PH BIAS	The differential current operating threshold for the phase units
GND BIAS	The differential current operating threshold for the ground system

The phase system will trip for a differential current exceeding:

$$I_{DIFF} \geq PH_BIAS_tot$$

I_{DIFF} is the total differential current from both ends, i.e. I_{local}@0 degrees + I_{remote}@0 degrees, as these currents are ideally in phase for an internal fault

PH_BIAS_tot is the bias as determined by the setting PH BIAS plus any increase according to Figure 2. The resulting PH_BIAS_tot depends on the set PH BIAS and the total scalar sum (restraint) of the currents at both ends, i.e. $|I_{local}| + |I_{remote}|$.

The ground system will trip for a differential current exceeding:

$$I_{DIFF_N} \geq GND_BIAS_tot$$

I_{DIFF_N} is the total 3I0 differential current from both ends, i.e. I_{local}@0 degrees + I_{remote}@0 degrees, as these currents are ideally in phase for an internal fault

GND_BIAS_tot is the bias as determined by the setting GND BIAS plus any increase according to Figure 2. The resulting GND_BIAS_tot depends on the set GND BIAS and the total scalar sum of the 3I0 currents at both ends, i.e. $|I_{local}| + |I_{remote}|$.

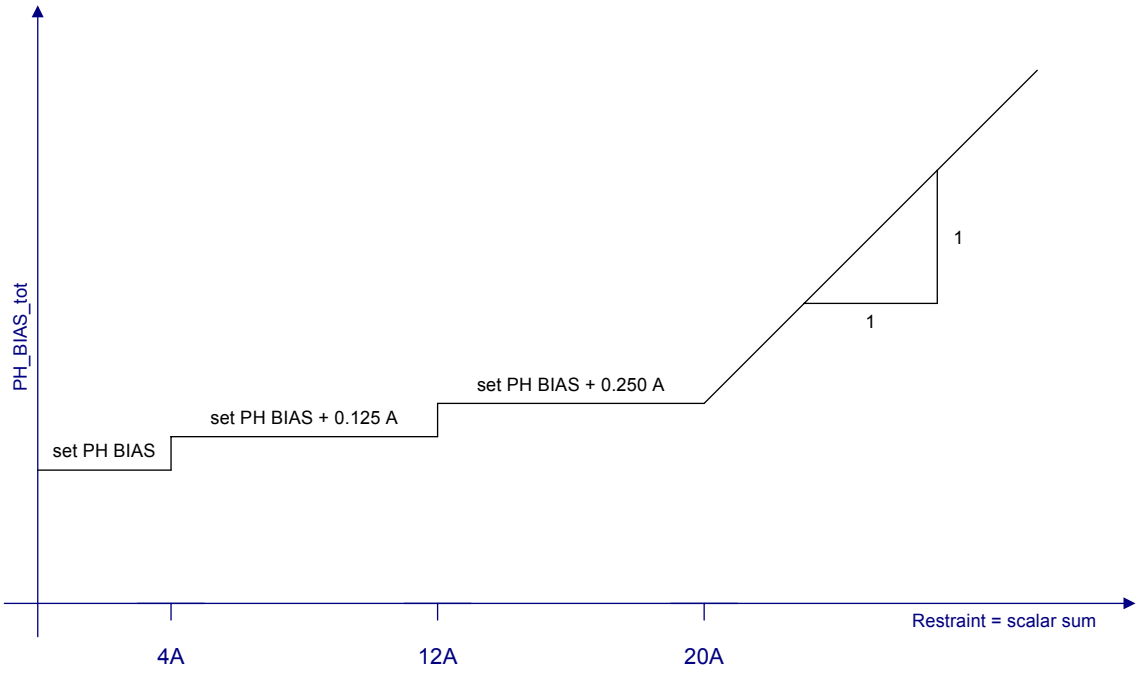


Figure 2: Phase Bias Characteristic

Charging Current

The basic principle of a differential protection scheme is that the sum of the currents entering the protected zone is zero. In case of a transmission line that may not be entirely true because of the capacitive changing current of the line.

The RFL 9300 basic setting guideline accommodates charging current up to 0.25 A secondary. Overhead lines generally have less charging current and does not have to be considered for determining of settings. Cables, however, may have a considerable charging current and the actual value should be checked.

Charging Current Estimation for Overhead Transmission Lines

Charging current can generally be ignored for overhead lines, unless they are very long.

For accurate charging current calculations, the actual capacitive reactance, or susceptance, should be used, less any shunt reactor impedance.

According to Blackburn's "Symmetrical Components for Power Systems Engineering" (ISBN 0-8247-8767-6) a rough approximation of shunt capacitive reactance (primary) for a 69kV or higher transmission line is:

$$X_1^{'} = 0.14 - 0.20 M\Omega mile$$

$$I_c = \frac{V_{line-neutral}}{X_1^{'}} \cdot miles$$

Only if the secondary charging current exceeds 0.25 A should it be taken into account for the BIAS setting.

Charging Current Estimation for Cables

Capacitive charging current is higher for cables than overhead lines and may have to be taken into account. Cable shunt capacitive reactance will be specified for the actual cable, can be taken from a table with typical cable data, calculated or measured.
Charging current can be calculated from given cable characteristics as:

$$I_c = \frac{V_{line-neutral}}{X_1^{'}} \cdot miles$$

For cables longer than 10 miles, BIAS CTRL (BIAS CONTROL) should be enabled, OHVD/UGD (OVERHEAD OR UNDERGROUND CABLE) should be set to UGD and DLAY SEC (TIME DELAY) should be set to 0.1/0.1 (100 ms). These cable settings increase the set bias by 3.0 A during 100 ms following breaker closing in order to override any capacitive inrush current. Please see Sections 4.2.3, 4.2.5 and 4.2.19

Setting Example 1

Line Data

CT ratio = 1200/5 = 240

115 kV, 38 miles

From local terminal, L:
Minimum fault current for internal three phase fault 3600 A primary, 15 A secondary
Assume two phase fault minimum current is 0.866 x three phase, i.e. 13 A secondary
Minimum fault current for internal phase to ground fault 2400 A primary, 10 A secondary

From remote terminal, R:
Minimum fault current for internal three phase fault 2160 A primary, 9 A secondary
Assume two phase fault minimum current is 0.866 x three phase, i.e. 7.8 A secondary
Minimum fault current for internal phase to ground fault 1440 A primary, 6 A secondary

Charging Current Estimation

A rough approximation of capacitive reactance and resulting charging current is:

$$X_1^{'} = 0.14 M\Omega mile$$

$$I_c = \frac{V_{line-neutral}}{X_1^{'}} \cdot miles = \frac{115000}{0.14 \cdot 10^6 \cdot \sqrt{3}} \cdot 38 A_{primary} = 18.02 A_{primary} = 0.08 A_{secondary}$$

Charging current << 0.25 A secondary and does not need to be taken into account for settings.

Phase Bias

The phase bias determines the differential current required for operation according to the formula:

$$I_L + I_R \geq PH_BIAS_tot$$

PH_BIAS_tot is the bias as determined by the setting PH BIAS plus any increase according to Figure 2. The resulting *PH_BIAS_tot* depends on the set PH BIAS and the total scalar sum of the phase currents at both ends, i.e. $|I_{local}| + |I_{remote}|$.

The phase bias should be set low enough to detect a fault on the line with the breaker open in one end, according to (1) below. A check that the selected PH BIAS setting will also detect a fault when both breakers are closed is made in (2) below.

(1) PH BIAS for Single-End-Infeed (Open Breaker)

For single end feed conditions, a trip signal will be issued from a received WCM message and current exceeding the bias.

In the example above, I_R is the lower current, 7.8 A secondary (phase-phase faults). Assuming that this would be the current available also when a line breaker is open (generally, the single-end-infeed current will be higher as the current distribution is different with one line breaker open), we would want the relay to operate for 7.8 A, with sufficient margin.

A margin of a factor of 2 is often used for current differential relaying, i.e. we want to set the threshold so that the relay operates for 50% of 7.8 A = 3.9 A:

The phase bias needs to be set to:

$$0.5 \cdot I_{R\min} > PH_BIAS_{tot} = PH_BIAS_{set}$$

Note that the scalar “sum” in this case is 3.9 A and the total bias (PH_BIAS_{tot}) according to Figure 2 is set bias (PH_BIAS_{set}).

$$PH_BIAS_{set} \le 0.5 \cdot I_{R\min} = 3.9A$$

Set PH BIAS = 3.5 A

(2) PH BIAS for Double-End-Infeed

For internal two phase faults $\angle I_L \cong \angle I_R$

For the example above, I_{Lmin} = 13 A and I_{Rmin} = 7.8 A (phase-phase faults).

A margin of a factor of 2 is recommended, i.e. we want to set the threshold so that the relay operates for 50% of (13A + 7.8A), or 50% of 20.8 A = 10.4 A.

The scalar sum is (13 + 7.8) x 0.5 = 10.4 A, i.e. the bias according to Figure 2 is PH_BIAS_{set} + 0.125 A.

$$0.5 \cdot (I_{L\min} + I_{R\min}) > PH_BIAS_{tot} = PH_BIAS_{set} + 0.125$$
$$PH_BIAS_{set} \le 0.5 \cdot (I_{L\min} + I_{R\min}) - 0.125 = 0.5 \cdot (13 + 7.8) - 0.125 = 10.28A$$

As we can see, the PH BIAS = 3.5 A calculated in (1) above is well below required threshold to ensure operation for double-end-infeed.

Ground Bias

The ground bias determines the differential current required for operation according to the formula:

$$I_L + I_R \ge GND_BIAS_tot$$

GND_BIAS_tot is the bias as determined by the setting GND BIAS plus any increase according to Figure 2. The resulting *GND_BIAS_tot* depends on the set GND BIAS and the total scalar sum of the 3I0 currents at both ends, i.e. $|I_{local}| + |I_{remote}|$.

The ground bias should be set low enough to detect a fault on the line with the breaker open in one end, according to (3) below. A check that the selected GND BIAS setting will also detect a fault when both breakers are closed is made in (4) below.

(3) GND BIAS for Single-End-Infeed (Open Breaker)

For single end feed conditions, a trip signal will be issued from a received WCM message and current exceeding the bias.

In the example above, I_R is the lower current, 6 A secondary. Assuming that this would be the current available also when a line breaker is open (generally, the single-end-infeed current will be higher as the current distribution is different with one line breaker open), we would want the relay to operate for 6 A, with sufficient margin.

A margin of a factor of 2 is often used for current differential relaying, i.e. we want to set the threshold so that the relay operates for 50% of 6 A = 3.0 A:

The ground bias needs to be set to:

$$0.5 \cdot I_{R\min} > GND_BIAS_{tot} = GND_BIAS_{set}$$

Note that the scalar sum in this case is 3.0 A and the bias according to Figure 2 is GND_BIAS_{set}.

$$GND_BIAS_{set} \le 0.5 \cdot I_{R\min} = 0.5 \cdot 6 = 3.0A$$

The setting range for GN BIAS is 1.0 to 2.25 A and the maximum value gives sufficient sensitivity:

Set GND BIAS = 2.25 A.

(4) GND BIAS for Double-End-Infeed

For internal ground faults $\angle 3I0_L \cong \angle 3I0_R$

For the example above, I_{Lmin} = 10 A and I_{Rmin} = 6 A

A margin of a factor of 2 is recommended, i.e. we want to set the threshold so that the relay operates for 50% of (10A + 6A), or 50% of 16A = 8A.

The scalar sum is 8 A and the bias according to Figure 2 is GND_BIAS_{total} = GND_BIAS_{set} + 0.125 A.

$$0.5 \cdot (I_{L\min} + I_{R\min}) > GND_BIAS_{total} = GND_BIAS_{set} + 0.125$$
$$GND_BIAS_{set} \le 0.5 \cdot (I_{L\min} + I_{R\min}) - 0.125 = 0.5 \cdot (10 + 6) - 0.125 = 7.875A$$

The selected GND BIAS = 2.25 A according to (3) above gives good margin for double-end-infeed conditions.

Setting Example 2 – Underground Cable

Line Data

CT ratio = 800/5 = 160

23 kV, 16 miles

From local terminal, L:
Minimum fault current for internal three phase fault 4200 A primary, 26.25 A secondary
Assume two phase fault current is 0.866 x three phase, i.e. 22.73 A secondary
Minimum fault current for internal phase to ground fault 2800 A primary, 17.5 A secondary

From remote terminal, R:
Minimum fault current for internal three phase fault 960 A primary, 6 A secondary
Assume two phase fault current is 0.866 x three phase, i.e. 5.2 A secondary
Minimum fault current for internal phase to ground fault 640 A primary, 4 A secondary

Shunt capacitive reactance = 2,070 ohms-mile

Charging Current Estimation

For cables, the charging current should be checked. Cable shunt capacitive reactance will be specified for the actual cable, can be taken from a table with typical cable data, calculated or measured.

$$X_1^{'} = X_0^{'} = 2070\Omega mile$$

$$I_c = \frac{V_{line-neutral}}{X_1^{'}} \cdot miles = \frac{23000}{2070 \cdot \sqrt{3}} \cdot 16 = 102.6A_{primary} = 0.64A_{\text{sec}ondary}$$

For this example, the charging current exceeds 0.25 A and the margin to the minimum setting should then be increased by 0.5 A. Therefore, the minimum recommended setting for GND BIAS is 1.5 A (1.0 + 0.5) and the minimum recommended setting for PH BIAS is 2.5 A (2.0 A according to Appendix 1 plus 0.5 A).

For cables longer than 10 miles, BIAS CTRL (BIAS CONTROL) should be enabled, OHVD/UGD (OVERHEAD OR UNDERGROUND CABLE) should be set to UGD and DLAY SEC (TIME DELAY) should be set to 0.1/0.1 (100 ms). These cable settings increase the set bias by 3.0 A during 100 ms following breaker closing in order to override any capacitive inrush current. Please see Sections 4.2.3, 4.2.5 and 4.2.19 of the RFL 9300 Instruction Manual.

The selected settings below should be checked so that sensitivity is sufficient during the 100 ms interval following breaker closing, i.e. when the set bias is increased by 3.0 A.

Phase Bias

The phase bias determines the differential current required for operation according to the formula:

$$I_L + I_R \geq PH_BIAS_tot$$

PH_BIAS_tot is the bias as determined by the setting PH BIAS plus any increase according to Figure 2. The resulting PH_BIAS_tot depends on the set PH BIAS and the total scalar sum of the phase currents at both ends, i.e. $|I_{local}| + |I_{remote}|$ plus the UGD bias increase of 3.0 A following breaker closing.

PH BIAS for Double-End-Infeed

In this example, it is assumed that double-end infeed will exist for all internal fault conditions.

For internal two phase faults $\angle I_L \cong \angle I_R$

For the example above, I_{Lmin} = 22.7 A and I_{Rmin} = 5.2 A

A margin of a factor of 2 is recommended, i.e. we want to set the threshold so that the relay operates for 50% of (22.7 + 5.2) A, or 50% of 27.9 = 14.0 A.

The scalar sum is (22.7 + 5.2) x 0.5 = 14.0 A and the bias according to Figure 2 is PH_BIAS_{set} + 0.250 A plus the 3.0 A increase following breaker closing.

$$0.5 \cdot (I_{L\min} + I_{R\min}) > PH_BIAS_{tot} = PH_BIAS_{set} + 0.250 + 3.0$$

$$PH_BIAS_{set} \leq 0.5 \cdot (I_{L\min} + I_{R\min}) - 0.250 - 3.0 = 0.5 \cdot (22.7 + 5.2) - 0.250 - 3.0 = 10.75A$$

The PH BIAS setting range is 1.0 – 8.0 A and the maximum setting gives sufficient sensitivity:

Set PH BIAS = 8.0 A.

The determined setting gives good margin for the capacitive charging current, 0.63A, estimated above.

Ground Bias

The ground bias determines the differential current required for operation according to the formula:

$$I_L + I_R \geq GND_BIAS_tot$$

GND_BIAS_tot is the bias as determined by the setting GND BIAS plus any increase according to Figure 2. The resulting GND_BIAS_tot depends on the set GND BIAS and the total scalar sum of the 3I0 currents at both ends, i.e. $|I_{local}| + |I_{remote}|$ plus the UGD bias increase of 3.0 A following breaker closing.

GND BIAS for Double-End-Infeed

For this example, double-end infeed will be present for all internal fault conditions.

For internal ground faults $\angle 3I0_L \cong \angle 3I0_R$

For the example above, I_{Lmin} = 17.5 A and I_{Rmin} = 4 A

A margin of a factor of 2 is recommended, i.e. we want to set the threshold so that the relay operates for 50% of (17.5A + 4A), or 50% of 21.5A = 10.7 A.

The scalar sum is 10.7 A and the bias according to Figure 2 is GND_BIAS_{tot} = GND_BIAS_{set} + 0.125 A plus 3.0 A following breaker closing.

$$0.5 \cdot (I_{L\min} + I_{R\min}) > GND_BIAS_{total} = GND_BIAS_{set} + 0.125 + 3.0$$

$$GND_BIAS_{set} \le 0.5 \cdot (I_{L\min} + I_{R\min}) - 0.125 - 0.3 = 0.5 \cdot (17.5 + 4) - 0.125 - 3.0 = 7.5A$$

The GND BIAS setting range is 1.0 – 2.25 A and the maximum setting provides sufficient sensitivity:

Set GND BIAS = 2.25 A.

The determined setting gives good margin for the capacitive charging current, 0.63A, estimated above.

Setting Example 3 – Tapped Load

Considerations for tapped line applications are given in Section 3.14 of the RFL 9300 Instruction Manual. The following is an example for a tapped line with a delta-wye transformer at the tap.

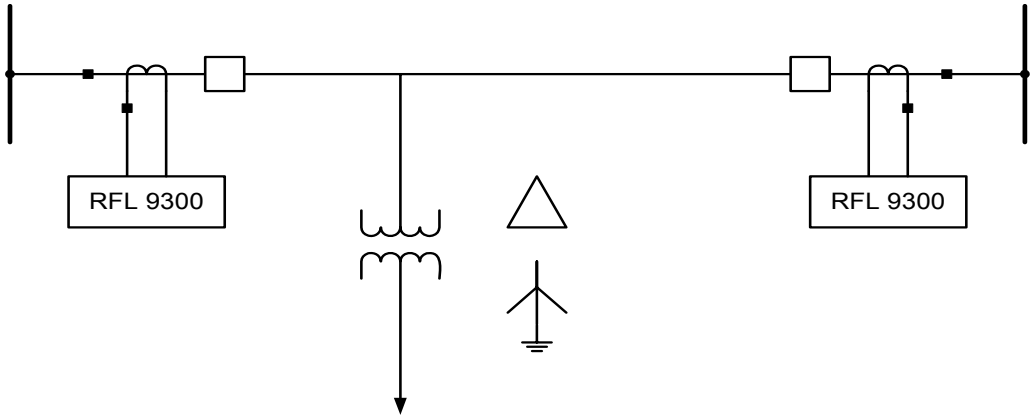


Figure 3: Tapped Load

Line Data

CT ratio = 2000/5 = 400
VT ratio = 230000/115 = 2000

ZT = transformer impedance = 10% on a 20 MVA base

$$ZT(ohms) = ZT(pu) \cdot \frac{kV^2}{MVA} = 0.10 \cdot \frac{230^2}{20} = 264.5 \text{ ohms, primary}$$

From local terminal, L:
Minimum fault current for internal three phase fault 6000 A primary, 15 A secondary
Assume two phase fault current 0.866 x three phase, i.e. 13.0 A secondary
Minimum fault current for internal phase to ground fault 4000 A primary, 10 A secondary

From remote terminal, R:
Minimum fault current for internal three phase fault 3600 A primary, 9 A secondary
Assume two phase fault current 0.866 x three phase, i.e. 7.8 A secondary
Minimum fault current for internal phase to ground fault 2400 A primary, 6 A secondary

Low Side, External, Faults

The RFL 9300 should not operate for a three phase fault on the load side of the transformer. Ignoring the impedance between the source and the high side of the transformer, the three-phase fault current for a low-side fault is:

$$I_{3\Phi} = \frac{V_{line-neutal}}{Z_T} A_{primary} = \frac{230000}{264.5 \cdot \sqrt{3}} = 502 A_{primary} = 1.26 AA_{\text{sec}ondary}$$

It is recommended to select PH BIAS larger than 3 times low-side fault current:

$$PH_BIAS > 3 \cdot 1.26 = 3.78A$$

Ground faults on the low side do not produce any zero sequence current to the relays and therefore do not need to be considered for the GND BIAS setting.

Internal Faults

PH BIAS should be set sensitive enough to detect all internal faults. Applying the same margin of a factor of 2 as discussed in Example 1, the PH BIAS setting should be:

$$0.5 \cdot (I_{L\min} + I_{R\min}) > PH_BIAS_{tot} = PH_BIAS_{set} + 0.125$$
$$PH_BIAS_{set} \le 0.5 \cdot (I_{L\min} + I_{R\min}) - 0.125 = 0.5 \cdot (13 + 7.8) - 0.125 = 10.27A$$

The setting range is 1.0 – 8.0 A and the condition for tapped load above was PH BIAS > 3.78 A. The maximum setting 8.0 A fulfills both the internal fault sensitivity requirement and the external fault stability requirement.

Set PH BIAS = 8.0 A

GND BIAS is calculated in the same way but based on minimum ground fault current:

$$0.5 \cdot (I_{L\min} + I_{R\min}) > GND_BIAS_{tot} = GND_BIAS_{set} + 0.125$$
$$PH_BIAS_{set} \le 0.5 \cdot (I_{L\min} + I_{R\min}) - 0.125 = 0.5 \cdot (10 + 6) - 0.125 = 7.8A$$

The setting range is 1.0 – 2.25 A and no additional condition is required for a delta-wye transformer tap. The maximum setting 2.25 A fulfills the internal fault sensitivity requirement.

Set GND BIAS = 2.25 A.

Appendix 1

Minimum PH BIAS setting

As can be seen from Figure 2, the RFL 9300 is very sensitive for currents up to 20 A scalar sum. This means that an external fault with 10 A fault current and maximum combined ct error (10% in opposite direction at the two line ends) could cause a differential current of 2 A. For higher fault currents, the restraint bias increases proportionally so that stability is secured.

The minimum setting for PH BIAS recommended is 2.0 A.

Please contact RFL Customer Service at 973.334.3100 extension 226 or email at customerservice@rflelect.com for any applications that may require a phase bias setting of less than 2.0 amps.