INSTRUCTION MANUAL

RFL 6710
Frequency-Shift Audio-Tone
Protective Relaying System

NOTICE

Publication Number MC 6710
Printed In U.S.A.
Revised November 16, 1992

RFL Electronics Inc.

WARRANTY

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RFL Electronics Inc.
Boonton, New Jersey USA

RFL Electronics Inc.

ERRATA SHEET

RFL 6710 Instruction Manual

Some minor errors have been found in the RFL 6710 manual. Please mark the following pages of your manual as indicated; these changes will be incorporated into the manual at the next printing.

Page 14:

In Table 1.3, the wrong suffix number was called out for the guard receiver resistor network required for 3 dB of boost. In the table, change the first "-6" in the "GUARD RECEIVER" column to "-5".

Page 44:

In the parts list for the Model 67 MBB LOGIC card, the part number for IC13 has been changed because the manufacturer has stopped making the listed part. Replacement information for IC13 is now as follows:

Circuit Symbol	Description	Part Number
IC13	MOS quad analog switch,14-pin DIP,Motorola MC14066BCP or equiv.	0615 246

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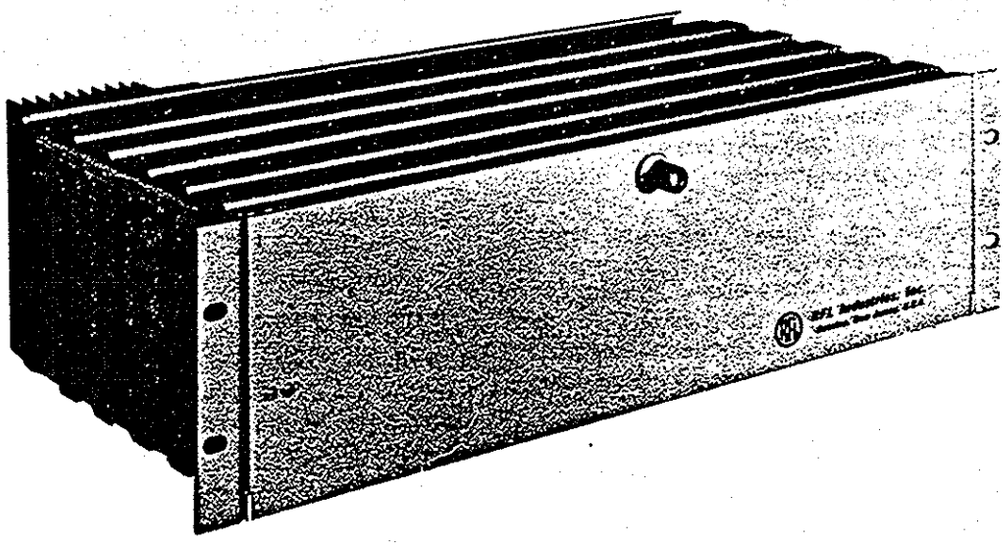


RFL Series 6710 Frequency-Shift Audio-Tone Protective Relaying System.

Introduction

The Series 6710 Protective-Relaying System has been designed to provide a modular-building-block approach to the assembly of protective-relaying systems. It transmits a single guard or trip command from one point to another over a voice-frequency communication system. The equipment can be arranged to form many different systems, so that security, dependability, speed of response, or some preferred combination of all three can be emphasized at the system designer's choice. The equipment exhibits a high degree of dependability. It can detect a valid trip during an instantaneous drop in signal level of as much as 20 dB, while, at the same time, it maintains a relatively high degree of security.

The Series 6710 System is a completely self-contained, solid-state system using frequency-shift keying of its carrier. It can be used directly over voice-frequency communication circuits, and its carrier may be frequency translated to powerline-carrier frequencies, including single-sideband systems. Typical dependability and security are shown in Figures 1.1 and 1.2.

SPECIFICATIONS

GENERAL

Primary Supply Voltage
21-28, 42-56, or 104-140 Vdc. Power-input circuit is floating. Demand is less than 40 watts.

Operating Temperature Range
−30 to 60°C.

Recommended Signal Frequencies
See Table 1.1

Input and Output Communication Circuits
Balanced 600 ohms, field-selectable for either two-wire or four-wire operation.

Operating Time
With transmitter and receiver connected back-to-back, and without an output relay, operating time is 12 ms with 340-Hz channel spacing. An 8-ms response time similarly is available for increased dependability with reduced security. Faster operating times are available by increasing the channel spacing.

Security and Dependability
See Figures, 1.1 and 1.2, for a typical system. Data shown were taken when using a signal-ratio network requiring at least 12 dB between levels of trip and guard signals, with a 20-dB dynamic range, and with the pre-trip timer at 4.5 ms. Security could be increased significantly if dependability, dynamic range, or speed were reduced. Dual-channel operation will improve security.

Trip Input
Twenty to 30 mA into a floating optical isolator. Power may be taken from the 24-, 48-, or 129-Vdc primary-power source

Trip Output
A choice of two different output relays is available: (a) A spring relay with 2.5-ms response time, one set of Form-C contacts rated at 30 amperes for 100 ms, 6 amperes continuous, and with dielectric strength of 2000 Vrms from contacts to coil.

(b) An auxiliary relay card with capacity for two Model 67AR-(XXX) relays with a response time of 2 ms. These are driven by the spring relays described in (a). Contact rating is 30 amperes for 100 ms, 3 amperes continuous. Available contacts are four Form-A, three Form-A, one Form-B, or two Form-A and two Form-B.

(c) Open-collector transistor output provides for use of other relays.

Guard, Low-Signal and Alarm Outputs
Optional relays provide an output signal which is the transfer of a set of Form-C contacts. Breaking capacity for a resistive load is three amperes, 250 Vac maximum. The alarm relay is normally energized and it de-energizes after 100 ms if either an abnormal signal condition or a power failure is sensed. All relays have a dielectric strength of 2000 Vrms between contacts and coil. Open-collector transistor outputs provide for use of other relays.

Interface Dielectric Strength
Trip input, trip-relay output, and audio-signal lines are isolated from ground and from all other circuits. Breakdown is 1500 Vrms, 50-60 Hz, or 2200 Vdc and 2500 volts at 1.5 MHz, in accordance with ANSI/IEEE C37.90-1978.

Dimensions and Weight
The equipment is fully contained in an RFL Model 68 rack-mounted chassis conforming to EIA specifications. It is 5¼" high, 12½" deep, and the panel is 19" wide (134 x 315 x 482 mm). Weight is less than 15 lbs., (6.8 kg).

TRANSMITTER

Output-Frequency Tolerance
±0.25% using an active-filter oscillator.

Trip-Boost Level and Duration
Adjustable with plug-in networks with a choice of levels from 0 to 6 dB, and a choice of period to 200 ms. 70 ms is standard.

Output Level
Adjustable from −30 to 10 dBm for four-wire operation, and from −30 to 5 dBm for two-wire operation.

Harmonic Output
All harmonics are more than 40 dB below the fundamental.

Amplitude Stability
±1 dB.

Flasher
An optional flasher keys the transmitter rapidly between guard and trip at a 20-Hz rate when the trip input is energized so that each signal continues alternately for 25 ms.

Mute Relay
This optional relay, used to switch off other signals when the transmitter has tripped, has two sets of Form-C mercury-wetted contacts. Two relays are provided on the card.

Output Filter
This optional filter for the transmitter reduces all harmonics to more than 60 dB below the fundamental, and it increases clear-channel trip time by not more than 3 ms when using 340-Hz channel spacing. Its balanced output circuit has a nominal source impedance of 600 ohms within the channel.

RECEIVER

Sensitivity
Adjustable from −40 to 0 dBm.

Bandwidth
See Figure 1.3

Dynamic Range
A 20-dB dynamic range is standard. A 30-dB range, optionally available, provides greater dependability with reduced security.

DESCRIPTION

The Series 6710 System is an audio-tone, frequency-shift-keyed, self-contained, protective-relaying system designed to employ solid-state circuits. Although basically a single-channel system, two transmitters may be used to provide a system in which a trip command moves one transmitter upward in frequency while the other is shifted downward to create a system which offers protection from undesired frequency translations.

The system is useful for permissive-transfer trip, direct-transfer trip, directional comparison (blocking or unblocking), and for phase-comparison relaying. It provides excellent security against false trips, dependability, and good response time, as shown in Figures 1.1, 1.2 and 1.3. Usual operating frequencies are between 1 and 3.3 kHz, although the system itself may be used up to 10 kHz if the communication link has the frequency-response capability. The communication medium may be a telephone line, microwave voice channel, single-sideband (SSB) powerline-carrier system, or microwave baseband with suitable translator. Either in-band noise monitoring or out-of-band techniques may be used with the Series 6710 System.

Used as a single channel, the Series 6710 is designed for directional-comparison blocking (DCB), and for permissive-transfer tripping (PTT) applications. Two channels can be combined, however, in a dual-channel system, using either upward or downward shifts in carrier frequency as a trip signal, for direct transfer tripping (DTT). The system is designed primarily as an in-band noise-monitoring channel. Out-of-band concepts, however, may be applied through the use of a separate 300-1000-Hz receiver, if desired.

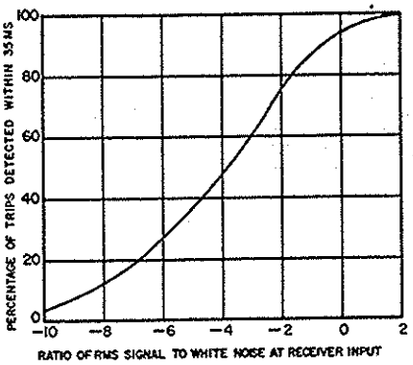


Figure 1.1. Typical dependability with 340-Hz channel spacing. Noise bandwidth was 30-3000 Hz, and noise was gated on when the transmitter was shifted from guard to trip. Trip-signal period was 35 ms, and center frequency of the channel was 1615 Hz.

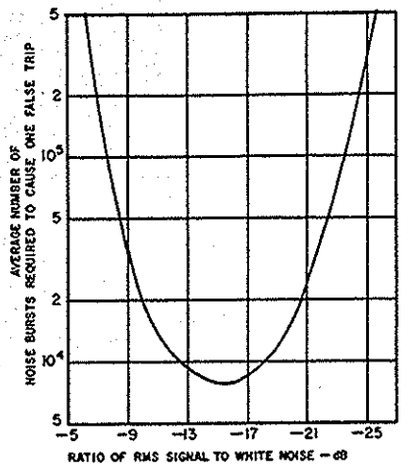


Figure 1.2. Typical security with 340-Hz spacing; measured without trip relay. System was continuously in guard, receiver-input level was −20 dBm, noise bursts were 250 ms on and 250 ms off with a noise bandwidth of 20-3000 Hz. With trip relay, security is one part in 40,000 with an S/N ratio of −15 dB.

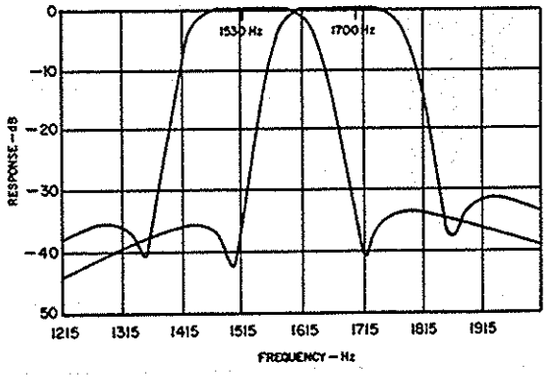


Figure 1.3. Typical response of receiver-input filters. Center frequency 1615 Hz, frequency shift ±85 Hz, bandwidth 170 Hz, and channel spacing 340 Hz.

Transmitter, receiver, power supply, and all options are housed in the Model 68 rack-mounted chassis shown in Figures 1.4, 1.5, and 1.6. The back plate of the chassis is equipped with barrier-type terminal strips for effecting external connection. The Model 68 Chassis contains 32 one-half-inch wide horizontal spaces for mounting circuit cards, and each card will require one or more such spaces. Table 1.2 shows the horizontal-space requirement of each module.

Cards may be stacked in the chassis in quantity up to the total of spaces available. As shown on Figure 1.4, the front door drops below horizontal for convenient access to circuit cards for testing or removal. Dimensions of the chassis appear on Figure 1.6.

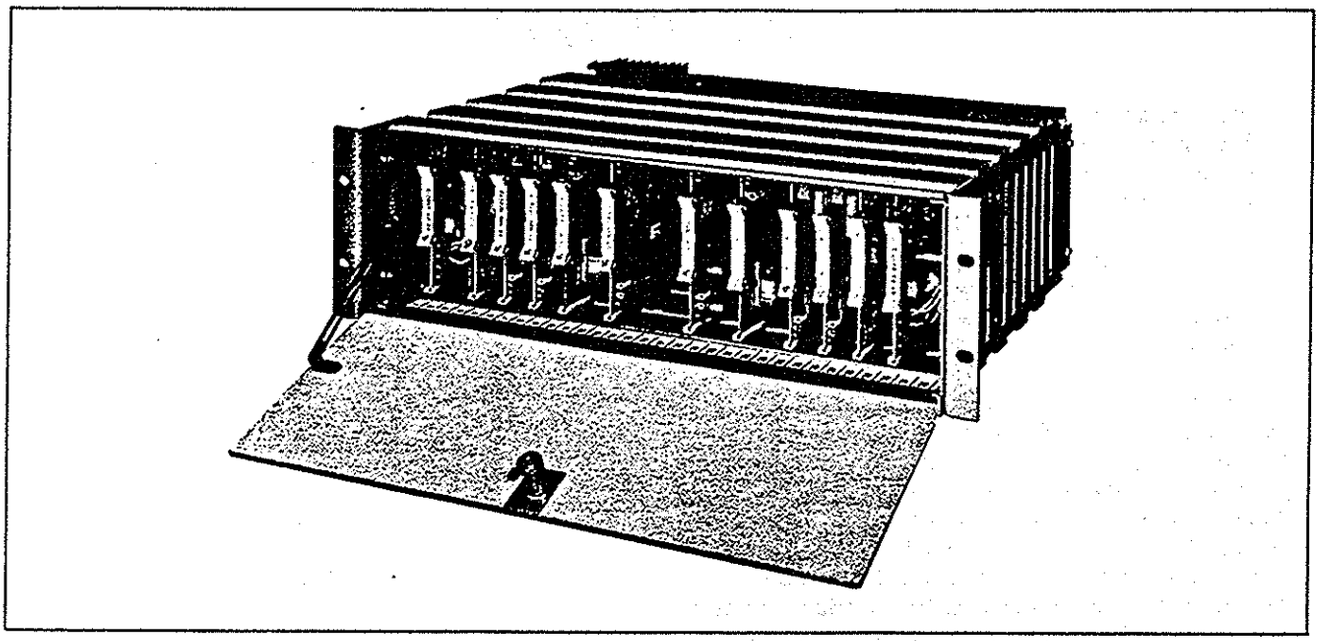


Figure 1.4. Card chassis with front door open.

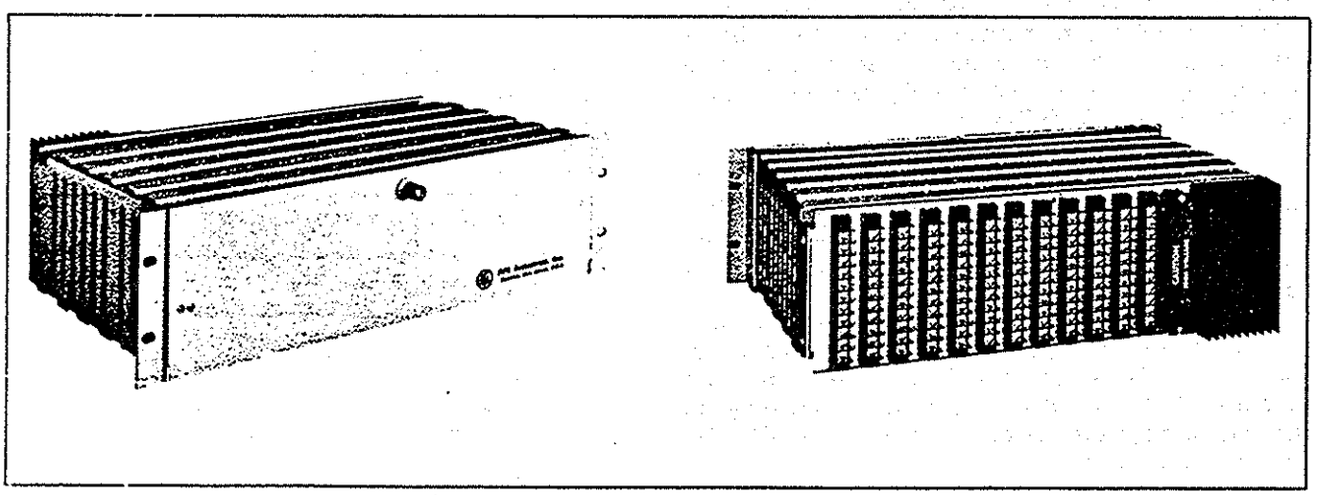


Figure 1.5. Typical card chassis.

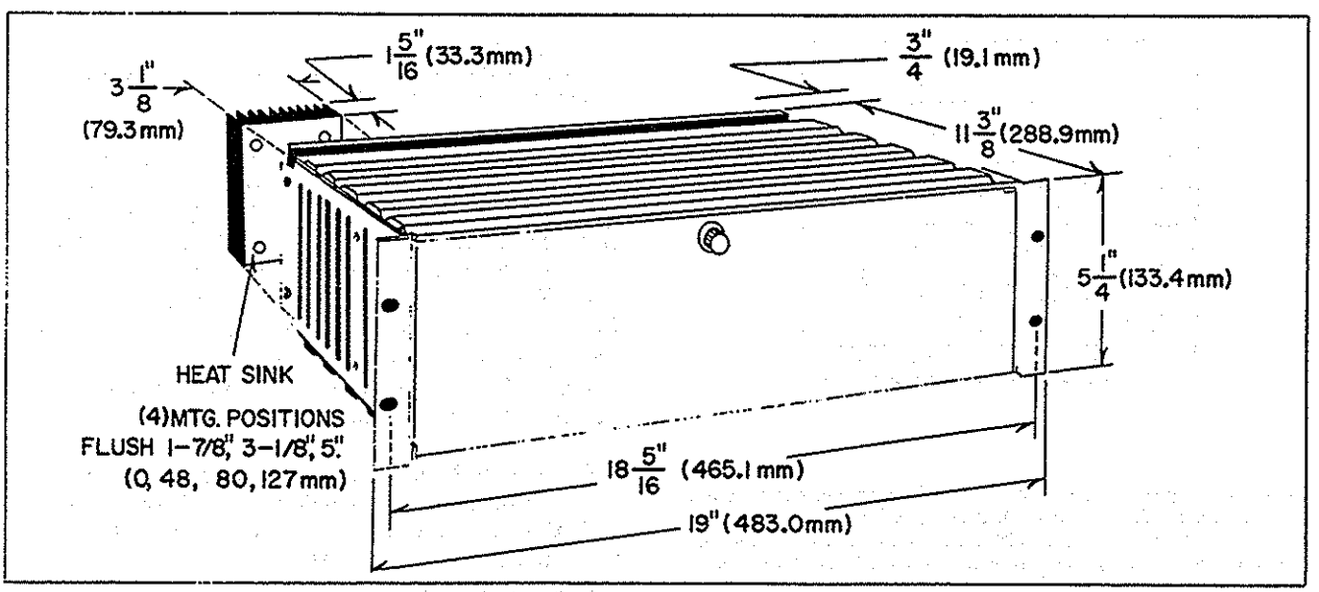


Figure 1.6. Outlines of Model 68 Chassis.

Transmitter

A block diagram showing major components of the Series 6710 System appears as Figure 1.7. At top-left of this figure, a trip voltage, taken from the station battery through a current-limiting resistor, is applied to the input device, an optical isolator. The isolator drives a Schmitt trigger which provides the high-frequency filtering and hysteresis used to suppress spurious transients that may appear at the input terminals by induction and by capacitive coupling with utility cables or other sources. Once thr trip voltage is detected by the Schmitt trigger, a logic-high signal is fed to the transmitter's logic circuit. There, by choice of jumper positions, the logic high may be used either directly, or inverted, to key the transmitter from low to high output frequency, or vice-versa.

The output of the oscillator passes first through an analog gate, used to key the output signal, and then to a summing and output amplifier, the gain of which may be adjusted, using a plug-in network, to supply the trip-boost function. Duration of the boost is set by the transmitter's logic circuit.

The output of the summing amplifier can be fed either directly to the interface module, or through an optional output filter used to reduce harmonics. On the interface module, a 600-ohm isolating transformer connects the output signal to either a two-wire or a four-wire communication circuit.

Receivers

Two receivers are used in the Series 6710 System. One is tuned to the guard frequency, while the other receives the trip signal.

Input-signal energy, entering through a 600-ohm isolation transformer, is fed to a separate bandpass filter at the input of each receiver. Each filter is set to the desired frequency, either guard or trip.

The signal then passes through two stages of amplification, through an operational rectifier, and into a lowpass filter. A voltage comparator and weighting network provide upper and lower limits of detection and compare the relative levels of signals at the two receivers. For example, when the trip signal is at a certain level, depending upon the weighting network used, above the level of guard signal, the SIG REF output terminal on the trip receiver goes high.

The high-limit, low-limit, and SIG REF logic levels from the trip and guard receivers are fed to the logic module, which has five discrete outputs, namely: TRIP OUT, GUARD OUT, ALARM, LOW-SIGNAL, and UVP (undervoltage protection). Four of these appear on the block diagram.

The logic module is provided with jumpers which can be set to provide (1) a guard-before-trip requirement, (2) to accept a trip if only an initial guard is received, or (3) to accept a trip without reception of any prior guard signal.

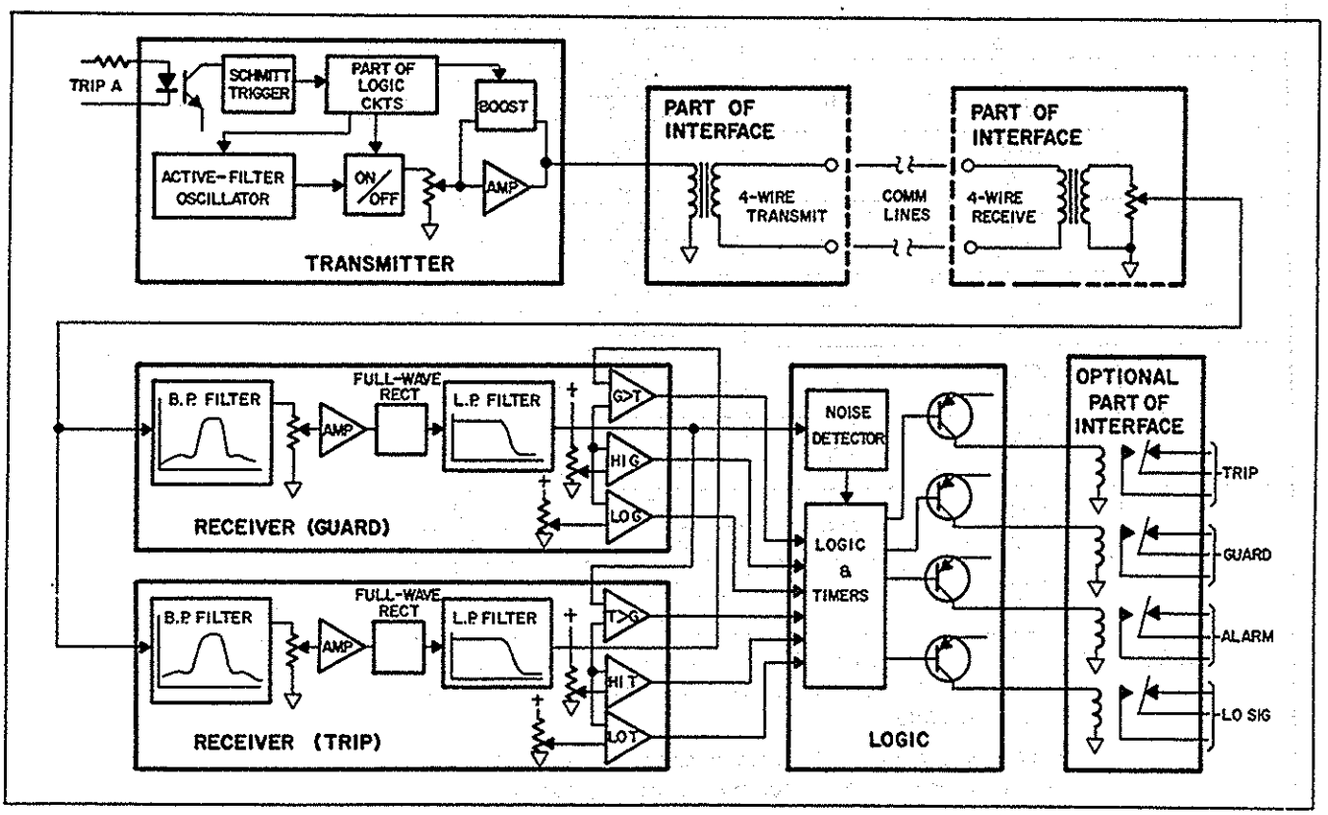


Figure 1.7. Block diagram of Series 6710 Protective-Relaying System.

A noise detector on the logic module monitors noise received in the guard channel. Excessive noise, high or low signal levels, and improper timing of signal all will cause the logic module to block trip and guard outputs and, if the improper condition persists for more than 100 ms, will signal an alarm condition.

The pre-trip timer of the logic module is a timer with two periods. These are selected according to the condition of the received signal. Normally, this timer requires that a received trip signal persist for at least 4.5 ms before it will qualify the signal as valid and produce a trip-output signal. If, however, an alarm condition occurs, the period of the pre-trip timer is lengthened to 10 ms to improve security. When desired, the pre-trip timer can be bypassed for use in high-speed, clear-channel applications.

The transistor outputs on the logic module can be used to drive external relays or to drive optionally available relays for which provision has been made on the interface module. The alarm relay is normally energized, and it is de-energized when an alarm condition exists. Trip and guard output may also be effected with Model 67AR-(XXX) Auxiliary Relays mounted on plug-in cards which fit into the Model 68 Chassis.

Plug-In Networks

Plug-in networks are used on both transmitter and receiver to facilitate a choice among certain functions.

On the transmitter, the frequency of the transmitted signal is chosen by using an appropriate plug-in network, listed in Table 1.1. The optional output filter for the transmitted signal is also a plug-in unit. The level of trip boost desired, if any, is similarly chosen.

On the receivers, plug-in networks are available to optimize security, dependability, dynamic range, or speed. It is recommended that RFL be consulted for assistance in choosing these.

TABLE 1.1
RECOMMENDED OPERATING FREQUENCIES
AND
FREQUENCY–DETERMINING COMPONENTS

GROUP	CENTER FREQ AND SHIFT Hz	CHANNEL SPACING Hz (Note 1)	OPERATING FREQ—Hz (Note 2)	SUFFIX FOR REQ'D RCVR INPUT FILTER HB-79505-(X)	SUFFIX FOR REQ'D XMTR FREQ NET HB-92966-(X)	SUFFIX FOR OPT. XMTR OUTPUT FILT. HB-79595-(X)
1	1275 ±85	340	L-1190	1	1	1
			H-1360	2		
2	1615 ±85	340	L-1530	3	2	2
			H-1700	4		
3	1955 ±85	340	L-1870	5	3	3
			H-2040	6		
4	2295 ±85	340	L-2210	7	4	4
			H-2380	8		
5	2635 ±85	340	L-2550	9	5	5
			H-2720	10		
6	2975 ±85	340	L-2890	11	6	6
			H-3060	12		
7	1275 ±170	680	L-1105	13	7	7
			H-1445	14		
8	1955 ±170	680	L-1785	15	8	8
			H-2125	16		
9	2635 ±170	680	L-2465	17	9	9
			H-2805	18		

NOTES: (1) The period of the pre-trip timer may be reduced as channel spacing is increased and as noise is reduced. See text in sections on description and on theory of logic module.

(2) Either the low or the high frequency may be used for trip while the other is used for guard. See Table 1.5 for placement of jumpers.

(3) CCITT frequencies and spacings are available on request.

On transmitters, receivers, logic modules, and on the interface, jumpers are provided to permit selection from among a variety of functions to adapt the system to the specific requirements of its application. Their functions are detailed in the section on Installation and in the various circuit-theory sections for individual modules.

Power Supply

The power supply is a dc-dc converter designed to operate from station batteries with nominal terminal voltages of 24, 48, or 129 Vdc. The converter is a 10-kHz high-power multivibrator which drives a power transformer. The output is rectified, filtered, and regulated to provide positive and negative 12-volt sources for operating the system.

TABLE 1.2
SPACE AND POWER REQUIREMENTS FOR CIRCUIT CARDS

MODEL	ASSEMBLY	DESCRIPTION	CURRENT REQUIRED		MODULE SPACES REQ'D
			+12V (mA)	–12V (mA)	
68 HPS–(XXX)–1	HB-41505 (1)	Power supply, current capacity	1.0A (2)	1.0A (2)	3
68 PS–(XXX)–1	HB-41500	Power supply, current capacity	0.375A (2)	0.375A (2)	3
67 MBB TRANS	HB-49020	Transmitter	40	3	3
Flasher	HB-49025	Option for Transmitter	4	0	0
Mute Relay	HB-49035	Option for Transmitter	40	40	0
67 MBB REC	HB-49030	Receiver	30	20	2
67 MBB AUX OSC	HB-49040	Multifrequency Oscillator	40	0	2
67 MBB LOGIC	HB-49050	Logic Circuit (3)	60	30	2
67 MBB INTER	HB-49055	Interface Card (4)	0	0	3
	HB-49559-006	Octal-base relay chassis	0	0	4
	HA-41823	High-speed octal-base heavy duty relay for trip or guard	55 (5)	55 (5)	0
	HA-33440	Heavy-duty, octal base relay for alarm or low-signal	12 (5)	12 (5)	0
67 MBB LEV IND	HB-49065	Signal Level Indicator & Monitor	78 (6)	78 (6)	2

NOTES: (1) Requires also Regulator HB-41520 mounted at back of Chassis, See Figure 1.6

(2) Also delivers 10 kHz, 40 V, unregulated.

(3) To the current demand shown for the logic circuit should be added the total current required by whatever output relays are chosen. When output relays are mounted on the interface card, their current will pass through the edge-connector fingers of that card.

(4) When the Model 67 MBB INTER is used without relays no power-supply current is taken through this card. When Model 67 MBB INTER-1 is used, maximum relay current at any one time (simultaneous LO-SIG and ALARM) will be 72 mA from both positive and negative sources. For Model 67 MBB INTER-2, the maximum relay current is 36 mA under the same conditions.

(5) Current for one relay.

(6) Includes relay current.

INSTALLATION

General

All circuit modules of the Series 6710 Protective-Relaying System are mounted in the Model 68 Chassis, shown in Figures 1.4, 1.5, and 1.6. Each chassis contains the complement of modules needed for the specified application, and each is individually wired for that application. Specific interconnection diagrams are supplied with each system. Systems comprising a number of chassis may be ordered as assemblies mounted in relay-rack cabinets. In such cases, the assembly is shipped as a unit, mounted horizontally in a wood crate, or by air-ride van.

Unpacking

Individual chassis are shipped in commercial packing cartons, one per carton. Care should be taken when opening to ensure that the equipment is not damaged or scratched. Examine all packing material carefully, so that items of value are not discarded. Packing material used in the chassis to keep modules in place during transportation should be removed carefully.

The 5¼-inch high chassis is fitted with a hinged front door. Access is gained by turning the central locking screw counterclockwise until the door can be opened. The 1¼-inch high chassis has a removable front panel, and access to the modules is the same.

Chassis mounting ears can be positioned so that the front panel is either flush or mounted forward with respect to the plane of the vertical supporting channels of the rack. Two sets of mounting holes for these ears are provided. By reversing the mounting ears in either set of holes, four choices of position are available.

Ventilation

To enhance reliability, the equipment should be operated within the specified range of ambient temperature. Ventilation should be provided to ensure that temperature limits are not exceeded within the enclosure for the equipment.

Electrical Connections

Connections to the chassis are made through barrier-type terminal blocks mounted on the rear. Details of typical input and output connections are shown in Figures 1.8 and 1.9.

When running trip-input leads, care should be taken to reduce the possibility of a false trip caused by currents induced in the leads. Trip-input leads should be assembled from shielded, twisted pair, with the shield grounded only at the chassis of the 6710. It is also recommended that these leads be physically separated from wires that carry either high current or high voltage, so that the possibility of spurious magnetic and electric coupling is minimized.

Table 1.1 includes a tabulation of part numbers for all frequency-dependent components for both transmitter and receivers, for all standard operating frequencies

Table 1.3 lists the standard choices for level-setting networks for both transmitters and receivers. RZ2 establishes the level of the transmitted signal, including non-boost, during both guard and trip. The standard choice shown for network RZ1, on the receiver, establishes the weighting ratios of guard and trip signals as well as the absolute dynamic range of the system, and it also sets the gain of the receiver's preamplifier. RFL should be contacted for availability of networks other than the standard shown.

SETUP PROCEDURE

SETUP PROCEDURE

General

This procedure assumes the equipment has been checked, is wired in a system, and is connected to a communication channel. Before proceeding, one should use Table 1.5 as a guide to be certain that all jumpers are positioned properly to obtain the performance specified. Then, transmitter-output level and receiver-input level may be set according to the procedure that follows:

Transmitter

(1) Connect a balanced, high-impedance true-rms ac voltmeter to the transmitter's output on the rear of the chassis, or to the input of the connected communication channel. This is used to monitor the output level of the transmitter.

(2) Determine the desired guard-signal output level from the transmitter, bearing in mind that if trip boost is used then the guard-signal level must be set so that the trip signal will not exceed the maximum level permitted. These maxima are given in Table 1.4. Note that signal levels cannot exceed 10 dBm for a four-wire circuit or 5 dBm for a two-wire circuit.

(3) Set the guard-signal output to the desired level by adjusting OUTPUT LEVEL, R19, on the transmitter.

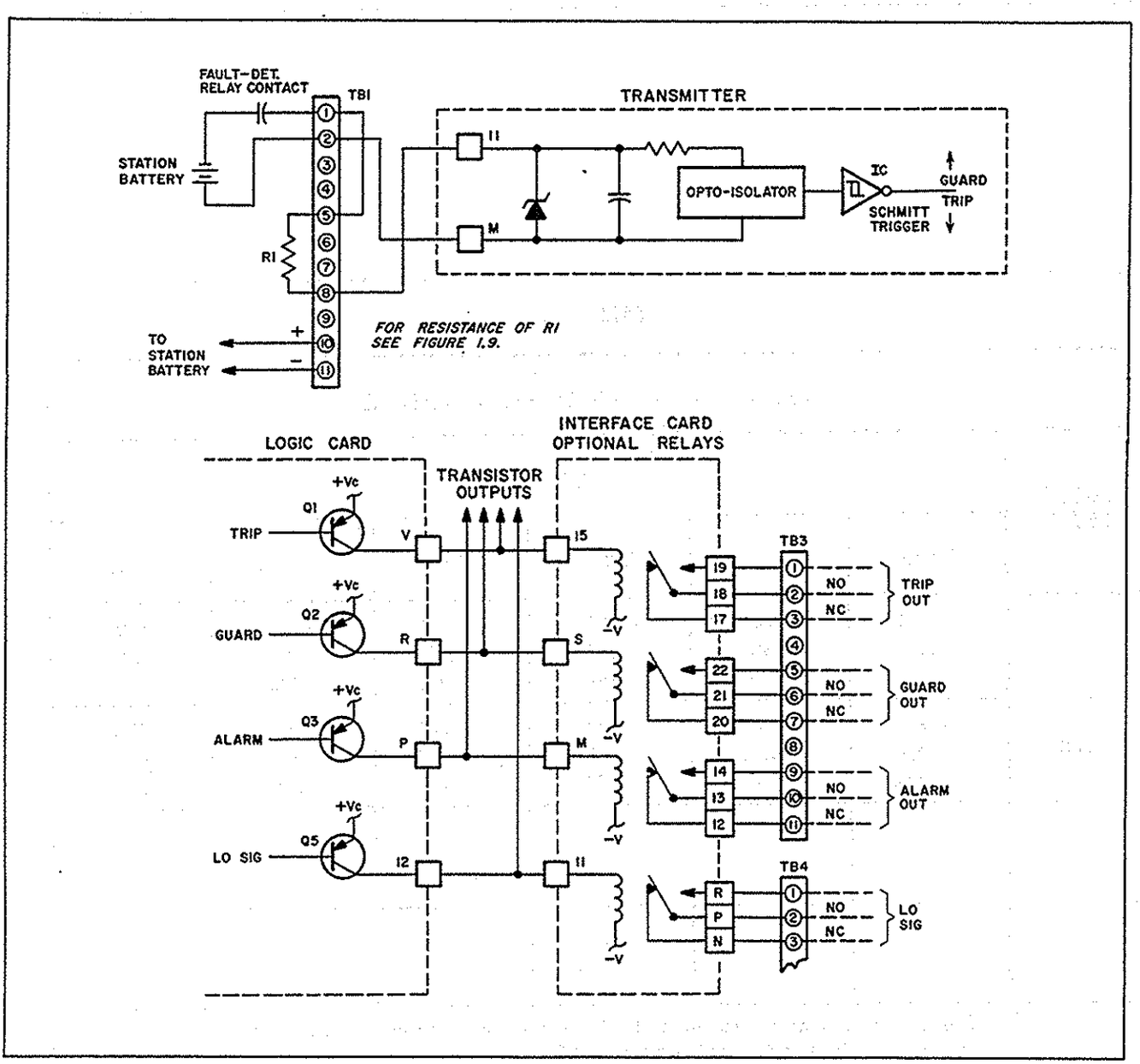


Figure 1.8. Typical input (above) and output (below) connections for Series 6710.

TABLE 1.3 PART NUMBERS FOR STANDARD LEVEL NETWORKS				
FUNCTION		TRANSMITTER	TRIP RECEIVER	GUARD RECEIVER
LEVEL	PULSE DURATION MILLISECONDS	SUFFIX FOR P/N HB-92967-(X) USED AT RZ2	SUFFIX FOR P/N HB-92968-(X) USED AT RZ1	
Non-Boost	–	–1	–1	–1
3 dB Boost	70	–2	–2	–6
6 dB Boost	70	–3	–2	–6

TABLE 1.4 MAXIMUM BOOST LEVELS AND DURATIONS						
BOOST LEVEL	BOOST TIME					
	70 ms	75 ms	100 ms	125 ms	150 ms	Units
3 dB	–.112 .977 .765	–.124 .975 .764	–.158 .967 .761	–.192 .960 .758	–.227 .952 .755	dBm mW volts
6 dB	–.308 .934 .748	–.331 .930 .746	–.424 .909 .738	–.531 .888 .729	–.615 .869 .722	dBm mW volts

This table represents the maximum level that may be sent over a 600-ohm telephone line without violating the Bell System 3pSEC. Rule.

Table 1.5
FUNCTIONS OF JUMPERS (1)

Module	Jumper	Position		Function
67 MBB TRANS	J1	A		No trip boost
		B		Timed trip boost
		C		Continuous boost during trip
	J2	A		Trip signal is higher output frequency
		B		Trip signal is lower output frequency
		C		Output frequency is fixed
	J3	A		K101 and K102 close during boost period
		B		K101 and K102 close during trip period
		C		K101 and K102 are inoperative
	J4	A		Optional flasher is operational
		B		No flasher is used
	J5	A		K101 is not used
		B		K101 is active
67 MBB AUX OSC	J1	A		Osc 3 on with trip input at B
		B		Osc 3 on with trip input at A
	J2	A		Osc 4 on if both A and B trip
		B		Osc 4 disabled
	J3	A		All osc selected by J1 and J2 are keyed by flasher
		B		No flasher control
	J4	A		Osc 1 is turned off if trip received at B
		B		Osc 1 permanently off
		C		Aux Osc module does not control Osc 1
67 MBB REC	J1	A		Gain of IC1B is 20 dB
		B		Gain of IC1B is unity
	J2	A		Enables DS3
		B		Disables DS3
	J3	A		Disables input attenuator
		B		Use only when using J4B
	J4	A		Provides direct connec. to input filter
		B		Provides 600-ohm input, attenuated 3dB when used with J3B
		C		Provides 600-ohm source impedance to input filter
67 MBB LOGIC (Note 2)	J1	A	X	No guard signal required prior to acceptance of valid trip
		B	Y	Makes jumper J2 effective
	J2	A	T	Single prior guard signal is required before acceptance of first and all subsequent trip signals
		B	G/T	Receipt of prior guard signal required before acceptance of each and every trip signal
	J3	A	A	Accepts a valid trip signal irrespective of level of signal received on guard frequency
		B	B	Defers acceptance of trip signal until guard-signal level falls below its low-limit threshold (low-signal guard).
	J4	A	A	Defeats system-blocking action when guard and trip signal levels are simultaneously above their low-limit thresholds
		B	B	Blocks system when guard and trip signal levels are simultaneously above their low-limit thresholds
	J5	A	G	Drives guard-signal output high immediately upon detection of guard signal
		B	GH	Requires received guard signal to persist for at least 15 ms before guard-signal output is permitted to go high
	J6	A	GP	Presence of a guard signal will cancel trip output
		B	TP	Presence of a trip signal will cancel guard output
67 MBB INTER	J1, J2	2W		Install for two-wire operation
		4W		Install for four-wire operation
	J3	A		Operation without transmitter-output filter
		B		Operation includes optional transmitter-output filter

Note (1) The original specification for a system will contain data providing the proper position of all jumpers for the application contemplated, and equipment will be shipped from RFL with jumpers in position. Maintenance personnel are cautioned to record positions of all jumpers before servicing, and to return them to their proper positions after testing.

(2) Some units of the Model 67 MBB LOGIC will have jumpers marked according to the designations given in the right-hand section of the column headed "Position".

Interface

(1) At the sending terminal in the system, adjust the transmitter according to the foregoing procedure.

(2) On the guard receiver, connect a sensitive dc voltmeter between TP2, OUTPUT (BLU) and TP3 GND (BLK).

(3) While a guard signal is being received at normal level, adjust R6, REC LEVEL ADJ, on the interface card until the dc output voltage measured is 1.6 Vdc. It may be noted that in systems employing trip boost the voltage at this point in the trip receiver will be lower by the amount of trip boost used.

The sensitivity of both guard and trip receivers has been adjusted at the factory to be identical. Because the foregoing adjustment was made on the interface card, and because no adjustment was made on either receiver, this adjustment sets the input signal to the proper level for both receivers. Though not necessary, those who wish to check the sensitivity of the trip-signal receiver may use a non-boosted trip signal as a test signal to check sensitivity of the trip receiver, but without disturbing the adjustment previously made on the interface card.

For adjustment of individual receiver-sensitivity controls, reference may be made to the discussion of receiver-circuit details starting on page 33 of this book.

This completes the adjustment of the basic system. The user may wish to use additional tests to check and adjust optional functions that may have been specified. Figure 1.10 shows typical waveforms.

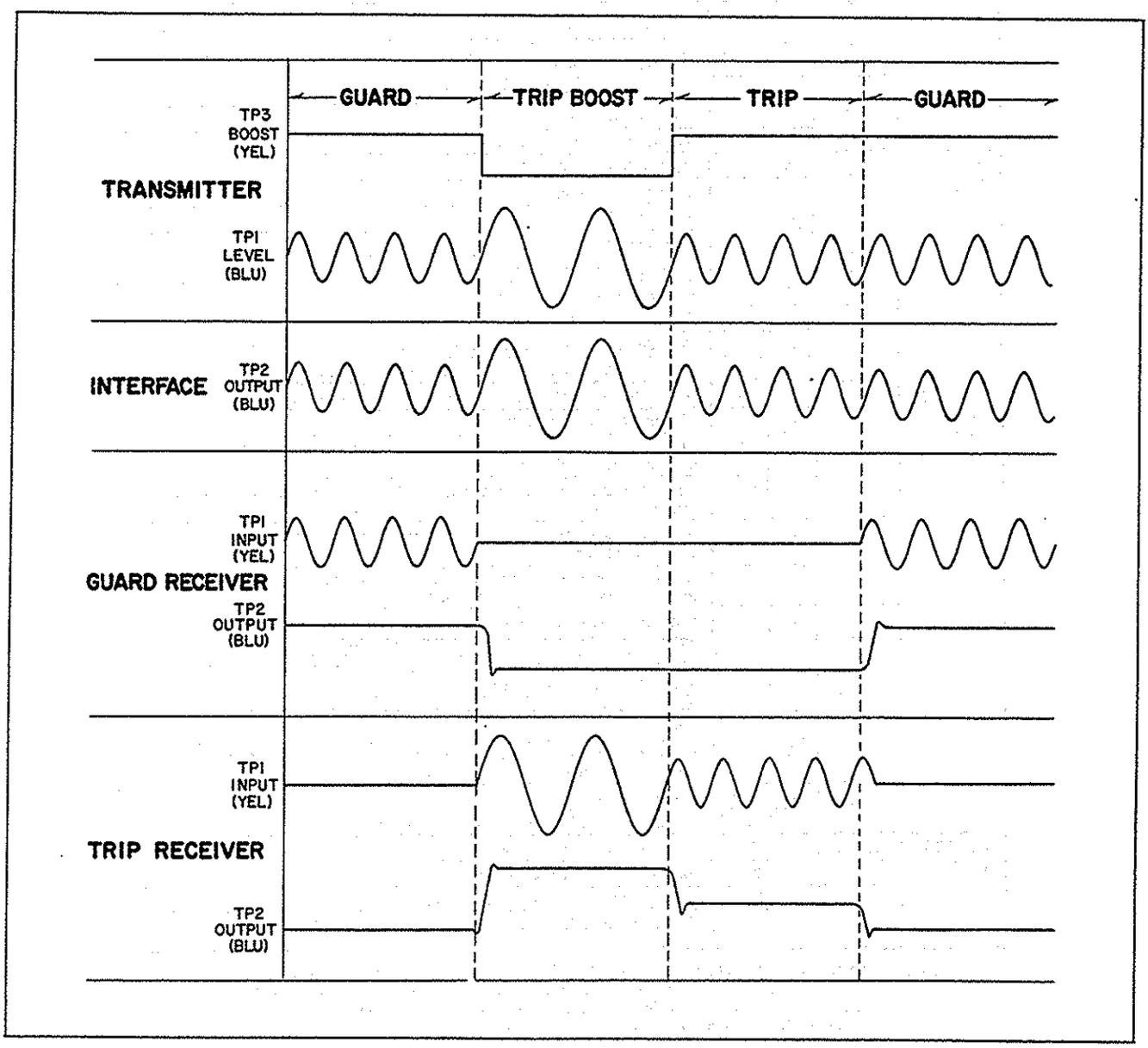


Figure 1.10. Test-point waveforms found in a typical system.

Multiplexing

Frequency multiplexing transmitters on a single communication line is simply accomplished, in the Series 6710 System, by connecting all output terminals in parallel and to Terminal E of the single interface card used for all signals. The interface card, of course, must be equipped with Option HB-49060, which is the transmitter-combining amplifier, shown on the schematic of the interface card.

Frequency multiplexing receivers is done by connecting all receiver-input terminals together and to Terminal 5 of the single interface card used for all signals.

Multiplexing connections for receivers and transmitters when located in different chassis are shown in Figures 1.11 and 1.12.

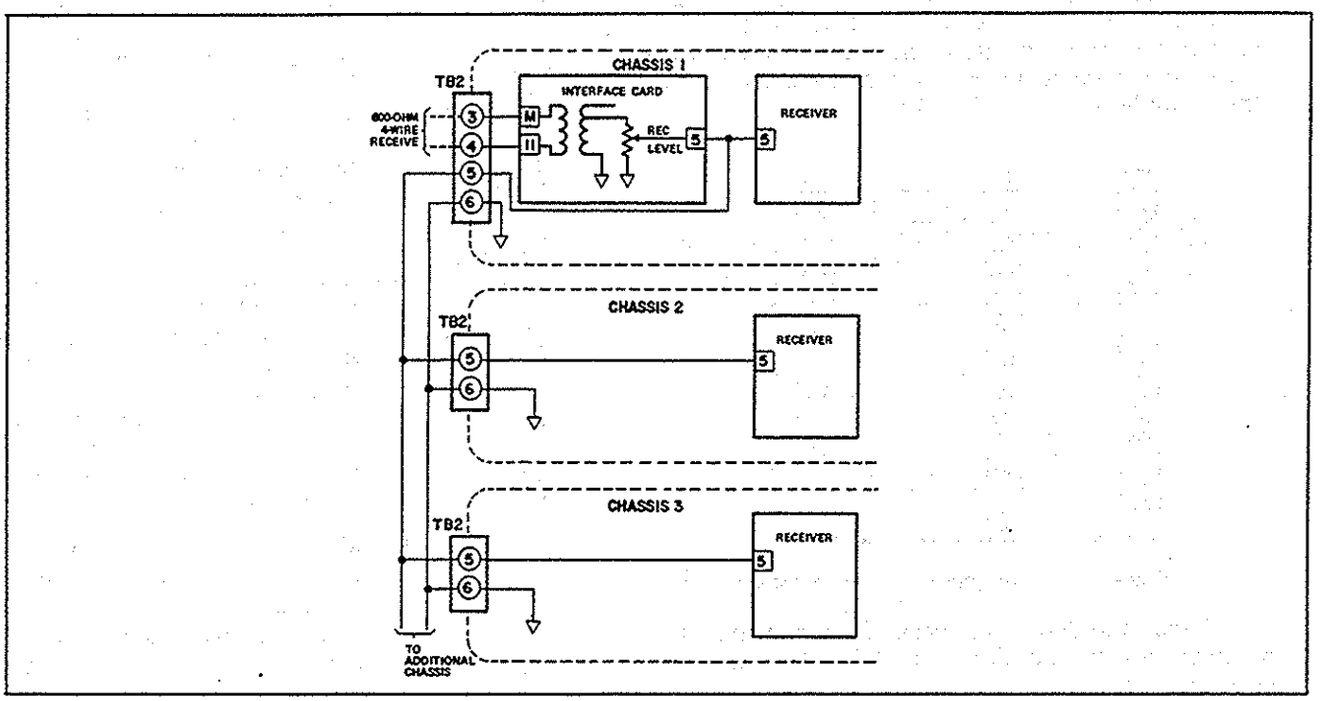


Figure 1.11. Multiplexing connections for receivers when mounted in separate chassis.

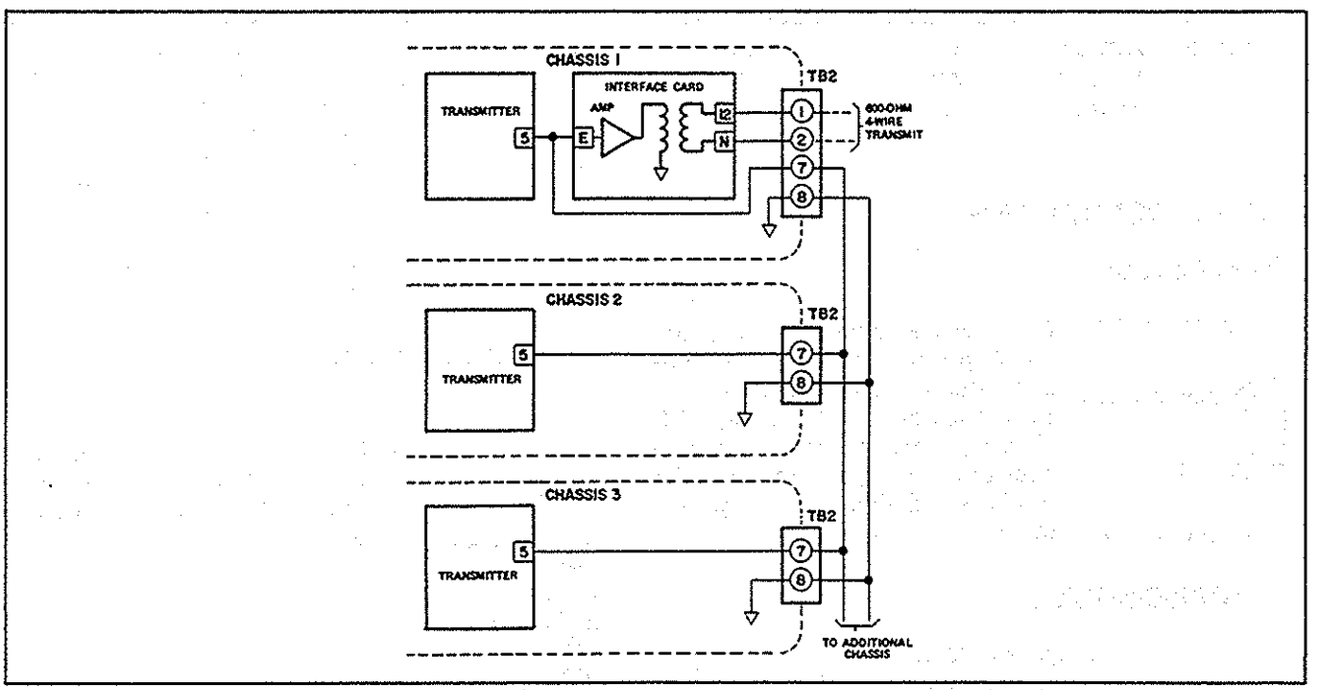


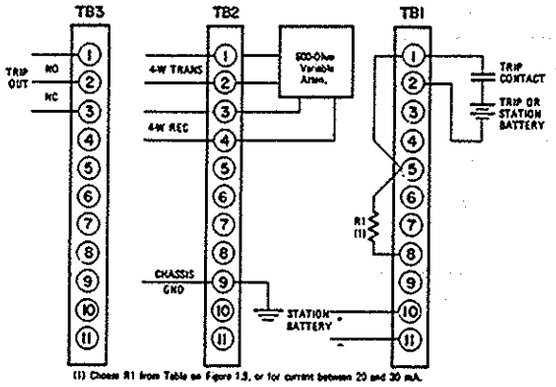
Figure 1.12. Multiplexing connection for transmitters when mounted in different chassis.

PROCEDURE FOR FIELD-ACCEPTANCE TESTS

The following procedure is intended to aid in validating the performance of each module of the system.

By referring to Table 1.5, check for proper placement of jumpers on each module.

Connect the equipment as outlined in Figure 1.13, in which it is assumed that transmitting and receiving frequencies are identical. If this is not the case, then both terminals must be available so that they may be tested back-to-back.



(1) Choose R1 from Table on Figure 1.5, or for current between 20 and 30 mA.

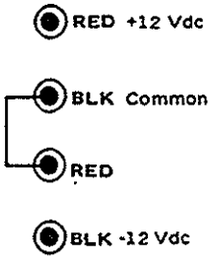
Figure 1.13. Connections for field-acceptance tests.

Check the dc-dc converter for correct polarity of input power, and for correct input voltage as listed below:

Model	Nominal Input Voltage	Input Voltage Range, Vdc
68 HPS-24DC-1	24	21-28
-48DC-1	48	42-56
-129DC-1	129	105-145

DC-DC CONVERTERS

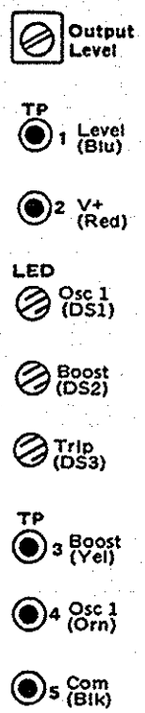
Test Points:



Move power switch to ON, and check positive and negative output voltages. These should be in the range between 11.4 and 12.6 Vdc. Input voltage may be varied over the range given to check for ±1% regulation of the power supply.

TRANSMITTER

(a) Check Table 1.1 for proper frequency-determining network, and Table 1.3 for proper trip-boost network.



(b) With a sensitive ac voltmeter connected between TP1 and TP5, check the span of the OUTPUT LEVEL control. It should range between 50 mV and 5 Vrms. With trip boost, the level observed will be below the maximum by the level of trip boost being used. Leave transmitter set at maximum output. Place a jumper between TP4 and TP5 and note that this should cancel the output signal, as indicated when DS1 extinguishes. Remove jumper and observe that output signal returns.

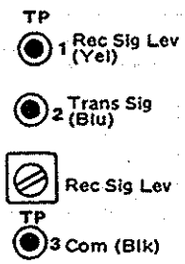
(c) Move voltmeter to output terminals at rear of chassis and check for maximum output level, depending upon whether a two-wire or four-wire connection is used. These levels are given in the Specifications, and the observed level will be reduced by the level of trip boost used.

(d) Monitor the output frequency with a frequency counter connected to TP1. Check for presence and frequency of guard signal. Key the transmitter to trip and check for presence and frequency of trip signal.

(e) If the system uses the trip-boost function, connect a jumper from TP3 to TP5. This will boost the signal level continuously, and the level may be measured with a sensitive ac voltmeter at TP1. Note that DS2 will be illuminated during trip boost.

(f) Key the transmitter to trip and observe that DS3 illuminates.

INTERFACE MODULE



(a) Measure the received-signal level at TP1 (YEL). It should be between 30 and 50 mVrms at this point

RECEIVERS

6(a) Guard Receiver

LED
Sig > Ref (DS3)
Hi Sig (DS1)
Lo Sig (DS2)
TP
1 Input (Yel)
2 Output (Blu)
3 Com (Blk)

(a) Connect a sensitive ac voltmeter to TP1 (YEL) and check for presence of guard signal at a level of approximately 10 mVrms.

Connect a dc voltmeter between TP2, OUTPUT (BLU) and ground. On the interface card adjust REC INPUT LEV for a dc-output voltage from the guard receiver of 1.6 volts. Do not adjust the sensitivity potentiometer on the receiver, for this is set permanently at the factory.

(c) Increase the input signal by 10 dB. The HI SIG lamp, DS1, should illuminate.

(d) Decrease the input signal to 10 dB below the level set at (a), foregoing. The LO SIG lamp, DS2, should illuminate.

(e) Return input signal to normal level. Since the system is transmitting a guard signal, the SIG>REF lamp, DS3, will be illuminated.

6(b) Trip Receiver

LED
SIG > REF (DS3)
Hi Sig (DS1)
Lo Sig (DS2)
TP
1 Input (Yel)
2 Output (Blu)
3 Com (Blk)

(f) Key the transmitter to trip. On the guard receiver, DS3 should extinguish and DS2 should be illuminated. Simultaneously, on the trip receiver DS3 should illuminate and DS2 should extinguish. Key the transmitter successively between guard and trip and note the significance of the changes in illumination of the lamps. Note that at no time should DS1, HIGH SIG, be illuminated on either receiver. Return the transmitter to trip.

(g) For the trip receiver, repeat steps (a) through (d) given for the case of guard receivers, except that at (b) do not readjust REC SIG LEV on the interface card. It was already adjusted to produce 1.6 Vdc at TP2 in the guard receiver with guard signal present, and the dc output level of the trip receiver should now automatically be 1.6 Vdc when an unboosted trip signal is used. If, however, the system uses trip boost, the trip receiver's output voltage will be reduced by the level of boost used. For example, if the system uses 3-dB trip boost then with the guard receiver set for an output voltage of 1.6 Vdc, the output from the trip receiver with an unboosted input will be 1.35 Vdc.

If this condition does not prevail, then R1, SENSITIVITY, may be adjusted on the trip receiver. A card extender will be required to gain access to R1 while the receiver is operating. Normally it is to be expected that R1 is already set at the factory and should need no further adjustment.

(h) With the input signal at its nominal level of −20 dBm, key the transmitter alternately between guard and trip. In each case check for an output voltage of 1.6 Vdc, without trip boost, at TP2 (BLU) of the proper receiver.

LOGIC MODULE

LED
Trip (DS1)
Guard (DS2)
Alarm (DS3)

(a) With the system receiving a guard signal at normal level, GUARD, DS2, should be illuminated.

(b) Key the transmitter to trip and note that DS1, TRIP, illuminates and that DS2 extinguishes.

(c) Change signal level by more than 10 dB both above and below the nominal −20 dBm level. ALARM, DS3, should illuminate, DS1 should extinguish, and DS2 should remain off. Without changing signal level, change system to guard frequency. DS3 should remain illuminated. Return signal to normal level. DS3 should extinguish, and DS2 should illuminate.

OPTIONAL TESTS

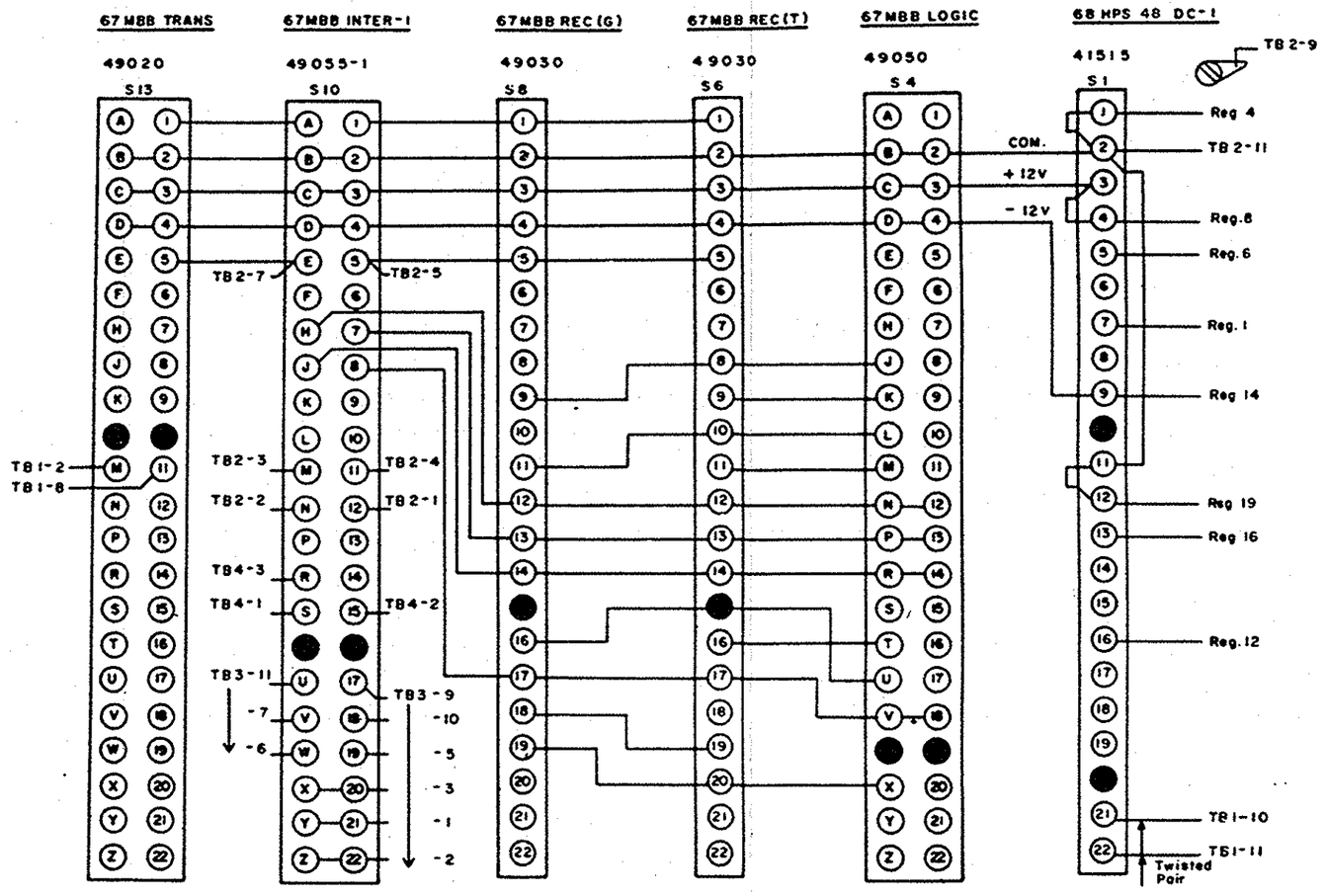
The foregoing tests are designed to verify normal operation of the basic modules of the Series 6710 System. When other features are added to the system, a similar procedure for verification of performance is recommended for every feature.

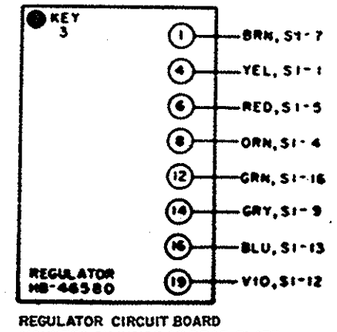
TABLE I

SERIES RESISTORS FOR TRIP KEYING				
TRIP VOLTAGE	24	48	110	129
RI OHMS	500	1500	3500	4500
RI RFL P/N	H-1100 -308	H-1220 -35	H-1100 -701	H-1100 -690

NOTES (WHERE APPLICABLE)

1 S - INDICATES PRINTED CIRCUIT BOARD SOCKETS
2 TB - INDICATES BARRIER STRIPS
3 ● - INDICATES KEY LOCATION
4 WIRING IS NO 22 STRANDED OF COLOR MARKED UNMARKED WIRE IS BUS WIRING AND/OR PART OF CIRCUIT BOARD DEPENDING UPON APPLICATION
5 RELAY CONTACTS ARE SHOWN UNENERGIZED
6 CHASSIS EQUIPPED WITH EXTERNAL JUMPER BETWEEN CIRCUIT COMMON AND RACK GROUND
7 MOUNT RESISTORS EXTERNAL PRODUCTION PLEASE NOTE
8 FOR 2W OPERATION CONNECT TONE LINE ON TB2-1 & 2
9 FOR 4W OPERATION CONNECT TX TONE LINE ON TB2-1 & 2 AND RX TONE LINE ON TB2-3 & 4.
} Refer to 67 MBB INTER Data Sheet
10 FOR UNI DIRECTIONAL SYSTEMS STRAP 67 MBB INTER 4W AND CONNECT TONE LINE AT 4W INPUT OR OUTPUT ON TB2
11 TO SEND TRIP APPLY VOLTAGE TO TB1-1 & 2
12 TO DETECT TRIP, CONNECT INDICATOR AND BATTERY BETWEEN TB3-1 & 2
13 TRIP & GUARD RELAY CONTACTS WIRING TO BE ROUTED IN SEPARATE HARNESS.





REGULATOR CIRCUIT BOARD MOUNTED ON INSIDE OF REAR PLATE

PARTS LIST

(1) 46963-001 FRONT PANEL
(1) 46964-002 REAR PANEL
(1) 1220-35 RESISTOR 1.5k, 5w (R1)

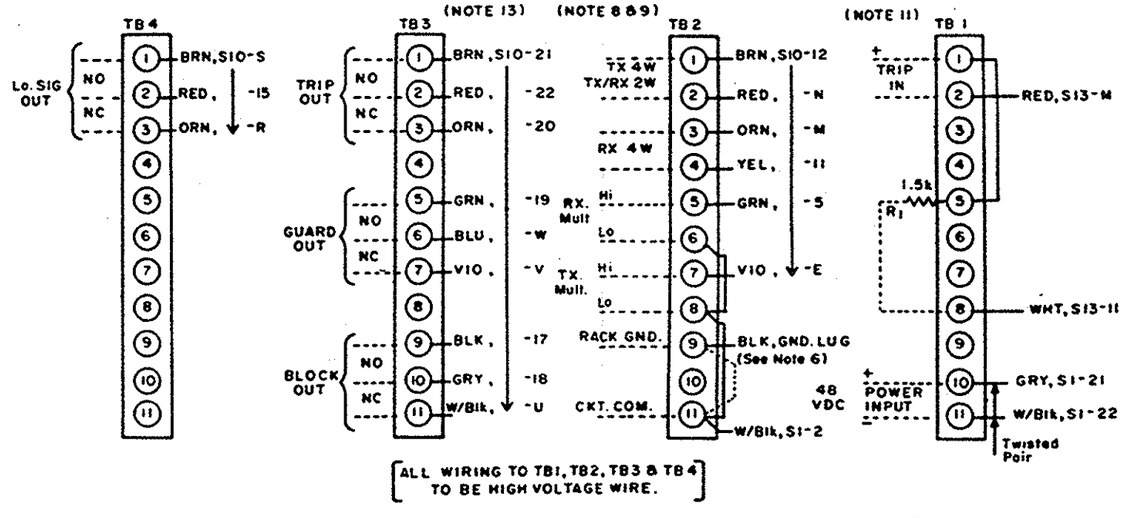


Figure 1.9. Typical interconnections in chassis.

Transmitter, Model 67 MBB TRANS

GENERAL

The transmitter of the Series 6710 System uses a two-frequency active-filter oscillator to generate the transmitted signal. The trip-keying circuit uses an optical isolator to isolate the system from the keying circuit. Trip-boost control, which elevates the level of a trip signal above that used for transmitting the guard signal, is available, and a low-voltage detector is used to monitor the power-supply voltage for protection against accidental generation of a false trip signal in the event that power-supply voltage should fail.

Three plug-on circuit cards are available for optional use with the transmitter. These are (a) an output filter for the transmitted signal, (b) a flasher which switches the output signal rapidly between trip and guard frequencies, and (c) a mute-relay card with two relays. Table 2.1 lists assigned model designations.

TABLE 2.1
MODEL DESIGNATIONS FOR TRANSMITTERS

FS TRANSMITTER SERIES 6710	HB-49020 Transmitter	HB-49025 Flasher	HB-49035 Mute Relay DPDT
67 MBB TRANS	•		
67 MBB TRANS-1	•	•	
67 MBB TRANS-2	•		•
67 MBB TRANS-3	•	•	•

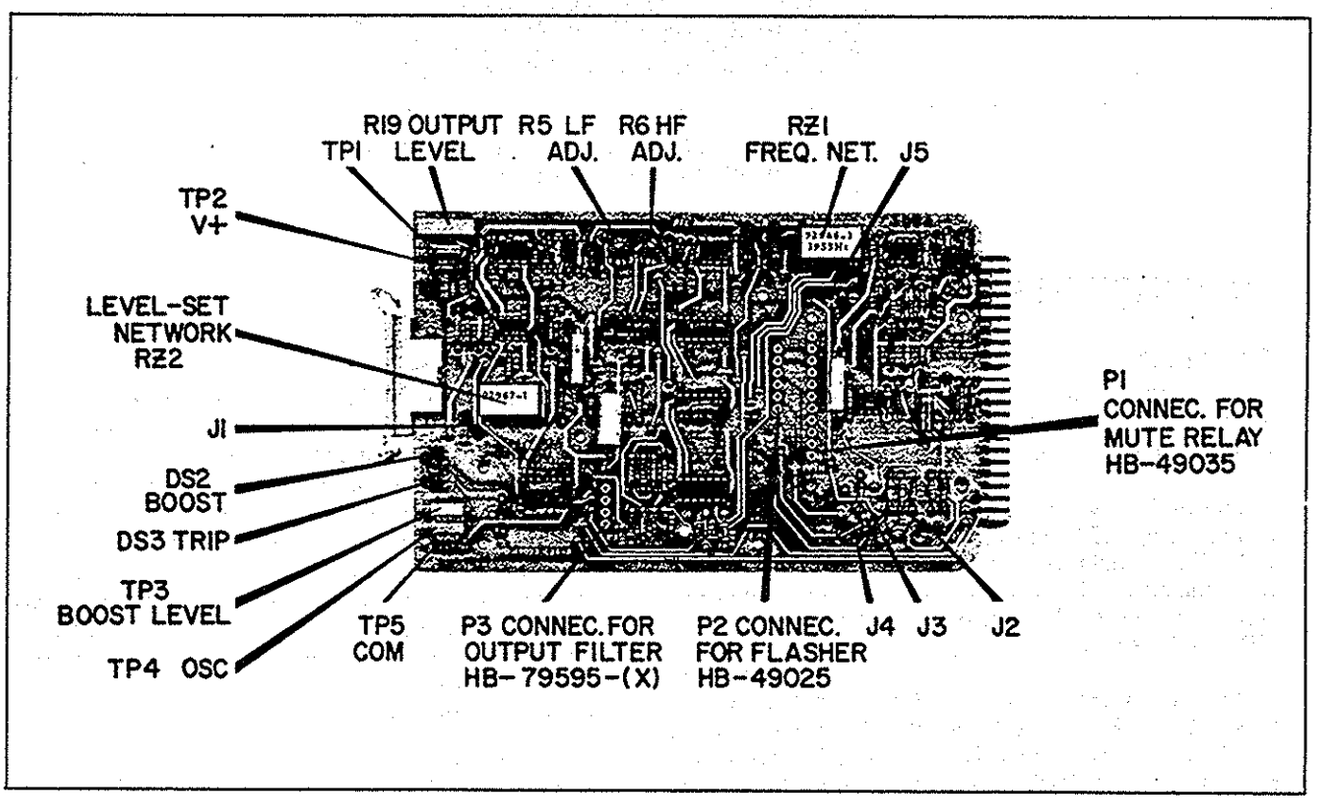


Figure 2.1. Model 67 MBB TRANS.

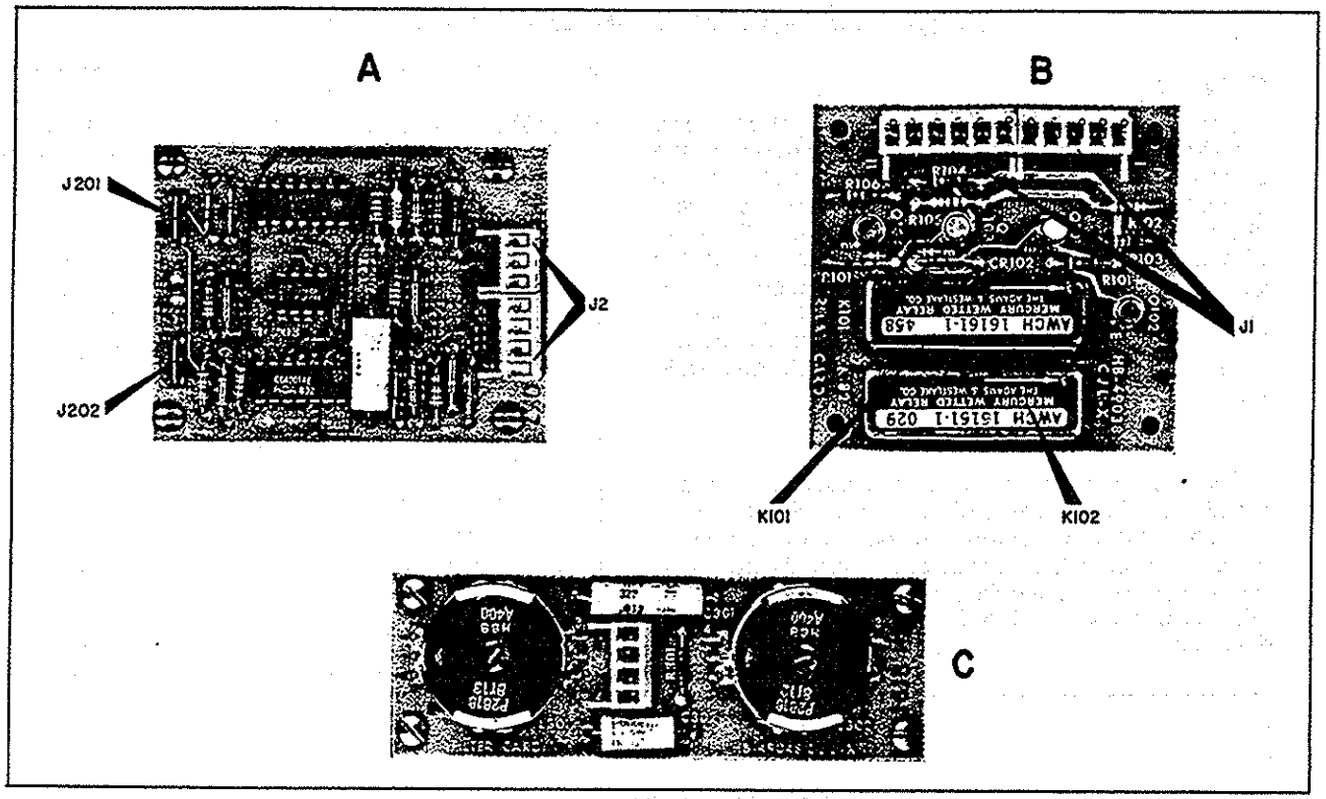


Figure 2.2. Optional plug-on cards for Model 67 MBB TRANS: A, HB-49025 Flasher; B, HB-49035 Mute-Relay Card, C, HB-79595 Output Filter.

CIRCUIT THEORY

Oscillator

The signal-generating portion of the transmitter is an active-filter oscillator, designated as Oscillator 1. It appears in the upper-left section of Figure 2.3.

The active elements of the oscillator are the two integrators, IC2A and IC2B, and feedback amplifier IC1. The oscillator is free running at a frequency determined by the resistance of the six elements of plug-in resistor RZ1 and by the capacitance of C8, C9, C10, and C11.

It will be observed that resistance-elements 3-14 and 6-11 of RZ1 may be shunted across elements 2-15 and 7-10, respectively, if the bilateral switches, IC7D and IC7C, are closed. When these switches are closed, the net resistance in each frequency-controlling circuit is reduced, and so the frequency of oscillation is increased. The control pins of these switches are connected together and to the control circuits for keying the output signal to either guard or trip frequency. A logic high causes the switches to become conducting.

Two adjustments have been provided on the circuit board for fine-tuning the oscillator to each of its two output frequencies. R5 is the low-frequency adjustment, while R6 sets the higher output frequency. Both are in the feedback path, and each is controlled by a bilateral switch. The control terminals of the one switch are connected through IC6D, used as an inverter, so that when one switch is turned on the other is off. IC5D-12 is connected to the transmitter-keying line, which raises the output frequency when this line is at a logic high. This same signal, passed through IC6D to IC5A-13, holds the latter switch off and renders R5 ineffective. R6 thus controls the value of the high frequency. With a logic low on the keying line the reverse occurs, and R5 sets the lower of the two output frequencies.

The output of the oscillator is taken from the output of the first integrator, at IC2B-7, and it is fed to a summing amplifier through bilateral switch IC7B. The control function, at Pin 5, is carried to the edge connector, at Terminals 7 and H, so that the output signal from the oscillator may be keyed on and off by a logic signal derived from an external source. A logic high will permit the signal to pass through the switch. DS1 will be illuminated when any signal from Oscillator 1 is being fed to the summing amplifier. TP4 (ORN) has been provided as a control point at which the oscillator may be keyed on or off for test purposes by applying either 12 Vdc or ground.

Summing Amplifier

IC4B is a summing amplifier used to combine the signal from Oscillator 1 with signals obtained from the auxiliary-oscillator module. These may be introduced through the edge connector at Terminals 9 and K.

A second function of the summing amplifier is to act as a boost amplifier by changing its gain when trip-boost operation is required during transmission of a trip signal.

Under normal conditions, the feedback resistor for IC4B is the parallel value of RZ2, elements 8-9 and 7-10, because the bilateral switch, IC7A, is normally held in its conducting condition. When trip boost is required, IC7A is opened. This removes RZ2 element 7-10 from the feedback network and raises the amplifier's gain by the chosen amount. The control signal used to switch IC7A also causes DS2 to illuminate during the period of trip boost. The choice among no boost, timed trip boost, or untimed trip boost is made by placing Jumper J1 in the desired position at the output of the trip-control circuit. This will be found at the lower center section of Figure 2.3.

Output Amplifier

The output of the summing amplifier is fed through R19, the OUTPUT LEVEL control, to IC3. R24 provides a 600-ohm source impedance for the output signal which appears between Terminal 1 and circuit common.

Trip Circuit

An optically isolated trip circuit, based on the use of opto-isolator IC8 and Schmitt trigger IC10C, is used for keying the transmitter. IC8 requires a 20-mA trip current. This is taken from the station battery, through the contacts of the trip relay, and through a dropping resistor whose resistance is determined by the voltage of the station battery as detailed on Figure 1.9. When the trip current passes through the light-emitting diode in IC8, the associated transistor becomes conducting and drops the voltage on IC10-5 from a logic high to a logic low. IC10C-6 then becomes a logic high.

Assume that Jumpers J2-A and J4-B are in place. In that case, the logic high from IC10C will cause switches IC7C and IC7D to become conducting and thereby to shift the output frequency to its higher value to signify a trip. Note that with Jumper J2 in Position B the normal (guard) condition of Oscillator 1 is with both bilateral switches conducting, so that guard frequency will be the higher frequency and trip will be signified with a shift to a lower frequency.

Trip-Boost Timer

The trip-boost timer is initiated from the trip signal which appears at IC10C-6. It consists of NOR gate IC6B, buffer IC10E, a timer circuit using RZ2 element 4-13 and C3, and comparator IC4A which operates with a reference of six volts at Pin 3.

The flip-flop comprised of IC9A and IC9B is initially set with IC9A-3 low and IC9B-4 high. This places a logic high on IC9C-8. Pin 9 of IC9C, however, is still low so that IC9C-10 is high, and there is no trip-boost signal. When the output of IC10C goes high, however, meaning that a trip command has been received, the output of IC6B goes low and drives the output of IC9C low to create a trip-boost signal. After about 0.7 time constants, the output of comparator IC4A will go low and reset IC9A high and IC9B low. This forces IC9C-10 high, and the trip-boost signal then returns to the non-boost condition. Trip-boost time is determined, thus, by the time constant, which is selected with a choice of plug-in unit RZ2.

Terminals 8 and J provide for control of the trip-boost circuit from an alternate source.

Low-Voltage Detector

A low-voltage detector is used to protect against possible generation of a false trip in the event of low power-supply voltage. Under normal conditions, the supply provides 12 Vdc and current flows through the base-emitter junction of Q1, which is found near the center of Figure 2.3. The collector of Q1 is, therefore,at approximately 12 volts, and it holds the control terminal of IC7B so that this bilateral switch is normally conducting. The sum of the zener voltage of CR6, 9.1 volts, and of the base-emitter voltage of Q1, 0.7 volt, is 9.8 volts. If the power-supply voltage drops below 9.8 volts, Q1 will no longer conduct, and switch IC7 will become open and prevent the passage of signal from Oscillator 1 to the output. The undervoltage-control signal is also brought out to the edge connector, at Terminal Y.

Mute-Relay Card

When the protective-relaying signal is carried as part of a speech-plus-data system, it is frequently desired, while transmitting a trip signal, to cancel all other data and speech signals and to dedicate the entire power in the channel to this one signal. The mute-relay card, designated as Option HB-49035, provides relays for effecting this function. It carries two relays with mercury-wetted, Form-C contacts, and each relay has a separate driver circuit.

Operation of the relays is under control of the signal from Jumper J3. With J3 at Position A, the relay-control signal appears upon initiation of a trip command and continues for the duration of either the trip-boost time or of the trip-command time, whichever is shorter. With J3 at Position B, the relay-control signal continues for the duration of the trip-command signal. At Position C there is no control signal.

With Jumper J5 at Position B, both relays will respond to the control signal. With J5 at position A, only K102 will respond to that signal.

Flasher

A flasher, Option HB-49025, is a plug-on card that mounts on the transmitter. It is used to shift the transmitter's output frequency, or the frequency of an auxiliary oscillator, or both, alternately between guard and trip whenever a trip command is received. The circuit of the flasher is shown as Figure 2.4.

The flasher has two modes of operation. These are controlled by the position of Jumpers J201 and J202.

With both jumpers in Position A, the flasher will respond to a trip command by shifting the oscillators under its control to trip frequency for a period equal to 1.14 time constants of R205 and C201, after which period it will return the oscillators to guard frequency and hold them there irrespective of the fact that a trip-command signal may still be present.

With the jumpers in Position B, the flasher will cause the oscillators under its control to shift alternately between guard and trip frequencies. The oscillators will remain at each frequency for a period equal to 1.14 time constants of R205 and C201. R205 may be changed to alter this period. When R205 is 200K ohms the period at each frequency is approximately 25 ms, so the flasher operates at a rate of approximately 20 Hz.

When Jumper J4, Figure 2.3 is in position A, and with Jumpers J201 and J202 both in Position B, then a trip-command signal appears at both IC201C-8 and IC202C-8. IC201C-9 is also high because this is its quiescent, or guard, state. Then IC201C-10 will be high and key the transmitter from guard to trip frequency.

Simultaneously, IC202C-10 and IC202A-1 will go low. IC202A-2 was already low because that is its quiescent state through IC202D. The output of IC202A is, therefore, high, and the inverting input of IC203 will follow that high somewhat later, as determined by the time constant of R205 and C201. About 1.14 time constants later, the voltage at IC203-2 will have risen above that at IC203-3 and cause the comparator to respond with a logic low at its output, Pin 6. This low is repeated at IC201A-3 and at IC201C-9. This causes IC201C to shift the transmitter from trip to guard frequency.

The logic low at IC201A-3, propagated through IC202D and IC202A, appears at IC202A-3 as a low. This discharges C201 through R205, and 1.14 time constants later the output of IC203, at Pin 6, will go high, restore the high at IC201C-9, and once again the transmitter will shift from guard to trip

Under normal conditions, the frequency-controlling capacitor in an RC oscillator, C201 in this case, will charge and discharge between about 60 and 30 percent, respectively, of its target voltage, except for the first cycle, for which its excursion from its quiescent state requires a voltage change of about 60 percent of the range. Therefore, the first trip signal from the transmitter could be expected to be longer than succeeding signals.

To prevent this, the arrival of a trip signal, which is a logic low at both input terminals of IC202B, causes IC202B-4 to rise instantaneously, and to pull the lower terminal of C201 almost instantaneously to a level equal to about one-third of the supply voltage, as set by R206 and R207.

In the single-trip mode, the oscillator's feedback path is opened at J202. The trip is propagated through the circuit as in the flasher mode, but 1.14 time constants later it is cancelled by the logic low from the output of IC203. This condition is held indefinitely because of the hysteresis provided by R211. When the trip-command signal disappears, IC202A-3 returns to a logic low and C201 is discharged rapidly through CR202.

The foregoing description of the operation of the flasher circuit holds true also for a trip signal at Input B,except that IC201D becomes the gate controlling the signal to the oscillators.

Output Filter

The optional output filter for the transmitted signal is a two-coil filter mounted on a plug-on card that fits the transmitter module. The balanced output signal has a nominal source impedance of 600 ohms within the filter's passband, and a rising impedance out of the band.

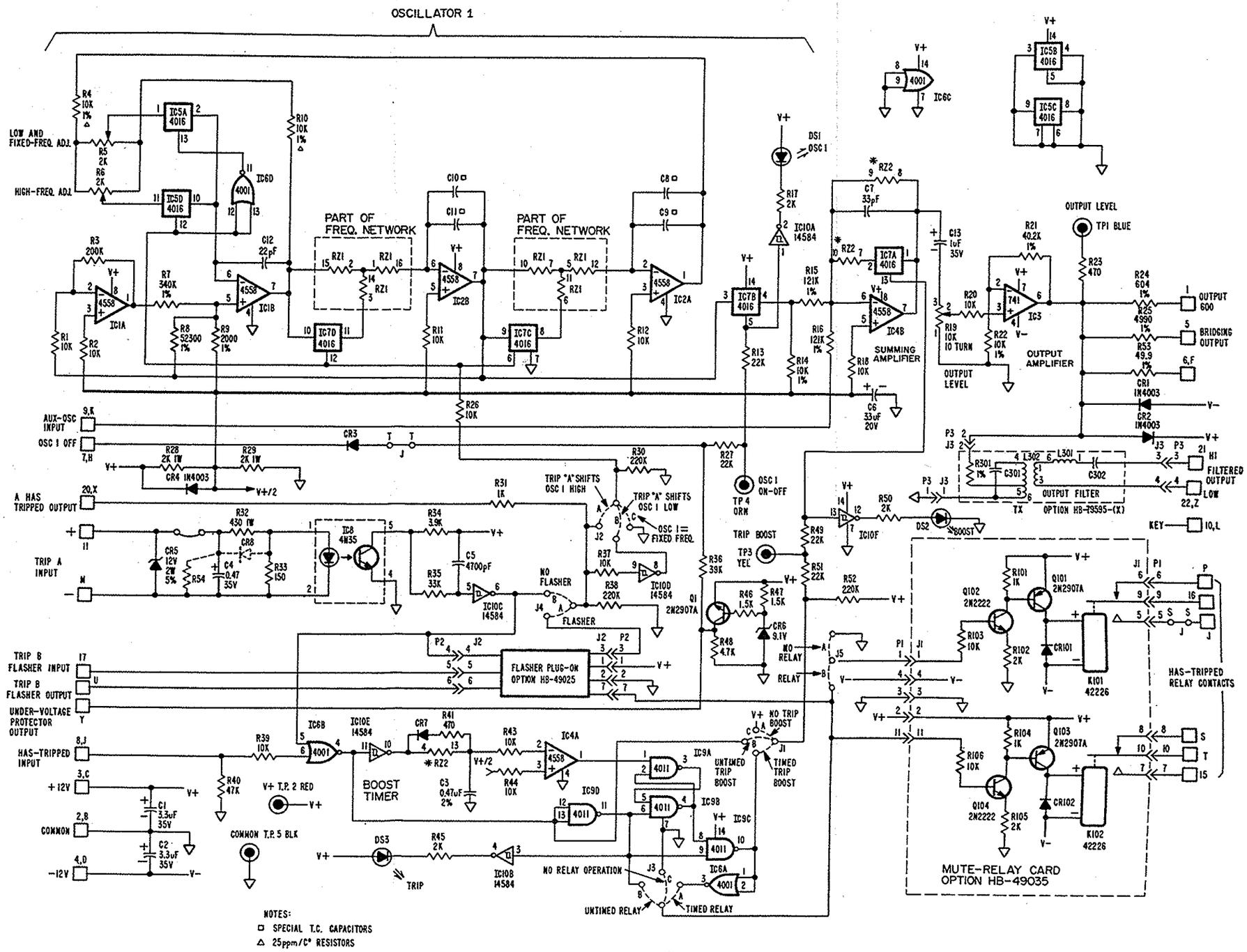


Figure 2.3. Schematic of circuit,
Model 67 MBB TRANS, with output filter and mute-relay option.

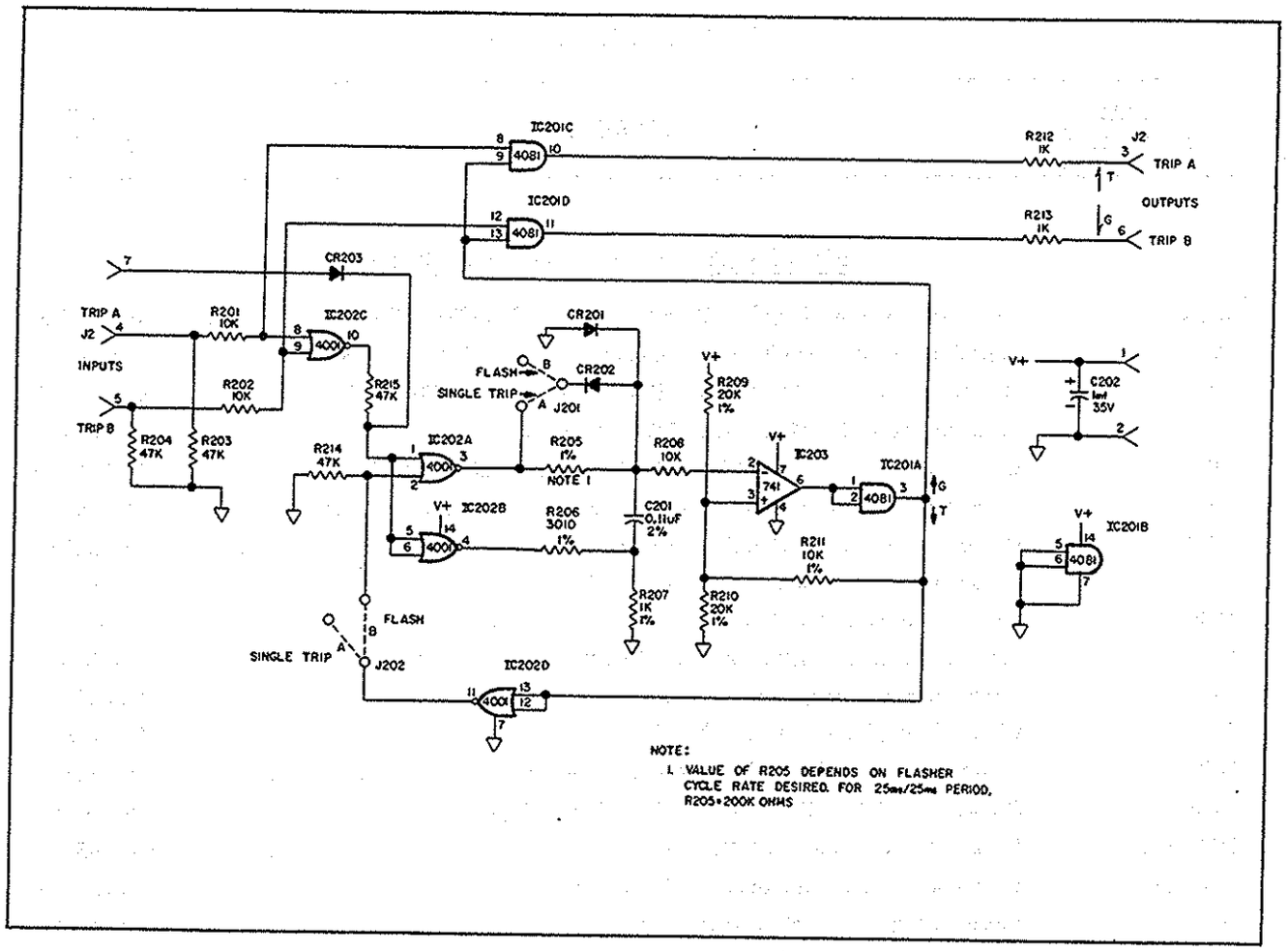


Figure 2.4. Schematic of circuit of flasher HB-49025.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 67 MBB Transmitter, Assembly HB-49020	
C1, 2	Capacitor, tantalum, 3.3μF, 20%, 35V, Kemet T322C335M035AS, or eq.	H-1007-1260
C3	Capacitor, metallized polycarbonate, 0.47μF, 2%, 100V, Wesco 32 MPC, or eq.	H-1007-971
C4	Capacitor, tantalum, 0.47μF, 10%, 35V, Kemet T322A474K035AS	H-1007-511
C5	Capacitor, poly., 0.0047μF, 2%, 100V, Wesco 32P, or eq.	H-5115-19
C6	Capacitor, tantalum, 33μF, 20%, 20V, Kemet T310C336M020AS, or eq.	H-1007-1161
C7	Capacitor, dipped mica, 33pF, 5%, 500V, Electromotive DM-15, or eq.	HA-16511
C8, 10	Capacitor, dipped mica, 0.002μF, 2%, 500V, Electromotive DM-19, or eq.	HA-16222
C9, 11	Capacitor, polypropolene, 510pF, 2.5%, 160V, Siemens B33063, or eq.	H-1007-1279
C12	Capacitor, dipped mica, 22pF, 5%, 500V, Electromotive DM-15, or eq.	H-1080-325
C13	Capacitor, tantalum, 1μF, 20%, 35V, Kemet T322B105M035AS, or eq.	H-1007-496
CR1, 2, 4	Diode, silicon, 1 amp, Type 1N4003	HA-30769
CR3, 7	Diode, silicon, Type 1N914B/1N4448	HA-26482
CR5	Diode, zener, 12V, 5%, 2W, Dickson 2EZ1205, or eq.	HA-35319
CR6	Diode, zener, 9.1V, 5%, 400mW, Fairchild 1N960B, or eq.	HA-41014
DS1, 2, 3	Lamp, LED, Dialight 550-0102, or eq.	HA-39568
IC1, 2, 4	Dual, linear, opamp, Raytheon RC4558NB, or eq.	H-0620-129
IC3	Linear opamp, National LM741CN, or eq.	H-0620-52
IC5, 7	Quad, bilateral switch, RCA CD4016AE, or eq.	H-0615-15
IC6	Quad, 2-input NOR gate, RCA, CD4001AE, or eq.	H-0615-3
IC8	Opto-isolator, Gen. Elec. 4N35, or eq.	HA-47104
IC9	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC10	Hex Schmitt trigger, Motorola MC14584CP, or eq.	H-0615-60
J1-5	Bar,shorting, single	HA-42904
Q1	Transistor, silicon, PNP, Type 2N2907A	HA-37439
R1-3, 11-13, 17, 18, 20, 23, 26, 27, 30, 31, 33-41, 43-52	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
R5, 6	Resistor, variable, metal-film, 2K, 10%, 0.5W, Bourns, Inc., 3339H-1-202	HA-90359
R7-9, 14-16, 21, 22, 24, 25, 28, 29, 53	Resistor, metal-film, 1%, 0.125W, value on schematic, Type RN55D, RFL Spec HA-38301	H-1510-(xxx)
R4, 10	Resistor, metal-film, 10K, 1%, 0.1W, Type RN55E, RFL Spec HA-38302	H-1510-1995
R19	Resistor, variable, metal-film, 10K, 10%, 0.75W, Helipot 79PR10K, or eq.	HA-39539
R32	Resistor, fixed, composition, 430 ohms, 5%, 1W, Allen Bradley GB, or eq.	H-1009-258
RZ1	Frequency-determining network for transmitter, Select from Table 1.1.	HB-79610-(X)
RZ2	Level-setting network for transmitter. Select from Table 1.3	HB-92967-(X)
———	Optional Output-Filter Assy., see Table 1.1	HB-79595-(X)
———	Schematic (Figure 2.3)	HE-49024

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Optional Mute Relay, Assembly HB-49035	
CR101, 102	Diode, silicon, Type 1N914B/1N4448	HA-26482
K101, 102	Relay, mercury-wetted contacts, single side stable Form-C, Adams and Westlake AWCH-16161-1, or eq.	HA-26901
Q101, 103	Transistor, silicon, PNP, Type 2N2907A	HA-37439
Q102, 104	Transistor, silicon, NPN, Type 2N2222A	HA-37445
R101-106	Resistor, fixed, composition, 5%, 0.25W, value on schematic, Allen Bradley CB, or eq.	H-1009-(XXX)
	Schematic, see insert in Figure 2.3	
	Optional Flasher, Assembly HB-49025	
C201	Capacitor, metallized polycarbonate, 0.11μF, 2%, 200V, Wesco 32MPC, or eq.	H-1007-1178
C202	Capacitor, tantalum, 1μF, 20%, 35V, Kemet T322B105M035AS, or eq.	H-1007-496
CR201, 202, 203	Diode, silicon, Type 1N914B/1N4448	HA-26482
IC201	Quad, 2-input AND gate, RCA CD4081BE, or eq.	H-0615-31
IC202	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC203	Linear, opamp, National LM741CN, or eq.	H-0620-52
R201-204, R208, R212-214	Resistor, fixed, composition, 5%, 0.25W, value on schematic, Allen Bradley CB, or eq.	H-1009-(XXX)
R205-207, 209-211	Resistor, metal-film, 1%, 0.125W, value on schematic, Type RN55D, RFL Spec HA-38301	H-1510(XXX)
——	Schematic (Figure 2.4)	HB-49029
	Optional Trans Filter, HB-79595-X	
L302	Tuned transformer, factory select	HB-55961-(xxx)
L301	Tuned coil, factory select	HB-55998-(xxx)
C302	Capacitor, poly., 2%, Wesco 32P or eq.	H-5115-(xxx)
C301	Capacitor, poly., 2%, Wesco 32P or eq.	H-5115-(xxx)
R301	Resistor, metal film 1%, Type RN55D	H-1510-(xxx)
	Schematic, see insert in Figure 2.3	

Auxiliary Oscillator, Model 67 MBB AUX OSC

PURPOSE

The auxiliary oscillator is provided to complement the function of the oscillator in the transmitter by making a multiplicity of trip signals available at different frequencies. It also provides a second trip-input circuit, designated as Trip-B Input, which is optically isolated and identical to that described for Trip A on the transmitter.

The logic circuits of the auxiliary oscillator may be used to control the on-off condition of Oscillator 1 on the transmitter module. In this mode, Oscillator 1 is used only to generate a guard-frequency signal, while Oscillators 2, 3, and 4 are used for trip signals.

Trip signals from the auxiliary oscillator are combined and fed to the summing and output amplifiers of the transmitter. Trip boost may be applied, at the transmitter, if required.

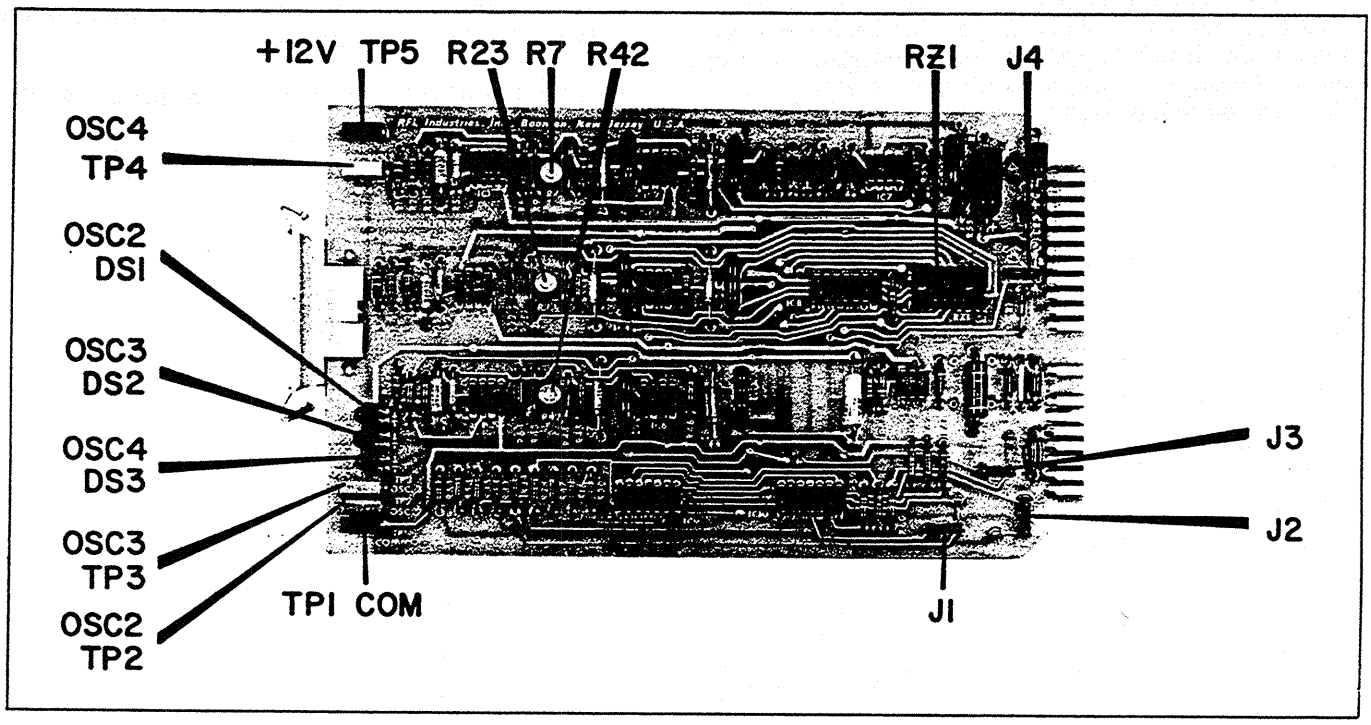


Figure 3.1. Model 67 MBB Auxiliary Oscillator.

CIRCUIT THEORY

Oscillator

The auxiliary-oscillator module uses three active-filter oscillators, designated Oscillators 2, 3, and 4. Oscillator 1 is in the transmitter. Only Oscillator 2 of the three identical circuits is described. The circuit is shown as Figure 3.2.

The active elements of Oscillator 2 are the two integrators, IC2A and IC2B, and feedback amplifier IC1. The oscillator is free-running at a frequency determined by elements 8-9 and 7-10 of RZ1, and by capacitors C15 through C18. The paralleled capacitors have been selected to minimize their temperature coefficients. Frequency of oscillation is set, in this oscillator, by selecting plug-in network RZ1 with proper resistance for the desired frequency. The frequency of oscillation is

$$f = \frac{1}{2\pi RC},$$

where R is the input resistance and C the capacitance of the two identical integrators. Frequency is trimmed by adjusting R7, which is connected in the feedback path. The output signal is taken from the output of the first integrator, at IC2A-1.

Output signals from the three oscillators are passed through three, parallel bilateral switches, IC8D, IC8A, and IC8C, and they are summed at the input of amplifier IC7A. The composite output of this amplifier passes through switch IC8B, where it is controlled by the logic signal from the undervoltage protection circuit in the transmitter.

IC7B is arranged to provide bias voltage, equal to one-half the power-supply voltage, to the three oscillators and to the output amplifier.

Trip-B Input

The input circuit for Trip B is optically isolated and identical in operation to the Trip-A input of the transmitter. Reference may be made to the discussion of the transmitter's circuits for details of operation.

Logic Circuits

IC9 and IC10 are the active elements of the logic circuits. These perform numerous control functions, depending upon what trip signals are used and on how the four jumpers on the circuit card are positioned.

A trip-command signal from Trip-Input B appears as a logic high at IC9D-8. Depending upon the position of J3, it will key the auxiliary oscillator to trip either directly or through the flasher. In either event, the trip command appears as a logic low at IC9F-12 and as a high at IC10A-4. Then, depending upon the position of J1, it may be used to key Oscillator 3.

A Trip-A command signal, received from the transmitter at Terminal 20, may be used to gate Oscillator 1, on the transmitter, depending on the position of J4. This signal also appears as a logic low at IC9E-10, from where it can be used to key Oscillator 2 to trip through IC10A and gate IC8D. Simultaneously, and provided there is a trip command from Input B, this logic low will combine, at the two inputs of IC10C, with a logic low caused by a command from Input B. Through J2, these two, in combination, can key Oscillator 4 through gate IC8C to generate a trip signal.

DS1, 2, and 3 indicate when Oscillators 2, 3, and 4, respectively, are operating.

Functions of the four jumpers are summarized in Table 1.5.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 67 MBB Auxiliary Oscillator, Assembly HB-49040	
C1	Capacitor, tantalum, 3.3μF, 20%, 35V, Kemet T322C335M035AS, or eq.	H-1007-1260
C2	Not used	
C3	Capacitor, tantalum, 0.47μF, 10%, 35V, Kemet T322A474K035AS, or eq.	H-1007-511
C4	Capacitor, polystyrene, 0.0047μF, 2%, 100V, Wesco 32P, or eq.	H-5115-19
C5	Capacitor, dipped mica, 0.001μF, 2%, 500V, Electromotive DM-19, or eq.	H-1080-286
C6	Capacitor, tantalum, 33μF, 20%, 20V, Kemet T310C336M020AS, or eq.	H-1007-1161
C7, 8, 11, 12, 15, 16	Capacitor, polypropolene, 510pF, 2.5%, 160V, Siemens B33063, or eq.	H-1007-1279
C9, 10, 13, 14, 17, 18	Capacitor, dipped mica, 0.002μF, 2%, 500V, Electromotive DM-19, or eq.	HA-16222
C19	Capacitor, dipped mica, 33pF, 5%, 500V, Electromotive DM-15, or eq.	HA-16511
CR1	Diode, silicon, Type 1N914B/1N4448	HA-26482
CR2	Diode, zener, 12V, 5%, 2W, Dickson 2EZ12D5, or eq.	HA-35319
CR3	Diode, rectifier, 1 amp., Type 1N4003	HA-30769
DS1, 2, 3	Lamp, LED, Dialight 550-0102, or eq.	HA-39568
IC1-7	Linear opamp., Raytheon RC4558NB, or eq.	H-0620-129
IC8	Quad bilateral switch, RCA CD4016AE, or eq.	H-0615-15
IC9	Hex Schmitt trigger, Motorola MC14584CP, or eq.	H-0615-60
IC10	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC11	Opto-isolator, Gen. Elec. 4N35, or eq.	HA-47104
J1-4	Bar, shorting, single	HA-42904
R1, 2, 3, 10, 11, 14, 16-19, 26, 27, 28, 30-35, 37, 38, 39, 45, 46, 47, 50-56, 59-63	Resistor, fixed composition, 5%, 0.25W, value on schematic, Allen Bradley CB, or eq.	H-1009-(XXX)
R4, 5, 6, 12, 13, 20, 21, 22, 29, 36, 40, 41, 57, 58, 64	Resistor, metal-film, 1%, 0.125W, value on schematic, Type RN55D, RFL Spec HA-38301	H-1510-(XXX)
R7, 23, 42	Resistor, variable, metal-film, 1K, 30%, 0.5W, Helipot 62PR1K, or eq.	HA-21776
R8, 9, 15, 24, 25, 43, 44	Resistor, metal-film, 10K, 1%, 0.1W, Type RN55E, RFL Spec HA-38302	H-1510-1995
R48	Resistor, fixed, composition, 430 ohms, 5%, 1.0W, Allen Bradley CB, or eq.	H-1009-25E
RZ1	Frequency-determining network, for auxiliary oscillator, Select from	HB-79615-(X)
——	Schematic (Figure 3.2)	HD-49044

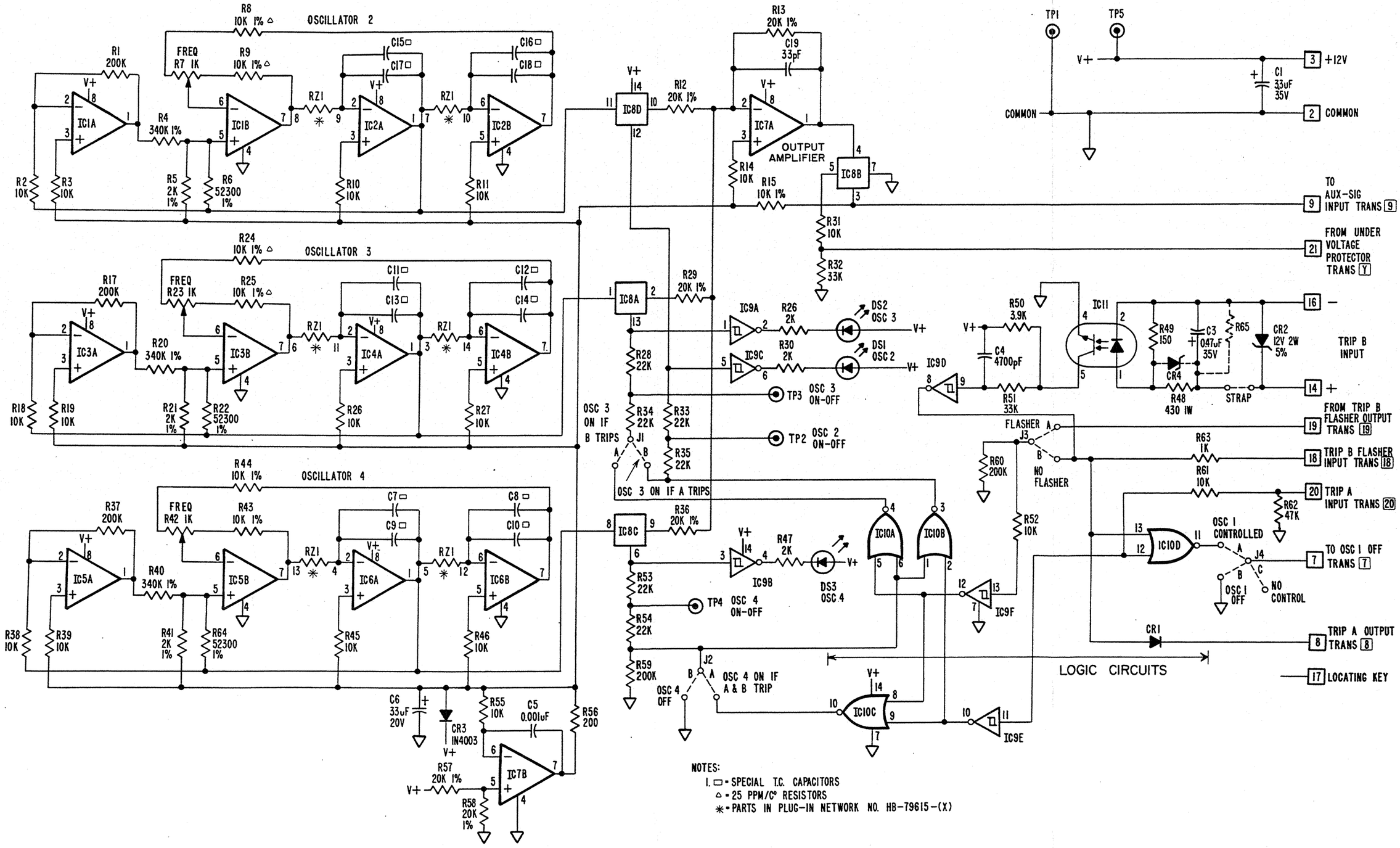


Figure 3.2. Schematic of circuit, Model 67 MBB Auxiliary Oscillator.

Receiver, Model 67 MBB REC

DESCRIPTION

The Model 67 MBB Receiver is the receiving component in the Series 6710 Protective Relaying System. At any receiving terminal at least two receivers will be required, one to receive at guard frequency, the other at trip frequency. Depending upon the complexity of the system, as when two or more trip frequencies are used, more than two receivers may be needed.

Receivers are usually operated at signal frequencies between 1000 and 3300 Hz, although operation may be extended as high as 10 kHz when the communication facility permits. Maximum input sensitivity is −40 dBm. Dynamic range is adjustable by choice of a plug-in network. Though usually set at 20 dB, the dynamic range can be as great as 30 dB.

The main components of the receiver are a plug-in bandpass filter used at the input, signal-conditioning and rectifying circuits, a level-limit detector, and a reference comparator which compares incoming-signal level with that of a reference signal from Terminal 19 of the other receiver in the system, either guard or trip as the case may be.

A choice of resistors, in those elements of plug-in resistor RZ1 which are associated with the reference comparator, makes it possible to weight the ratios of signal levels accepted. The reference comparator, whose operation is detailed later in this section, requires a wide difference in levels to exist between the incoming signal and the reference signal before its output changes state. This enhances the security of the system by creating a dead zone in which signal level may fluctuate without accepting the change as valid data. The ability to change these resistors permits the designer to choose among security, dependability, and dynamic range according to the needs of his system.

For example, the receiver can be given a wide dynamic range, as would be necessary when the communication link is a powerline-carrier system where signal levels reduce significantly during a fault. In such a system, security is traded for dependability. On the other hand, when the communication line is a microwave system or telephone line, where signal levels are closely controlled and not affected by a powerline fault, the dynamic range can be reduced considerably to enhance the security of the system while still retaining a satisfactory level of dependability.

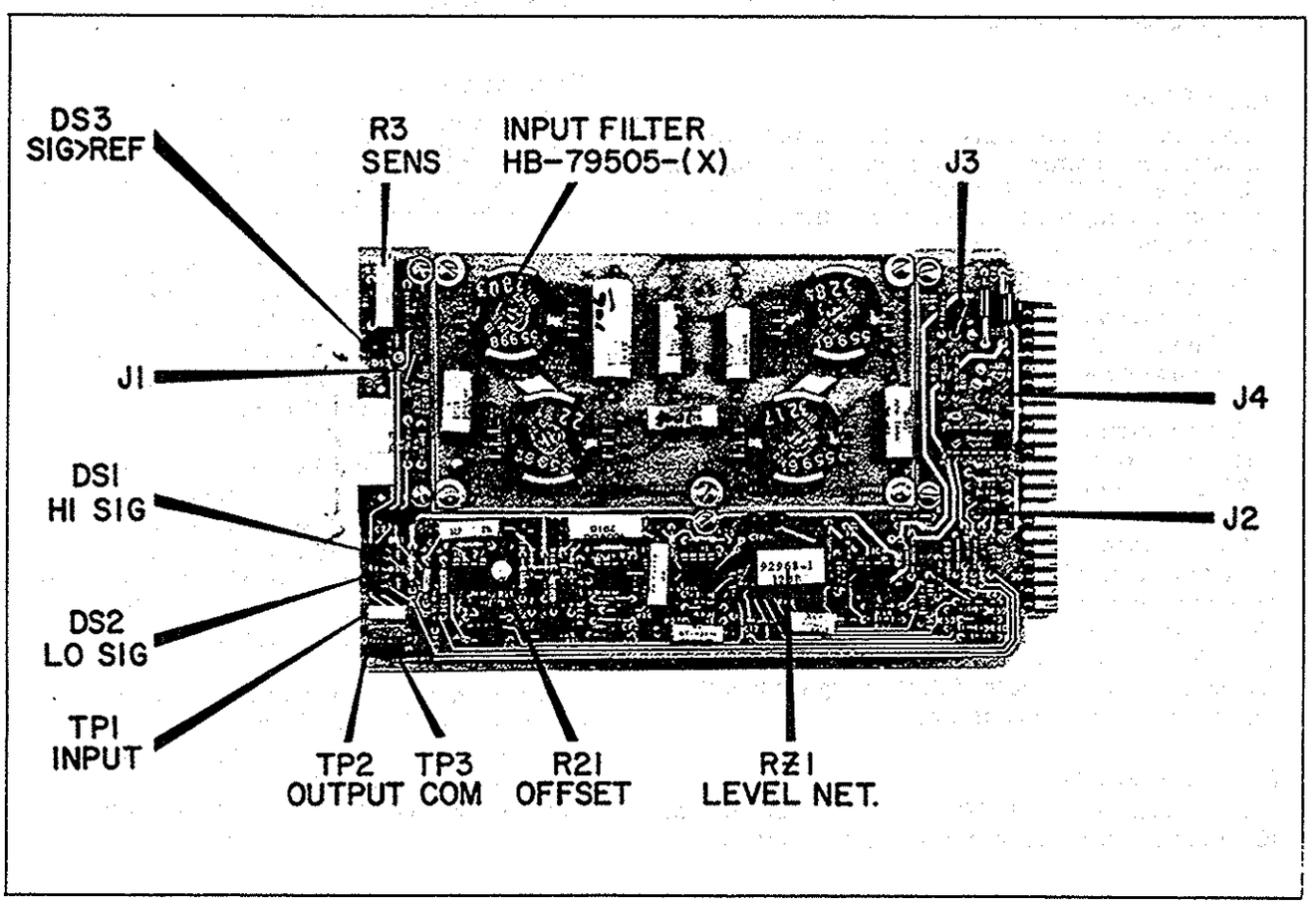


Figure 4.1. Model 67 MBB Receiver.

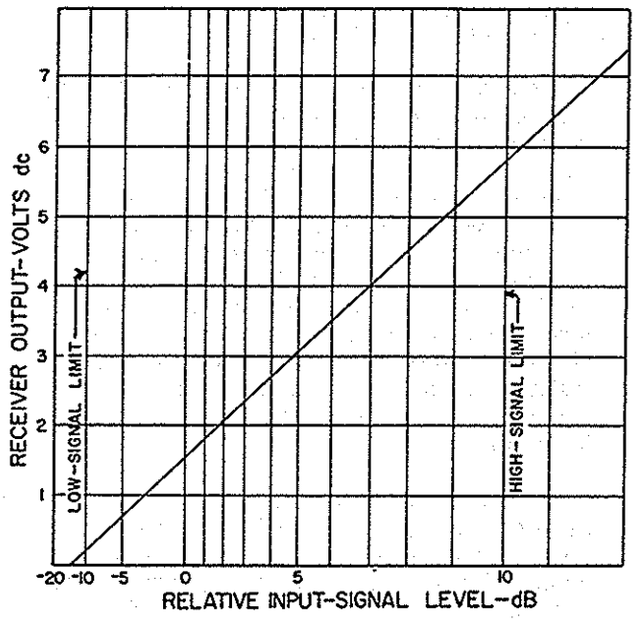


Figure 4.2. DC output level of receiver vs. input level of reference signal for 20-dB weighting.

CIRCUIT DETAILS

The incoming signal is applied to a passive bandpass filter, Figure 4.3, which is either a four-, five-, or six-coil Cauer (elliptical) filter. The filter assembly is selected from Table 1.1, according to the bandpass frequency required.

Input Circuit

From the input filter, the signal is passed through the sensitivity control, R1, to a two-stage amplifier using IC1B and IC1A. The gain of IC1B is set by the position of Jumper J1. At Position A the gain is 20 dB. At Position B it is unity.

The gain of IC1A is set by the value of element 1-16 in network RZ1, which is selected from Table 1.3. The output of IC1A is available at Terminal 22 of the edge connector.

The ac output signal from IC1A is full-wave rectified in the operational rectifier based on IC2A and IC2B as its active elements. IC2B is an impedance buffer, and its inverting input is used, also, to cancel voltage offsets in the circuit by adjusting R21. Simultaneously, IC2B, R22, and C7 provide one pole of a four-pole, active lowpass filter which also includes IC3B. The cutoff frequency of this filter is typically 900 Hz, and its output is a filtered dc signal which is fed to the inputs of IC4B, a high-limit detector, and IC4A, a low-limit detector.

Limit Detectors

The upper limit of IC4B, and the lower limit of IC4A are determined, respectively, by the values of elements 8-9 and 7-10 of RZ1, the plug-in network. Typically, the upper limit is 5 volts and the lower limit is 500 mV, which gives a dynamic range of 20 dB. Under normal operating conditions, the signal from the lowpass filter is within this range, the outputs of the two comparators are high, and neither DS1 nor DS2 is illuminated.

Reference Comparator

The reference comparator, IC3A, compares the level of the received signal against the level of the sum of the three reference inputs at Terminals 18, 20, and 21 of the edge connector. The summing junction is at the non-inverting input. When the level of the incoming signal is greater than the summed reference, the output of IC3A will be low. After passing through IC5D, this will appear as a high at the output at Terminal 16, SIG REF. At the same time, the output of IC5C will be low and will illuminate DS3 to show that the signal level is greater-than the reference level, a normal condition.

The signal level from the lowpass filter, and the three reference-signal levels, all can be weighted by selection of the four elements of RZ1, which forms a voltage divider for these signals, as shown.

The rectified signal output from the active lowpass filter is also made available, for use elsewhere in the system, at Terminal 19.

Dynamic Range

The receiver is normally adjusted to deliver a dc output signal of 1.6 volts, at Terminal 19, when supplied with the nominal level of signal in the system in which it is operated.

Figure 4.2 shows the dc output signal from the receiver as a function of input-signal level. On this plot, 0 dB corresponds to the 1.6-volt output level of the receiver, and the alarm-level points denote the levels for low- and high-signal alarms, respectively, over a range of about 20 dB.

It will be observed that the nominal output-signal level of the receiver can be changed from 1.6 volts to some other value by adjustment of the SENSITIVITY control, R1. For example, if the receiver is set for a nominal output voltage of 2.8 volts, then the dynamic range of the system extends from 5 to −15 dB, which is still a 20-dB range.

The standard plug-in network at position RZ1, listed in Table 1.3, provides for a ratio of 12 dB between levels of guard and trip signals, and for a dynamic range extending from 10 to −10 dB. For other signal-weighting ratios and for other dynamic ranges, it is recommended that RFL be contacted

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 67 MBB Receiver, Assembly HB-49030	
C1, 3	Capacitor, tantalum, 2.2μF, 20%, 25V, Kemet T322B225M025AS, or eq.	H-1007-645
C2, 4, 6	Capacitor, dipped mica, 15pF, 5%, 500V, Electromotive DM-15, or eq.	HA-16506
C5	Capacitor, tantalum, 1μF, 20%, 35V, Kemet T322B105M035AS, or eq.	H-1007-496
C7	Capacitor, poly., 0.00865μF, 2%, 100V, Wesco 32P, or eq.	H-5115-32
C8	Capacitor, poly., 0.0375μF, 2%, 100V, Wesco 32P, or eq.	H-5115-62
C9	Capacitor, poly., 0.0075μF, 2%, 100V, Wesco 32P, or eq.	H-5115-29
C10	Capacitor, dipped mica, 510pF, 2%, 500V, Electromotive DM-19, or eq.	HA-16634
C11	Capacitor, poly., 0.001μF, 2%, 400V, F-Dync PST-11, or eq.	H-5115-274
C12	Capacitor, poly., 0.011μF, 2%, 100V, Wesco 32P, or eq.	H-5115-37
C13, 14	Capacitor, tantalum, 3.3μF, 20%, 35V, Kemet T322C335M035AS, or eq.	H-1007-1260
CR1-5	Diode, silicon, Type 1N914B/1N4448	HA-26482
DS1, 2, 3	Lamp, LED, Opcoa ORL-1, or eq.	HA-41518
IC1-4	Linear opamp., Raytheon RC4558NB, or eq.	H-0620-129
IC5	Hex Inverter/Buffer, RCA CD4049AE, or eq.	H-0615-7
J1-4	Bar, shorting, single	H-42904
R1, 5-8, 10, 11, 13-16, 18, 19, 20, 22-25, 29, 35, 41-43, 50, 51, 53, 54	Resistor, metal-film, 1%, 0.125W, value on schematic, Type RN55D, RFL Spec HA-38301	H-1510-(xxx)
R2, 4, 9, 12, 17, 26-28, 30-34, 36-40, 44-49, 52, 55	Resistor, fixed, composition, 5%, 0.25W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
R3	Resistor, variable, metal-film, 10K, 10%, 0.75W, Helipot 79PR10K, or eq.	HA-39539
R21	Resistor, variable, metal-film, 20K, 30%, 0.5W, Helipot 62PR20K, or eq.	HA-21778
RZ1	Weighting-ratio network, selected from Table 1.3	HB-92968-(xxx)
——	Input-Filter Assembly, See Table 1.1	HB-79505-(x)
——	Schematic (Figure 4.3)	HD-49034

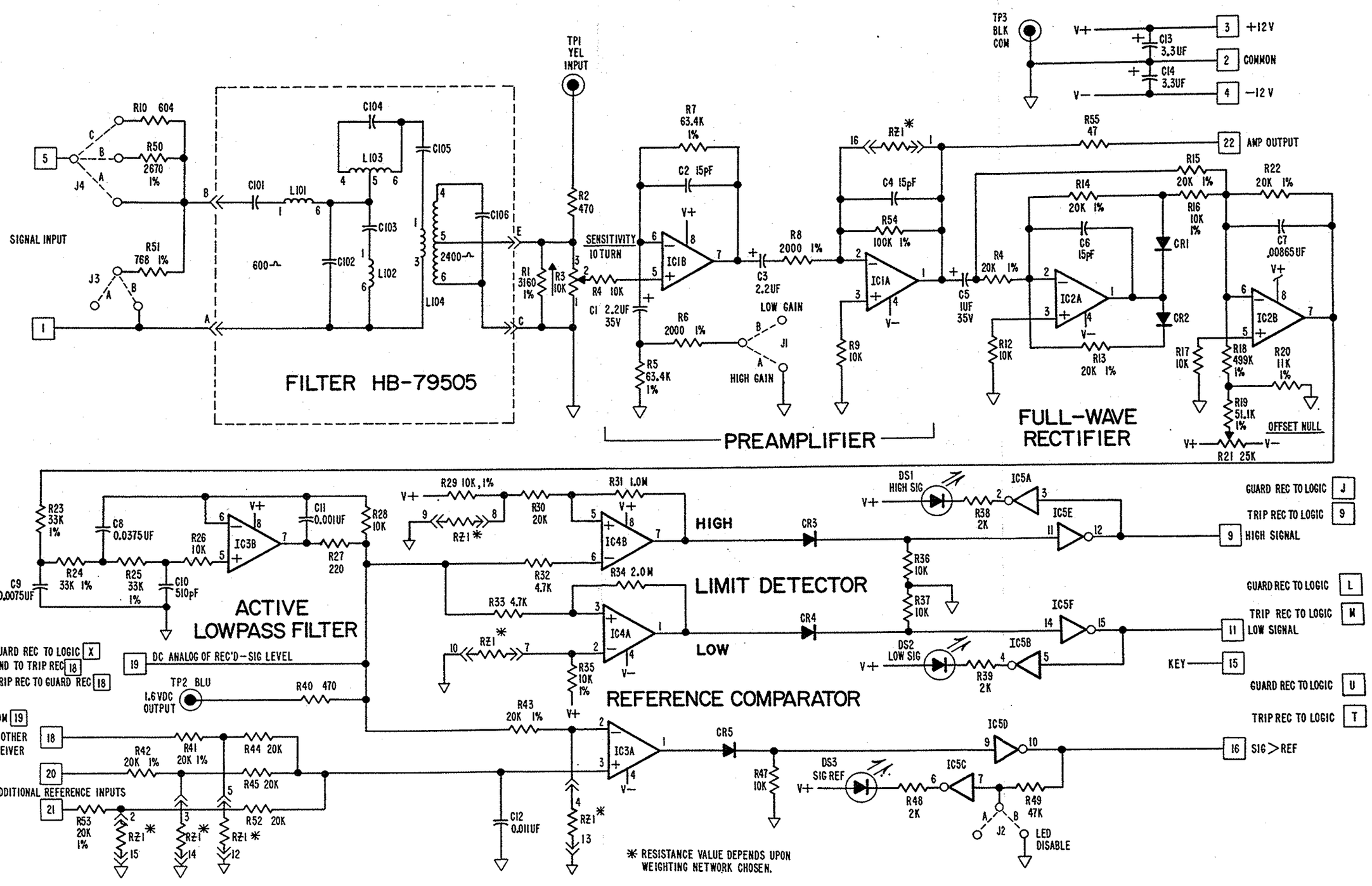


Figure 4.3. Schematic of circuit, Model 67 MBB Receiver.

Logic Circuit, Model 67 MBB LOGIC

GENERAL

The Model 67 MBB Logic Circuit provides the functions necessary to determine the status of the received signal and to qualify it as valid, or invalid, whether it be a guard signal or a trip signal. The logic circuit compares the level of one signal with that of the other, and checks timing and sequence of the signals before it releases a trip command. The module has all the circuits necessary to provide the following functions:

(a) valid guard- and trip-output signals
(b) return of guard cancels the trip-hold timer
(c) pre-trip and pre-guard timers
(d) valid-guard-before-trip timer
(e) valid-trip-after-guard timer
(f) alarm timer
(g) restore timer
(h) guard required before trip only on first trip
(i) trip-hold timer
(j) high-speed clear-channel tripping.

A block diagram of the logic circuits is shown as Figure 5.2.

CIRCUIT DETAILS

Trip-Detection Circuits

Detection of a trip signal starts at the trip receiver, in which the reference comparator compares the level of the trip signal received with the level of the signal received by the guard receiver. The plug-in resistor network, RZ1, Figure 4.3, on both receivers is selected so that the trip-signal level normally must be at least 12 dB greater than that of the guard signal for it to be accepted as a valid trip signal. The same test is applied to validate a guard signal.

In the following discussion of the passage of trip and guard signals through the logic circuits, the block diagram, Figure 5.2, and the timing diagram, Figure 5.3 will be helpful. In Figure 5.3, it is assumed that there is a quiet channel with no disturbances, that all signals are at normal level, and that guard signal has just been applied to an empty channel at time 0, at the left edge.

When the incoming trip signal has passed the level test, it appears at Terminal T, of the logic module as an input signal. Terminal 16 provides for the case where a second trip is required to generate a valid trip-output signal from the logic card. In such a case, the low source impedance of the source for the second trip will hold IC5B low until a logic high is received, so that the requirement is established that two logic-high signals must be at the inputs to IC5B for the logic card to release a trip-output signal.

In either case, the trip signal then appears at IC5C-8 as a logic one, where it must combine with the signal at IC5C-9, which is the second input to this AND gate. Pin 9 of IC5C will be at a logic high

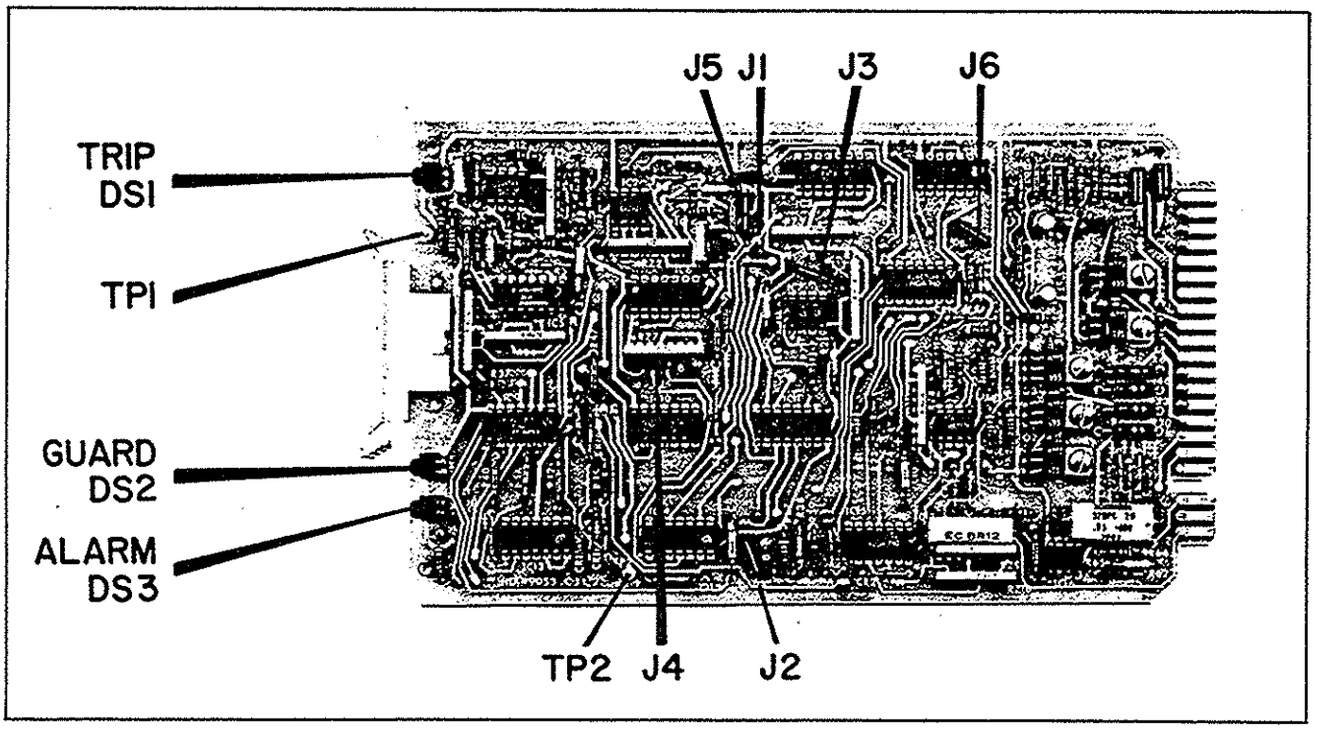


Figure 5.1. Model 67 MBB LOGIC.

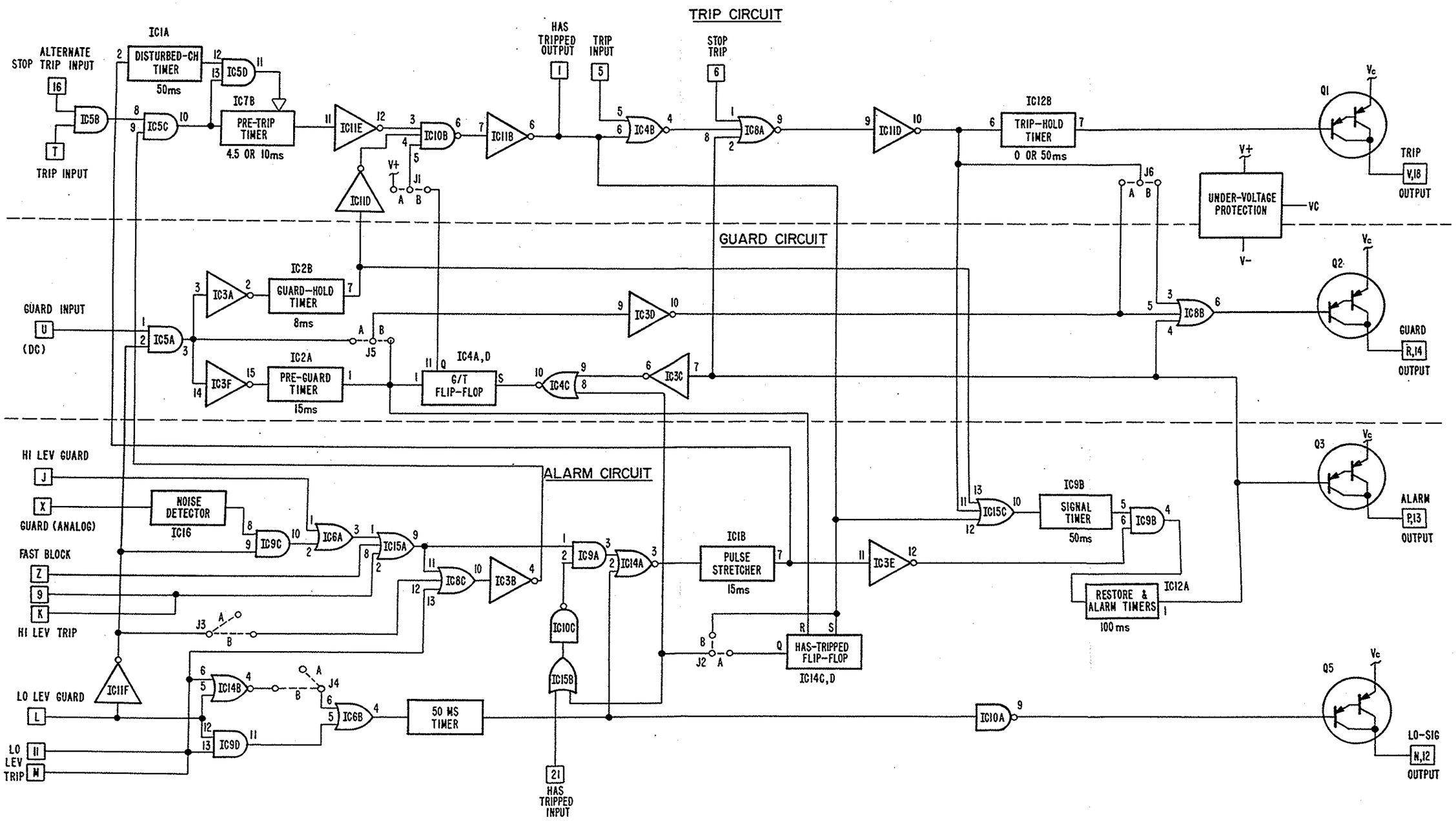


Figure 5.2. Block diagram of logic circuits.

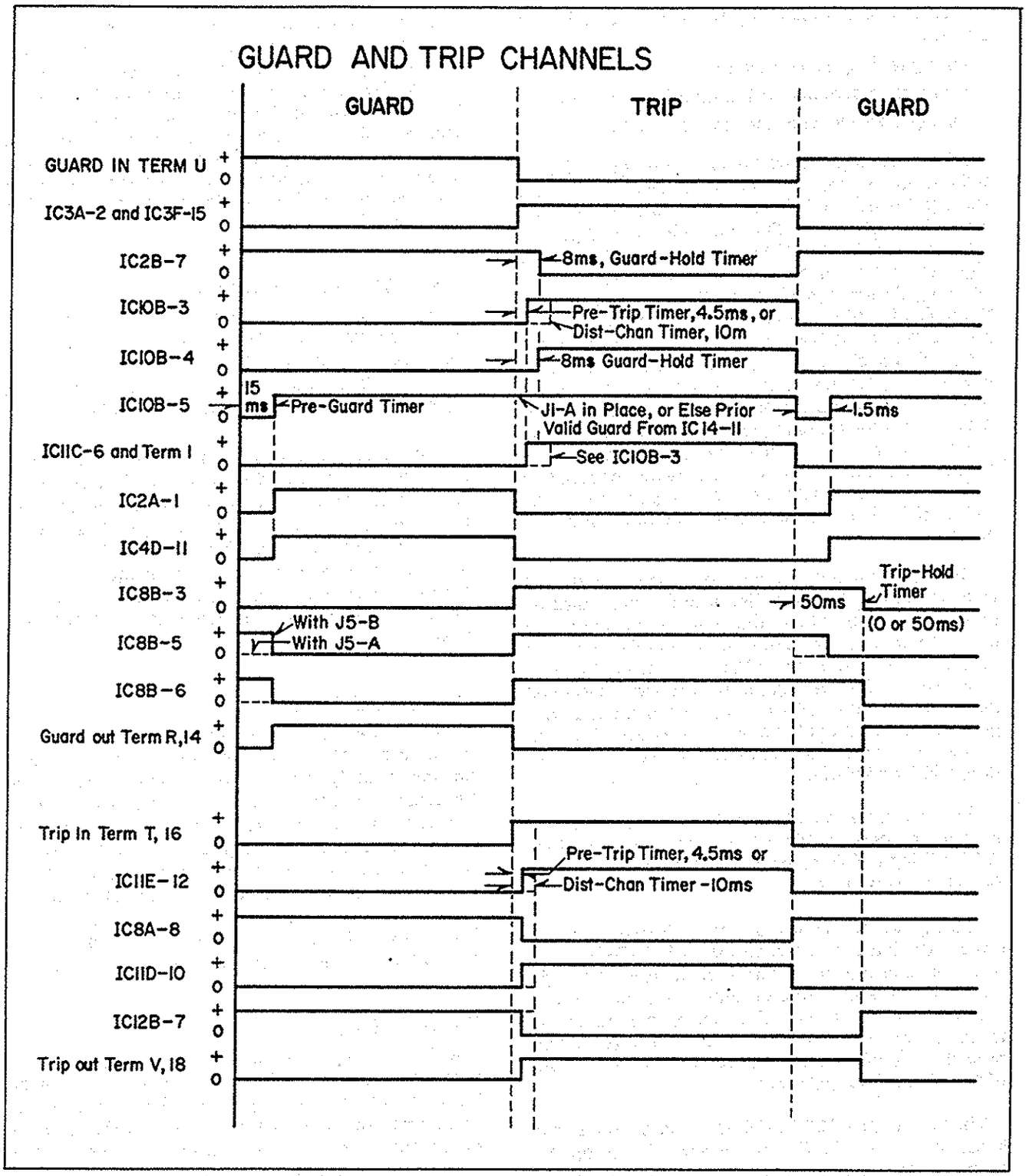


Figure 5.3. Timing diagram showing circuit path for guard and trip conditions. This diagram assumes a quiet channel, no disturbances, and all signals at normal level.

unless any of the following undesired conditions is present:

(a) a guard signal is present,

(b) noise is detected in the guard channel, or

(c) trip-signal level is too low, or absent.

After the trip signal passes through IC5C, it follows either of two paths. At IC5D-13,it will pass through the gate only if the disturbed-channel timer, IC1A, has not been activated, which would place a logic low at IC5D-12. When both inputs of IC5D are high, the period of the pre-trip timer is reduced by charging C4 through R9, as well as through R5 from the logic high at IC5C-10. The shorter period of the pre-trip timer establishes the requirement that the received trip signal persist for at least 4.5 ms at IC5C-10. If, however, the disturbed-channel timer has been activated by any of the foregoing three conditions, then C4 charges only through R5 and the pre-trip timer requires that the received trip signal persist for at least 10 ms before being accepted as valid at the input of IC7B, and this appears as a logic high at IC11E, which signals the detection of an acceptable trip signal.

The trip signal now appears at IC10B-3, and for it to pass through the gate Pins 4 and 5 must also be high. For Pin 4 to be high, the guard signal must have disappeared from the output of the guard receiver for at least 8 ms, as determined by the guard-hold timer, IC2B. For Pin 5 to be high, either Jumper J1-A must be in place, or else, with Jumper J1-B in place a valid guard condition must have been previously detected by the pre-guard timer, IC2A, and held by the flip-flop, IC4A and IC4D.

With all tests satisfied at the three inputs of IC10B, its output, Pin 6, will go low and drive IC11B-6 high. This signal is available at Terminal 1 of the edge connector.

The trip signal will also appear at IC4B-6 and will drive IC8A-8 low and the output of IC11D-10 high. It is assumed that Input Pin 2 of IC8A is at a logic low, and this will be true provided that no abnormal condition, such as excessive noise, low trip-signal level, or incorrect sequence of trip after guard prevails, any of which would come from the output of the alarm timer, IC12A-1.

The logic high at IC11D-10 immediately drives the input high at IC12B-6. The output of this opamp then goes low and causes Q1 to become conducting and indicate a valid trip at Terminals V and 18 on the edge connector. Simultaneously, DS1 will be illuminated.

R24, R70, and C8 comprise the trip-hold timer. When IC11D-10 goes low, as at the discontinuance of a trip signal, C8 will discharge through R24 and R70, and thus hold Pin 6 of IC12B momentarily high so that the trip-output signal persists momentarily after removal of the trip signal. The input to IC12B also has a choice of two jumpers associated with it. With Jumper J6-A (guard present) in place, as soon as a valid guard condition has been-detected the action of the trip-hold timer will be cancelled and the trip output also will be immediately cancelled. With Jumper J6-B (trip present) in place, then in the presence of a valid guard signal the trip output is not cancelled, nor is guard output from Terminals R and 14 permitted until the period of the trip-hold timer has expired.

Guard-Detection Circuits

Detection of a guard signal commences at the guard receiver, and after satisfying the signal-level test requiring that guard-signal level is greater than trip-signal level, the guard signal is released to the logic card where it appears at Terminal U.

The received guard signal will drive the output of IC5A high, providing that Input Pin 2 is also high. And Pin 2 will be high provided that at least the minimum permissible level of guard signal is detected at the receiver. Typically, this level is 500 mV, and a logic low signifying adequate level is received at Terminal L of the logic card. The output of IC5A drives three inverters, IC3A, IC3D, and IC3F.

Guard-Hold Timer

IC3A is the input to the guard-hold timer, and in the presence of a guard signal its output goes low and immediately forces the output of IC2B high. This becomes a logic low at IC11A-2 which appears as a low at one input of IC10B and thus prevents a trip in the presence of a guard signal. Pin 4 of IC10B will return to a logic high only after the period of the guard-hold timer, 8 ms, has expired following the removal of a guard-signal input to the logic circuit. The output of the guard-hold timer, IC2B-7, also drives the input to the signal timer, IC15C-13.

Pre-Guard Timer

IC3F is the input to the pre-guard timer, which requires that a logic high remains at IC3F-14 for at least 15 ms for the output at IC2A-1 to go high. Once this output goes high, it means that a valid guard condition has been established through the presence of uninterrupted guard signal for the required period. The period of the pre-guard timer is set by R18 and C7.

G/T Flip-Flop

The output of IC2A drives IC4A-1, which is the set input to the G/T (guard-before-trip) flip-flop consisting of IC4A and IC4D. The high from IC2A-1 provides a logic high at IC4D-11, for we assume that the reset input, at IC4D-13 is low. The high at

IC4D-11 provides a high at IC10B-5, and thus establishes the requirement that a valid guard signal must precede a trip signal. If this requirement is not desired, the jumper at IC10B-5, J1, must be at Position A.

The logic high at IC2A-1 also drives another flip-flop, IC14C and IC14D. This flip-flop permits one to establish the requirement that only the first trip need be preceded by a valid guard signal, and that this requirement is not demanded for acceptance of subsequent trip signals, so as to provide for the event that a valid trip was subsequently lost momentarily due to loss of carrier. The choice is made with J2.

Guard-Output Signal

A guard-output signal appears as a logic high, at Terminals R and 14, whenever Q2 becomes conducting, and this occurs when the output of IC8B, at Pin 6, becomes low. This requires that all three inputs of IC8B be low. Pin 3 normally is low either because no trip is present or because the trip-hold timer has completed its period. Pin 4 will be low so long as no abnormal condition causes a logic high from IC12A-1. Pin 5 will be low because of the inverted logic-high signal from IC3D-10, and the time at which Pin 3 will be low will be determined by which jumper is used at the input of IC3D.

If Jumper J5-A is chosen, a guard-output signal will appear at Terminals R and 14 immediately upon receipt of the receiver's guard-output signal, through IC5A. If Jumper J5-B is used, the guard-output signal from the logic card will appear only after the guard signal has been validated for 15 ms by the pre-guard timer, IC2A.

In either case, the presence of an accepted guard signal is signified by the illumination of DS2.

Blocking and Noise Detection

At Terminal X, the rectified-dc output signal from the guard receiver is sampled, and it is filtered with R63, R64, C12, and C13, after which it provides a dc reference at IC16A-2. The timing diagram, Figure 5.4, shows the sequence. The instantaneous dc signal is divided by R65 and R66, and it is applied to the other input terminal of opamp IC16A. When the instantaneous value of the signal jumps 1 dB higher than the average, at the input of IC16A, the output goes high to signal the presence of noise on the guard channel.

This noise signal is combined with inverted LO LEV GUARD at IC9C, with HI LEV GUARD at IC6A, and with HI LEV TRIP and FAST BLOCK at IC15A. If any of these abnormal conditions, including the noise at IC16A-1, is detected, IC15A-9 goes high. This is combined, in IC8C, with LO LEV TRIP and, if Jumper J3 is in Position B, with the inverse of LO LEV GUARD to drive IC8C-10 high. This high after inversion through IC3B, blocks passage of a trip signal from the input circuit by impressing a logic low at IC5C-9.

NOISE DETECTION AND TRIP BLOCKING

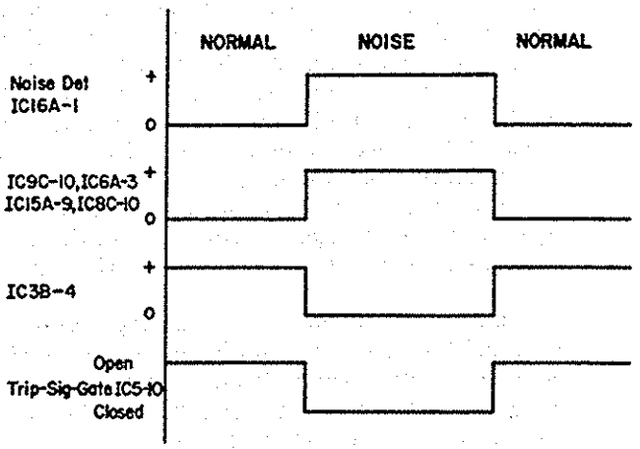


Figure 5.4. Timing diagram showing noise detection and resultant trip blocking.

IC15A-9 also provides a high input to IC9A-1. But if a trip has already been received through Terminal 21, IC15B, and inverted through IC10C, then IC9A-2 will be low and will prevent the blocking signal from making the output of IC9A high.

Low-Signal Timer and Alarm

Under normal-signal conditions, during either guard or trip, the logic level at one of either Terminal L or M will be low (normal signal level) while the other will be high (signal absent). Under these conditions, IC9D-11 is low, IC14B-4 is low, and these pass through IC6B and IC10A to place a high on the base of Q5 so that Terminals N and 12, driven by it, are not energized. The timing diagram, Figure 5.5, shows the sequence of events.

LOW-SIGNAL ALARM TIMING

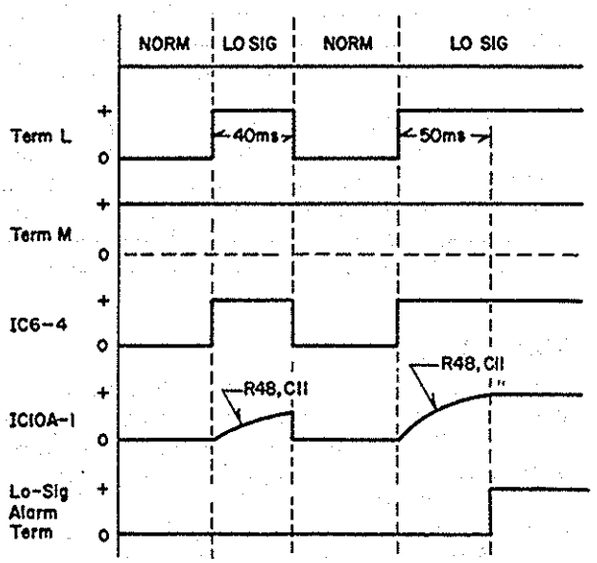


Figure 5.5. Timing diagram showing action of low-signal timer and response of alarm circuits.

Under abnormal (low-signal) conditions, both Terminals L and M will be high and this will move IC9D-11 high and a logic high will appear at IC6B-4. If this signal continues for 50 ms, or more, as determined by the time constant, R48 and C11, of the LO-SIG ALARM TIMER, then IC10A-9 goes low and causes Q5 to become conducting. This is the low-signal alarm which appears as a logic high at Terminals 12 and N, and which may be used either in its logic form or to energize a relay such as K3, the optional alarm relay available on the interface card.

Jumper J4-B provides for blocking the system, through IC14A, when both trip and guard signals are simultaneously present (logic lows at Terminals L and M), which is an abnormal condition. When J4-A is chosen, this function is defeated.

Pulse Stretcher

Either the low-signal condition, a high at IC6B-4, or a blocking signal from IC9A-3, will make IC14A-3 low, and this drives IC1B-7 high. IC1B, R11, and C5 form a pulse-stretcher circuit, so that even if the logic low from IC14A-3 is very short it will rapidly discharge C5 and hold the output from IC1B high for at least 15 ms. Figure 5.6 shows the sequence.

The logic high at IC1B-7 is applied to the disturbed-channel timer at IC1A-2, and a logic high will persist at that point for at least 50 ms, as set by R2 and C3, after the logic high representing the disturbed condition has been removed. The minimum time, therefore, for which the period of the pre-trip timer is increased to 10 ms is at least 60 ms, and could be longer if the disturbance persists.

Disturbed-Channel Timer

Under normal conditions, with a trip signal present, both inputs of IC5D are high, and so R9 is thereby connected in parallel with R5. These two paralleled resistors, together with C4, set the period of the pre-trip timer at 4.5 ms. See Figure 5.6.

With abnormal conditions, a logic high from IC1B-7 will drive the output of IC1A low. This will open gate IC5D and disconnect R9 from its parallel connection with R5. Thus, under disturbed-channel conditions, the time constant of the pre-trip timer becomes 10 ms, as set by R5 and C4 alone.

Signal Timer

The logic-high alarm signal at IC1B-7 is also inverted through IC3E and appears as a low at Pin 12 and at IC9B-6. The other input of IC9B, Pin 5, is connected to IC15C through a 50-ms signal timer. IC15C-10 will be low if neither a guard-hold signal (IC15C-13), a trip signal (Pin 12), nor a trip-hold signal (Pin 11) is present. If absence of guard or trip persists for more than 50 ms, the input to IC9B goes

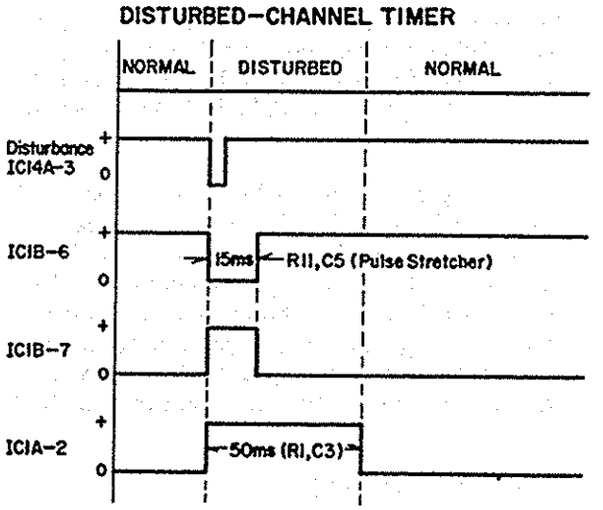


Figure 5.6. Timing diagram showing response of pulse stretcher and disturbed-channel timer to a disturbance.

low. Thus IC9B-4 will go low if a low is received from either the pulse stretcher or the signal timer. This represents an abnormal condition, as discussed in the following.

Alarm and Restore Timers

If the system is not in an alarm state, then IC12A-1 is low. See Figure 5.7. This logic low is inverted in IC11B and closes bilateral switch IC13C. R42, C10, and IC12A form the alarm timer, which has a period of about 100 ms. A low at IC9B-4 (abnormal condi-

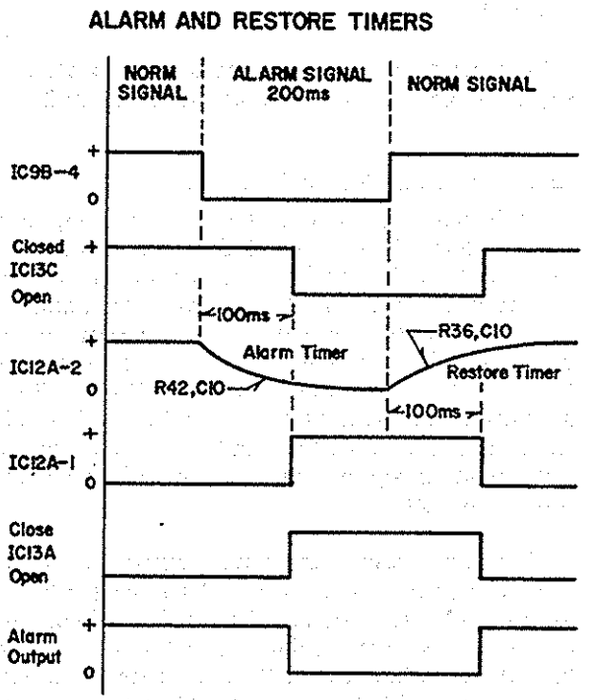


Figure 5.7. Timing diagram showing response of alarm and restore timers and alarm output to a disturbance.

tion)must last for at least 100 ms before IC12A-1 goes high to signal an alarm. When it does go high, IC13A becomes conducting and IC13C becomes open. The alarm timer is then effectively removed from the circuit and the restore timer, R36 and C10 takes control. Under this control, IC9B-4 must remain high (normal condition) for 100 ms before the alarm condition is removed.

Thus, the alarm circuit has two independent timers. When the system is not in alarm the alarm timer is connected and requires the abnormal condition to persist for 100 ms before signaling an alarm. Once the system is in alarm, the restore timer is connected and requires normal conditions to continue for 100 ms before clearing the alarm.

Alarm Functions

When the system goes into alarm, the logic high at IC12A-1 also illuminates DS3, to signify that the system is inoperative, and it turns off Q3 so that the alarm relay is de-energized.

The logic high at IC12A-1, which signifies an alarm, is also connected to IC8A-2, where it prevents a trip output, and to IC8B-4, where it prevents a guard output.

The logic high is also inverted by IC3C and appears as a low at IC4-9. If Jumper J2-B (guard-before-trip), at the output of IC14D, is used, then the absence of a trip signal will place the low (no trip) from IC11C-6 on IC4C-8. This, combined with the low from IC3C-6, will force IC4C-10 high and reset the G/T flip-flop, IC4A and IC4D. This puts a low from IC4D-11 on IC10B-5 through Jumper J1-B and prevents a trip.

When the guard signal returns, the G/T flip-flop is reset from the output of the pre-guard timer, IC2A-1. With Jumper J2-B in place, then, a valid guard must be received after an alarm before a trip signal will be accepted.

If, at the output of IC14D, a jumper is installed at J2-A, and not at J2-B, the only requirement for guard signal is that it precedes only the first trip. After the first trip, the flip-flop, IC14C and IC14D, is set and IC4C-8 is held high indefinitely. Thus, an alarm will not reset the G/T flip-flop and IC4D will remain high, hold IC10B-5 high, and allow a trip to be accepted.

If Jumper J1-A, at Pin 5 of IC10B, is installed then Pin 5 is always high and no guard signal is required to precede acceptance of a trip signal.

Low-Voltage Detector

The low-voltage-detector circuit consists of Q4, Q6, Q7, Q8, CR18, CR19, CR20, and associated resistors. Should the 12-volt supply drop below 9.8 volts, Q7 will no longer be conducting. This, in turn, shuts off Q6, which shuts off Q4 which supplies emitter current to the four output transistors. Similarly, if the −12-volt supply drops below −9.8 volts, Q8 ceases to conduct. This also shuts off Q6 which shuts off Q4. Thus Q4 is turned off by failure of either or both the positive and negative power supplies.

When Q4 is turned off, the failure of power to the other output transistors prevents the possibility of a false output signal being caused by low power-supply voltage.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 67 MBB Logic, Assembly HB-49050	
C1, 2	Capacitor, tantalum, 3.3μF, 20%, 35V, Kemet T322C335M035AS, or eq.	H-1007-1260
C3, 9, 10, 11	Capacitor, tantalum, 1μF, 10%, 35V, Kemet T110A105K035AS, or eq.	H-1007-1156
C4, 6	Capacitor, metallized polyester, 0.047μF, 5%, 250V, Siemens MKH B32561, or eq.	H-1007-1403
C5, 7	Capacitor, metallized polycarbonate, 0.056μF, 5%, 250V, Siemens MKMB325410, or eq.	H-1007-1404
C8	Capacitor, metallized polyester, 0.01μF, 5%, 250V, Siemens MKHB32560, or eq.	H-1007-1369
C12	Capacitor, metallized polycarbonate, 0.95μF, 2%, 100V, Wesco 32MPC, or eq.	H-1007-1340
C13	Capacitor, metallized polycarbonate, 0.715μF, 2%, 100V, Wesco 32MPC, or eq.	H-1007-1377
CR1-18, 21-29	Diode, silicon, Type 1N914B/1N4448	HA-26482
CR19, 20	Diode, zener, 9.1V, 5%, 400mW, Fairchild Type 1N960B, or eq.	HA-41014
DS1, 2, 3	Lamp, LED, Dialight 550-0102, or eq.	HA-39568
IC1, 2, 7, 12, 16	Linear, opamp., Raytheon RC4558NB, or eq.	H-0620-129
IC3, 11	Hex inverter/buffer, RCA CD4049AE, or eq.	H-0615-7
IC4, 14	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC5, 9	Quad, 2-input AND gate, RCA CD4081BE, or eq.	H-0615-31
IC6	Quad, 2-input OR gate, RCA CD4071BE, or eq.	H-0615-24
IC8, 15	Triple, 3-input OR gate, RCA CD4075BE, or eq.	H-0615-33
IC10	Triple, 3-input NAND gate, RCA CD4023AE, or eq.	H-0615-8
IC13	Quad bilateral switch, Fairchild F4066PC only	H-0615-65
Q1-5	Transistor, silicon, PNP Darlington, Motorola MPS-U95, or eq.	HA-47509
Q6, 8	Transistor, silicon, NPN, Type 2N2222A	HA-37445
Q7	Transistor, power, PNP, National Type 2N4249, or eq.	HA-41919
R1, 3, 4, 6, 7, 8, 10, 12, 13, 14, 16, 17, 19, 22, 23, 25-29, 31, 32, 34, 35, 37, 39, 40, 41, 43, 44, 45, 47, 49, 50-60, 62, 63, 64, 67-71	Resistor, fixed, composition, 5%, 0.25W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
R2, 5, 9, 11, 15, 18, 20, 21, 24, 36, 38, 42, 48, 65, 66	Resistor, metal-film, 1%, 0.125W, value on schematic, Type RN55E, RFL Spec HA-38301	H-1510-(xxx)
R30, 33, 46, 61	Resistor, fixed, composition, 2 ohms, 5%, 0.5W, Allen Bradley EB, or eq.	H-1009-1060
RZ1, 2, 8	Resistor, network, 10K, 2%, 4R/P, 1.1 watt, CTS 750-83-R10K, or eq.	HA-91185
RZ3-7, 9, 10	Resistor, network, 47K, 2%, 4R/P, 1.1 watt, CTS 750-83-R47K, or eq.	HA-47879
——	Schematic (Figure 5.8)	HE-49054C

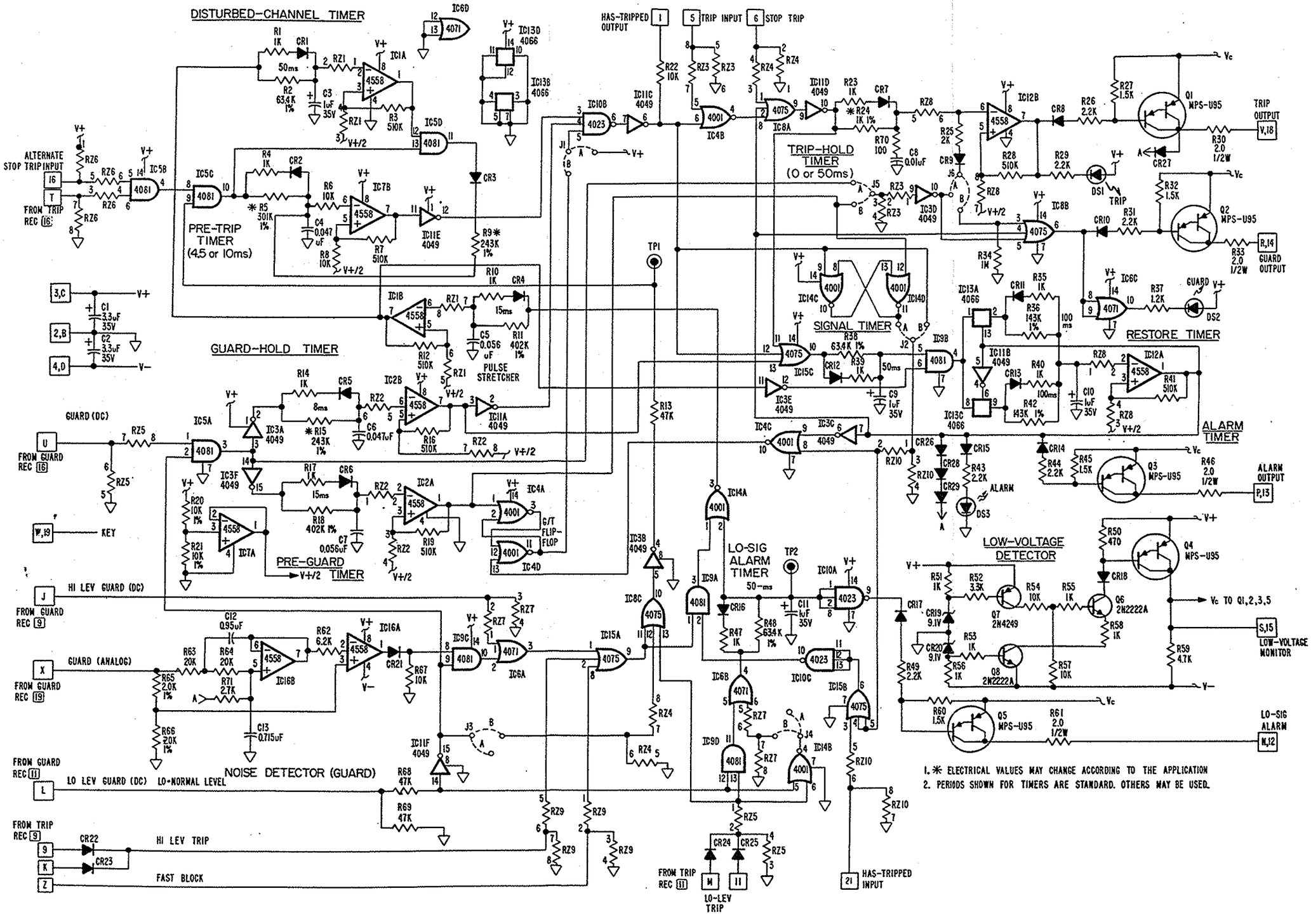


Figure 5.8. Schematic of circuit, Model 67 MBB LOGIC.

Interface Module, Model 67 MBB INTER

PURPOSE

The interface module provides for connecting the Series 6710 Protective-Relaying System to the external circuits with which it is associated. Interfaces for trip output, guard output, alarm output, low-signal condition, and communication system are provided. The module also protects against transient electrical disturbances that may be induced or carried on input and output lines. The module is shown in Figure 6.1.

CIRCUIT DETAILS

A schematic diagram of the circuits of the interface module is shown in Figure 6.4 on which the circuit is grouped into two sections, a communication section and a status section.

Communication Section

The communication section uses transformers T1 and T2 for matching a 600-ohm line under either two-wire or four-wire operating conditions. The choice between the two modes is effected by positioning J1 and J2 as indicated.

The transmitting section contains a combining amplifier, IC1 and transformer T1.

The receiving portion uses transformer T2 and a master level-adjusting potentiometer, R6. All receivers are connected in parallel to Terminals 5 and 1, and by adjusting R6 the level of the composite signal to all receivers is set simultaneously. This received signal is monitored at TP1, but the input level to the receivers is monitored at another test point, also designated TP1, on each of the paralleled receivers while receiving a signal to which that receiver is tuned.

Jumper J3 provides for applications requiring the optional output filter, HB-79595-(X), which is mounted on the transmitter module. With J3 at Position A, the output filter is bypassed, and the combining amplifier is not used. At Position B, the optional output filter is included in the signal path, but it must be installed on the transmitter. For applications using the combining amplifier, J3 is left in Position B.

Status Section

The status-indicating section of the interface module provides for four relays for announcing the status of trip, guard, alarm, and low-signal conditions. All are driven from open-collector transistors on the logic module.

The trip relay, K1 on Figure 6.2, is energized by Q1 on the logic card. Its coil voltage is nominally twelve volts, but it is operated from a 24-volt source through dropping resistor R11 which limits the coil current. When Q1 on the logic card first becomes conducting, however, the full 24-volt supply appears across the coil of K1 as C8 begins to charge.

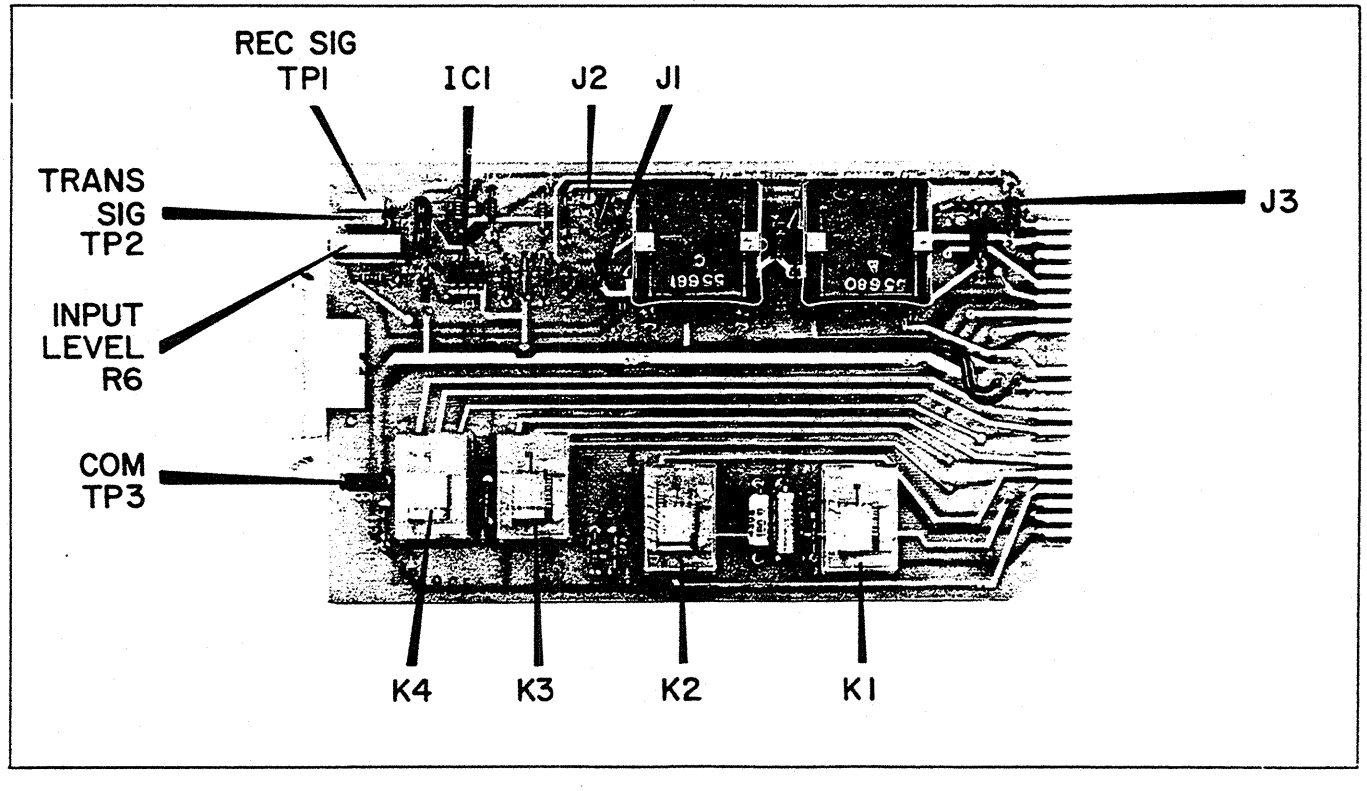


Figure 6.1. Model 67 MBB INTER-1.

This accelerates the operation of the armature of K1 and gives faster response to a trip signal. After C8 is charged, R11 sets the current in the coil.

K2 is controlled by Q2 during a valid guard condition.

The alarm relay is normally energized through Q3, and it is released to signal an abnormal condition.

The low-signal relay is normally de-energized. It is driven by Q5 on the logic module, and it is used to announce a low-signal condition on both guard and trip channels.

All relays have one set of Form-C contacts.

Output-Circuit Options

The output of the Series 6710 System consists of four output signals, derived from open-collector PNP transistors, which give the status of the system. These signals are TRIP, GUARD, ALARM, and LOW-SIGNAL. In all cases, the transistors are used to drive relays, the position of whose contacts denotes the status of each signal. Several choices, both mechanical and electrical, are available.

(1) The Model 67 MBB INTER-1 provides four high-speed relays mounted on the circuit card. The trip relay has a response time of 2.5 ms and one set of Form-C contacts rated at 30 amperes for 100 ms, 6 amperes continuous. The single set of Form-C contacts on guard, alarm, and low-signal relays is rated for 3 amperes, 250 Vac. All relays have a dielectric strength of 2000 Vrms from contacts to coil.

(2) The Model 67 MBB INTER carries no relays to provide for the possibility that other relays, not mounted on the interface card but driven by the open-collector transistors on the logic card, may be used.

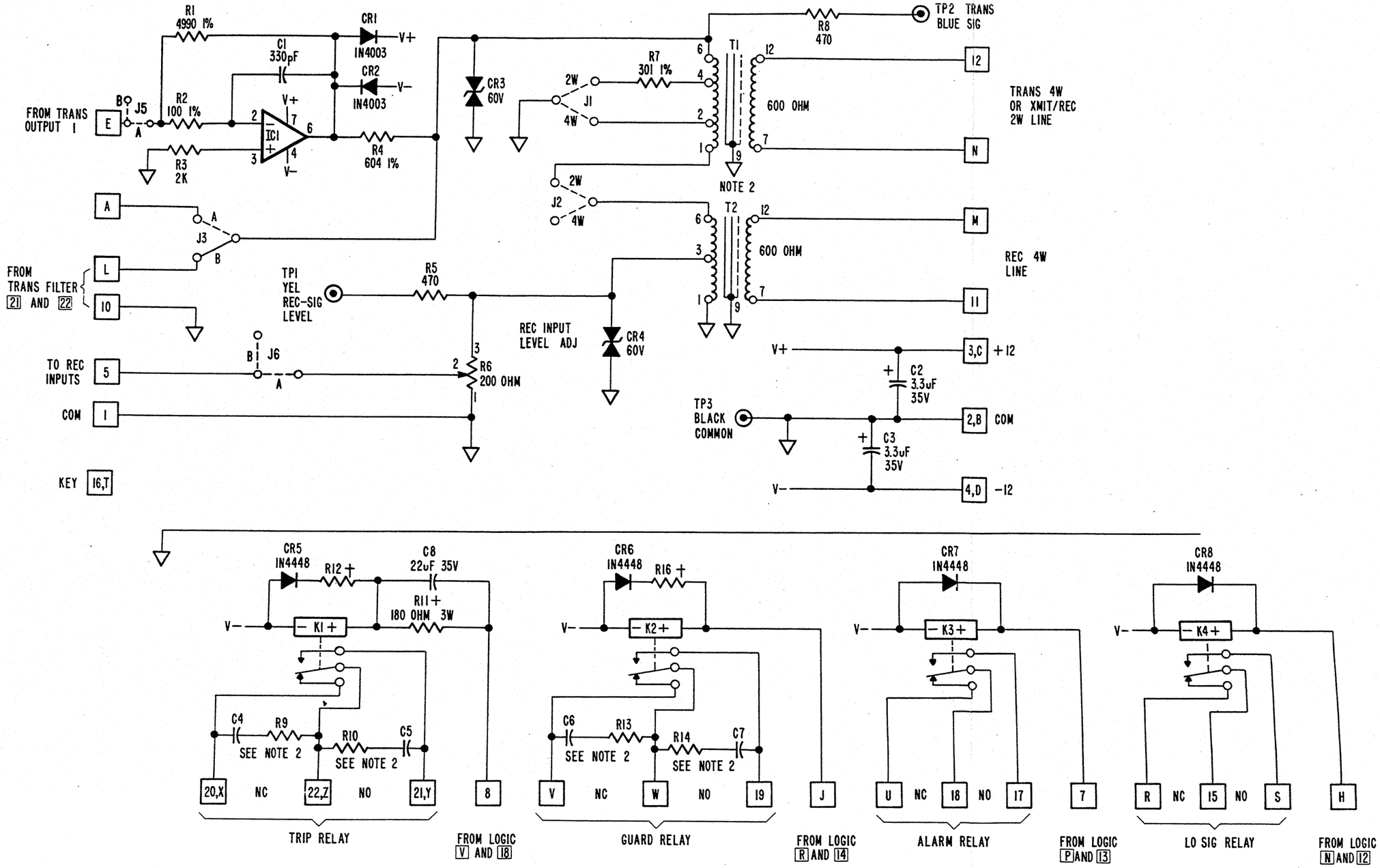
External relays may be mounted on a Model HB-49559-006 Chassis which is fastened permanently in the Model 68 Chassis. This relay chassis occupies four, standard one-half-inch module spaces in the Model 68 Chassis, and it can be fitted with up to six octal sockets for holding up to six of either of the following two relays, in any combination.

(2a) Relay Option HA-41823, recommended for trip- and guard-output functions, has a response time of 4 ms. It has two sets of Form-C contacts which will carry 30 amperes for 100 ms, ten amperes continuously. Dielectric strength is 750 Vrms between mutually insulated, conductive elements. Breakdown voltage across the contacts is 2500 Vrms.

(2b) Relay Option HA-33440, recommended for alarm and low-signal functions, carries two sets of Form-C contacts rated for 5 amperes at 120 Vac or 32 Vdc, non-inductive. Dielectric strength is 750 volts between coil and contacts.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 67 MBB INTER, Assembly HB-49055	
C1	Capacitor, dipped mica, 330pF, 2%, 500V, Electromotive DM-19, or eq.	HA-16624
C2, 3	Capacitor, tantalum, 3.3μF, 20%, 35V, Kemet T322C335M035AS, or eq.	H-1007-1260
C4-7	Not used	
CR1, 2	Diode, silicon, 1-amp, Type 1N4003	HA-30769
CR3, 4	Varistor, 60-volt, Gen. Elec. V-100ZA3, or eq.	HA-29663
IC1	Linear opamp., National LM714CN, or eq.	H-0620-52
R1	Resistor, metal-film, 4.99K, 1%, 0.125W, Type RN55D, RFL Spec HA-38301	H-1510-713
R2	Same as R1, 100 ohms	H-1510-1098
R3	Resistor, fixed, composition, 2K, 5%, 0.25W, Allen Bradley CB, or eq.	H-1009-760
R4	Same as R1, 604 ohms	H-1510-773
R5, 8	Same as R3, 470 ohms	H-1009-751
R6	Resistor, variable, metal-film, 200 ohms, 10%, 0.75W, Helipot 77PR200, or eq.	HA-26486
R7	Same as R1, 301 ohms	H-1510-1196
R9, 10, 13, 14	Not used	
T1	Transformer, match and isolation	HC-55681
T2	Transformer, match and isolation	HC-55680
———	Schematic (Figure 6.4)	HD-49059
	Model 67 MBB INTER-1, Assembly HB-49055-1	
	This model contains all components listed for Model 67 MBB INTER, plus the following:	
C8	Capacitor, tantalum, 22μF, 20%, 35V, Corning CCZ-035-226-20, or eq.	H-1007-657
CR5-8	Diode, silicon, Type 1N914B/1N4448	HA-26482
R11	Resistor, wirewound, 180 ohms, 5%, 3.25W, Ohmite 995-3A, or eq.	H-1100-464
R12, 16	Resistor, fixed, composition, 62 ohms, 5%, 0.25W, Allen Bradley CB, or eq.	H-1009-942
K1	Relay, SPDT, 12 Vdc, Schrack RU115-012, or eq.	HA-48166
K2, 3, 4	Relay, SPDT, 24 Vdc, Schrack RU115-024, or eq.	HA-48167



1. † RESISTOR VALUES DEPEND ON TYPE OF RELAY USED.
2. FOR T1 AND T2, DIELECTRIC STRENGTH BETWEEN WINDINGS, SHIELD, AND HARDWARE IS TESTED AT 2500 Vdc.

Figure 6.4. Schematic of circuit, Model 67 MBB INTER-1.

Series 6000 DC-DC Converter Power Supplies

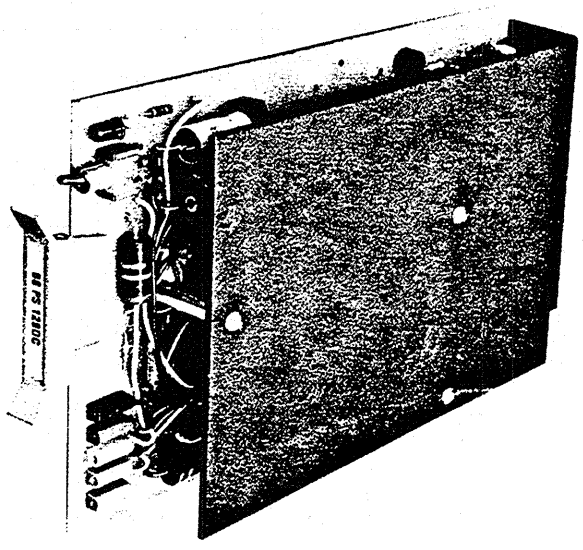


Figure 7.1. Typical 0.375-Ampere DC-DC Power Supply. Metal bracket spanning the circuit card is the heat sink for IC1 and IC2.

DESCRIPTION

These six DC-DC Converters are part of the group designed to supply necessary dc power to RFL Series 6000 equipment. All power supplies provide dual 12-Vdc outputs which are isolated and surge-protected from the primary-power source. The two 12-volt outputs are completely independent and may be wired externally to obtain plus and minus 12 Vdc, +24 Vdc, or −24 Vdc. An auxiliary 10-kHz squarewave output has been provided for low-power external functions.

Models with "PS" in their designation utilize an integral series-pass-type voltage regulator and will deliver 0.375 ampere from each, independent output.

Models with "HPS" in their designation utilize an external regulator and heat dissipator, provision for which has been made in all RFL Model 68 Chassis. These will deliver 1 ampere from each independent output.

As suggested by their model numbers, both low-current and high-current models are available for operation from primary-power sources with levels of 104-140 Vdc (nominal 129 V), 42-56 Vdc (nominal 48 V) or 21-28 Vdc (nominal 24 V).

Overvoltage protection, based upon the familiar crowbar principle, is included on all models. Its presence is indicated by the suffix "-1" in the model number.

Table 1 summarizes the various models.

THEORY OF OPERATION

These supplies use a two-transformer inverter, as shown on Figure 7.6. Power transistors Q1 and Q2 act as switches alternately turning on and off, and so reversing the flow of primary current through T2.

In both T1 and T2, the sides of the windings indicated by dots have the same polarity: When Q1 is on, for example, all the dotted sides are positive. The secondary windings of T1 hold Q1 on and Q2 off. When the flux density of T1 reaches saturation, its voltages drop to zero and then reverse. At this point, Q2 turns on and Q1 turns off, and the sequence starts over again. The frequency of oscillation is approximately 10 kHz.

The output of T2 is rectified and filtered by CR3, CR4, C6, and C7. IC1 and IC2 are integrated circuits functioning as series regulators. In low-current converters, these regulators are located on a heat sink attached to the circuit board carrying all other circuits. For one-ampere converters these series regulators and their associated filter capacitors C1 and C3, or C2 and C4, are located on the external heat dissipator of Option HB-46580. Figure 7.6 shows the power unit and one-amp regulator. Figure 7.5 shows the 0.375-amp regulator.

For overvoltage protection (OVP), the output voltage is monitored by zener diode CR5 or CR7. If output voltage exceeds the zener voltage, current through R5, or R7, will fire the gate of SCR1, or SCR2, and the SCR thus becomes a short-circuit across the power supply. The current so drawn will destroy Fuse F3, or F4 and drop the output voltage to zero. Power to the load cannot be restored unless the fuse is replaced, and should not be restored until the fault is cleared.

An auxiliary 10-kHz squarewave output is available at Terminals 17 and 18 for external functions. The output will vary between 34 and 52 volts, peak-to-peak, depending upon input voltage to the converter. The sum of currents taken from Terminals 17 and 18, plus that from the lower output circuit, Figure 7.6, should not exceed one ampere.

TABLE I

Module Designation	HB-41505 1A Pwr.Sply.-129VDC	HB-41515 1A Pwr.Sply.-48VDC	HB-41935 1A Pwr.Sply.-24VDC	*HB-46580 Pwr. Sply. Reg.	HB-41535 Overvolt.Prot.Opt.	HB-41500 Pwr.Sply.-129VDC	HB-41510 Pwr. Sply.-48VDC	HB-41930 Pwr.Sply.-24VDC
68 HPS 129DC-1	•			*•	•			
68 HPS 48DC-1		•		*•	•			
68 HPS 24DC-1			•	*•	•			
68 PS 129DC-1					•	•		
68 PS 48DC-1					•		•	
68 PS 24DC-1					•			•

*This regulator is a unit separate from the power supply, but is always required except when ordering spare or replacement modules.

TECHNICAL DATA

Input Voltage: 24-volt units: 21-28 Vdc
48-volt units: 42-56 Vdc
104-140 Vdc
Allowable ripple: 1.5 Vrms, max.

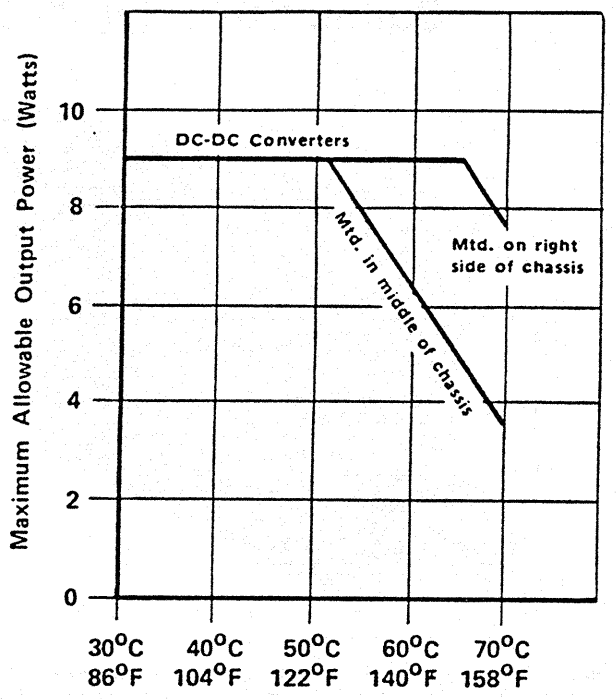
Output Voltage: Two independent 12-Vdc outputs, not adjustable. Each output will be between 11.4 and 12.6 V for any combination of input voltage, load, and temperature.

Output Current: 0.375 A max. from each output for 68 PS units, 1.0 A from each output for 68 HPS units. See Figure 7.4 for max. total rating of 68 PS units.

Overvoltage Trip: 13.5 to 15.5 Vdc, not adjustable.

Ambient Temperature: −30°C to +70°C.

Size: 1.5" x 4.713" x 8". Requires three module increments in RFL 68 Chassis for either high-current or low-current modules. In addition, 1-Ampere units require space at rear of 68 Chassis for mounting HB-46580, for which provision is made with certain backplates.



Derating curve for all 0.375-ampere DC-DC Converters.

INSTALLATION

The accompanying curve shows recommended deratings for all 0.375-ampere power supplies. It does not apply to one-ampere units, for which no derating is required owing to their external heat sink. These curves are based upon maximum input voltage and upon installation in a chassis which itself was mounted between two unventilated chassis in a 19-inch rack.

Other considerations can modify the curves. If forced air is used, the curves will improve. On the other hand, the temperature inside a chassis will rise approximately ½°C per watt dissipated in the chassis itself and so cause the curves to worsen. A small improvement is obtained when an air gap of 1-¾ inches is left between chassis.

The power output is based upon the sum of the powers taken from the two output sections. One side of the supply may be used at a higher output current than the other; and it is necessary only to keep the total power output below the derating curves. Of course, the maximum output-current levels given in the Specifications should not be exceeded.

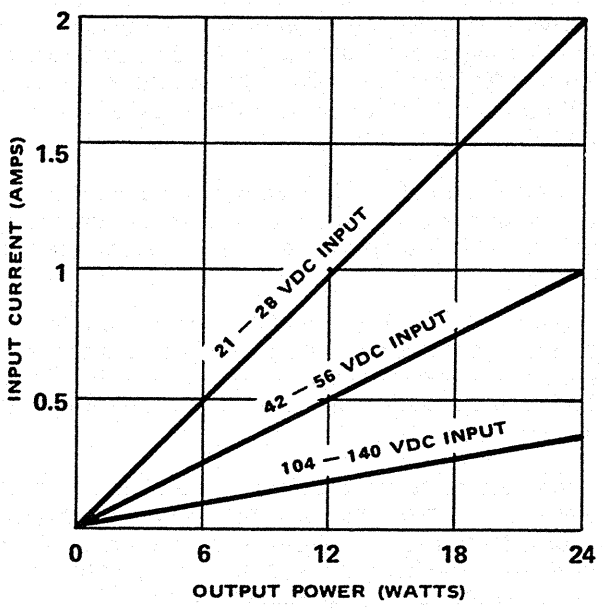


Figure 7.4. Typical input current vs. output power.

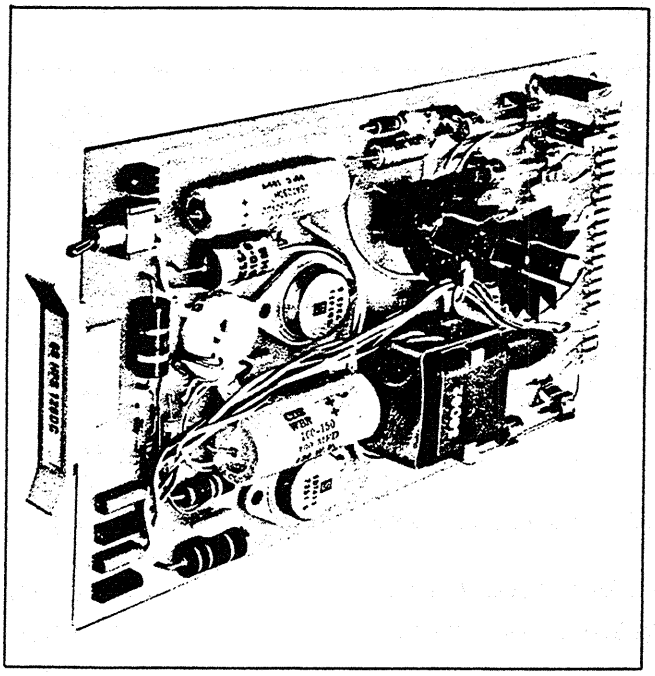


Figure 7.2. Typical 1-Ampere DC-DC Power Supply. Heat radiators shown on CR3 and CR4 are used to increase heat dissipation. Series regulator for one-ampere units is separate module, shown in Figure 7.3.

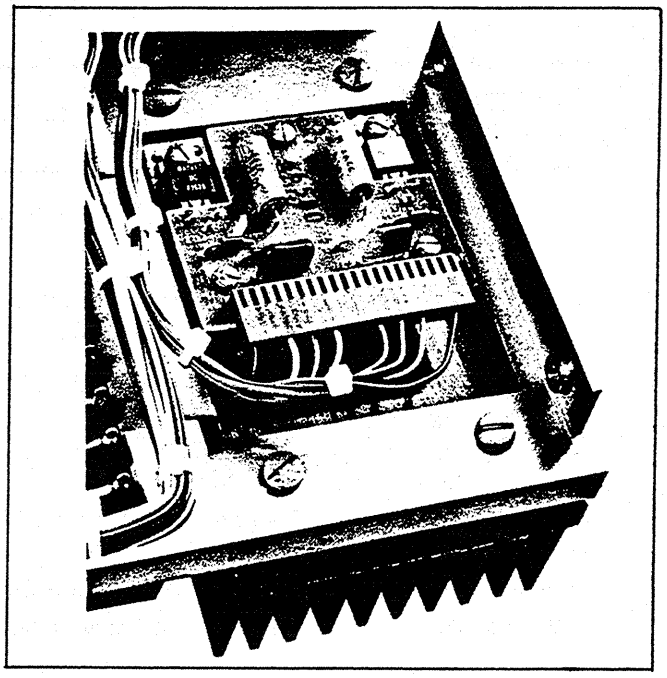


Figure 7.3. Option HB-46580, used with all one-ampere supplies, is externally mounted at rear of 68 Chassis used to house all Series 6000 equipment.

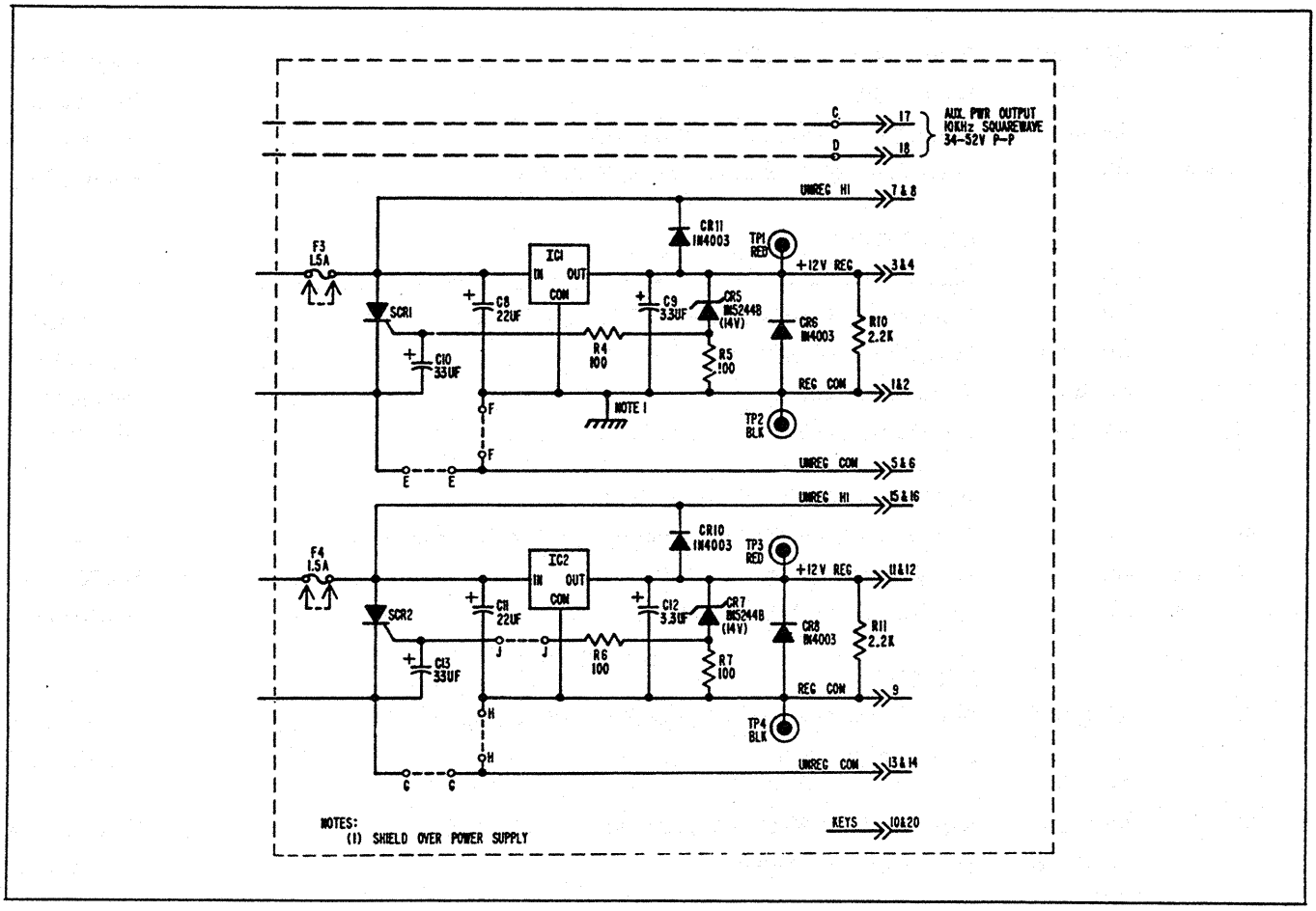
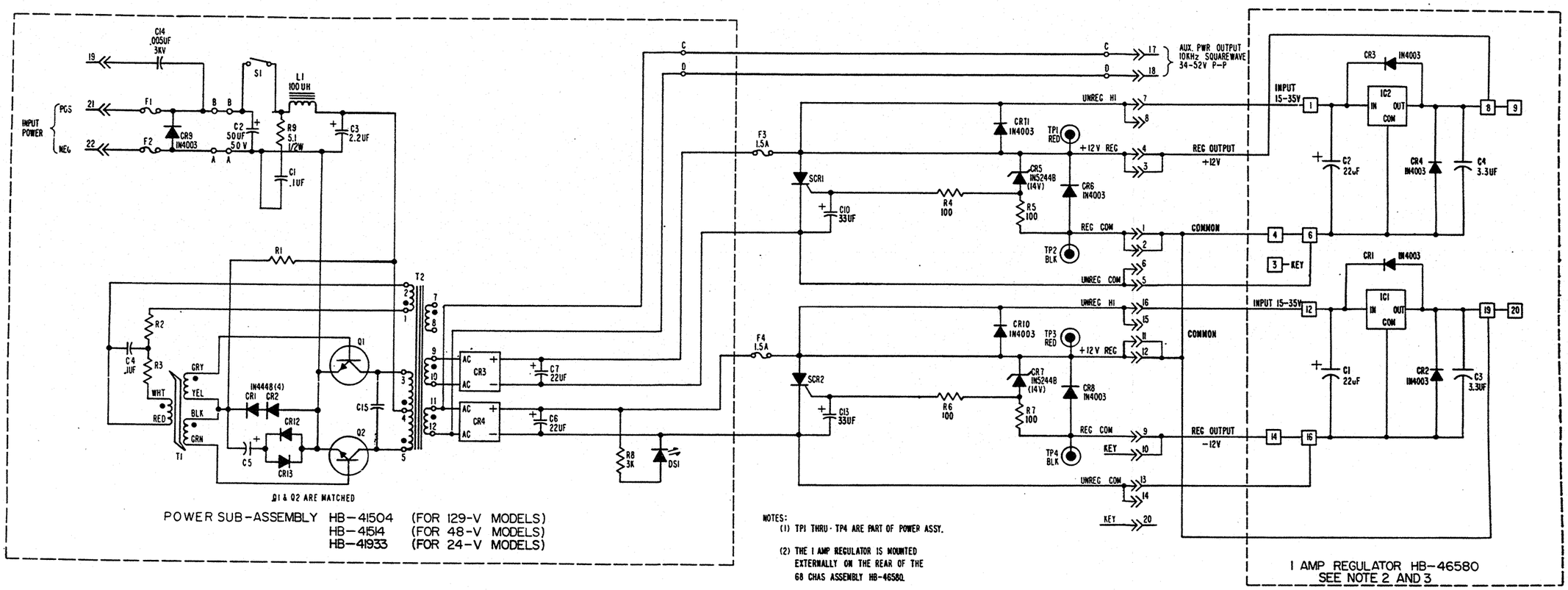


Figure 7.5. Schematic of circuit of regulator used in 0.375-ampere supplies.

PARTS LIST

CIRCUIT SYMBOL		DESCRIPTION	PART NUMBER
		Series 6000 DC-DC Converters	
		CAPACITORS	
C1	All	Capacitor, met. poly.: 0.1μF, 10%, 250V, Seacor 106-01	H-1007-1255
C2	All	Capacitor, electrolytic: 50μF, −10% +100%, 150V, C-D WBR-50-150	H-1007-1263
C3	All	Capacitor, mylar, 2.2μF, 5%, 200V, Wesco 32MM	H-1007-833
C4	All 129V	Same as C1	
C4	All 48V	Same as C1	
C4	All 24 & 12V	C4 is omitted	
C5, 6, & 7	All	Capacitor, tantalum: 22μF, 20%, 35V, Corning CCZ-035-226-20	H-1007-657
C8 & 11	All 0.375-A		
C9 & 12	All 0.375-A	Capacitor, met. poly.: 3.3μF, 10%, 250V, Seacor 106-0.1	H-1007-1260
C10 & 13	All	Capacitor, met. poly.: 33μF, 10%, 250V, Seacor 106-0.1	H-1007-1142
C14	All	Capacitor, ceramic disc: 0.005μF, −20 − +80%, 3kV, RMC 3KV5000Z5U	H-1007-1264
C15	All 129V	Capacitor, dipped mica, 470pF, 2%, 500V, Electro Motive DM-19	HA-16632
C15	All 48V	Capacitor, dipped mica, 2000pF, 5%, 500V, Electro Motive DM-20	HA-16222
C15	All 24V	Omitted	
		FUSES	
F1 & 2	All 129V	Fuse, slo-blo, ¾ A, 125V	HA-10780
	All 48V	Same, 1.5A	HA-35852
	All 24V	Same, 3.0A, 125V, Littlefuse 313 003	HA-6607
F3 & 4	All	Fuse, 1.5A, 250V, 3AG, Littlefuse 312-01.5	HA-41524
		INDUCTORS	
L1	All	Choke, Ferrite-core, 100μH, 2A, 0.103 ohm, Caddel Burns 6310-8	HA-41074
T1	All	Transformer, inverter-driver	HB-38366
T2	All 129V	Transformer, power	HB-38061
T2	All 48V	Transformer, power	HB-38062
T2	All 24V	Transformer, power	HB-38549
		MISCELLANEOUS COMPONENTS	
S1	All	Switch, toggle SPDT: Right angle mtg., C & K Components 7101-A	HA-39562
TP1 & 3	All	Test jack, red: Cinch 119437-B	HA-38116-2
TP2 & 4	All	Test jack, black: Cinch 119437-C	HA-38116-3
		RESISTORS	
R1	All 129V	Resistor, fixed comp.: 15K, 5%, 2W, Allen Bradley HB	H-1009-251
	All 48V & All 24V	Same as above, 2.7K	H-1009-1062
R2	All 129V	Resistor, fixed: 33 ohm, 5%, 2W, Allen Bradley HB	H-1009-1064
	All 48V & All 24V	Same as above, 22 ohm	H-1009-1063

CIRCUIT SYMBOL		DESCRIPTION	PART NUMBER
R3	All 129V	Resistor, fixed comp: 12 ohm, 5%, 1W, Allen Bradley GB	H-1009-1065
	All 48V & All 24V	Same as above, 10-ohm	H-1009-4
R4, 5, 6, 7	All	Resistor, fixed comp: 100 ohm, 5%, ¼W, Allen Bradley CB	H-1009-758
R8	All	Resistor, fixed comp.: 3K, 5%, 1W, Allen Bradley GB	H-1009-466
R9	All	Resistor, fixed comp: 5.1 ohm, 5%, ½W, Allen Bradley GB	H-1009-712
R10, 11	All	Resistor, fixed comp: 2.2K, 5%, ¼W, Allen Bradley CB	H-1009-767
		SEMICONDUCTORS	
CR1, 2, 12, & 13	All	Diode, silicon, Type 1N914B	HA-26482
CR3 & 4	All	Rectifier bridge assy., Varo VS-148X	HA-39509
CR5 & 7	All	Diode, zener: 14V, 5%, 500mW, Type 1N5244B	HA-41075
CR6, 8, 10, 11	All 0.375-A Units	Diode, rectifier: 1A, Type 1N4003, Solitron S4003TA20	HA-30769
DS1	All	Light-emitting diode, Dialight Cp. 550-0102	HA-39568
IC1 & 2	All	Three-terminal voltage reg., Fairchild UGH 7812393, National LM340-12T	H-0620-69
Q1 & 2	All 129V	Transistors, matched pair	HA-46756
	All 24V	Transistors, matched pair	HA-46757
SCR1 & 2	All	Silicon controlled rectifier, Motorola 2N4441 or GE C122F	HA-41072
	All	Schematic (Figure 7.6)	HE-48107
		PARTS LIST FOR 1-AMP EXTERNAL REGULATOR, P/N HB-46580	
C1 & 2	All 1-Amp.	Same as C8 in basic unit	
C3 & 4	All 1-Amp.	Same as C9 in basic unit	
CR1, 2, 3, & 4	All 1-Amp.	Diode, rectifier, 1A, Type 1N4003	HA-30769
IC1 & 2	All 1-Amp.	Same as in basic unit	
R10 & 11	All	Resistor, fixed comp: 2.2K, 5%, ¼W, Allen Bradley CB	H-1009-767



OPTIONAL COMPONENT LISTING						
SUB-ASS'Y	R1	R2	R3	F1, F2	C5	C15
HB-41504	15K	33	12	.75A	22UF	470 pF
HB-41514	2.7K	22	10	1.5A	22UF	2000 pF
HB-41933	2.7K	22	10	3A	22UF	—

NOTES:
(1) TP1 THRU TP4 ARE PART OF POWER ASSY.

(2) THE 1 AMP REGULATOR IS MOUNTED EXTERNALLY ON THE REAR OF THE 68 CHAS ASSEMBLY HB-46580.

(3) FOR 0.375-AMPERE SUPPLIES THE REGULATOR IS ON CIRCUIT CARD AND SCHEMATIC IS SHOWN SEPARATELY.

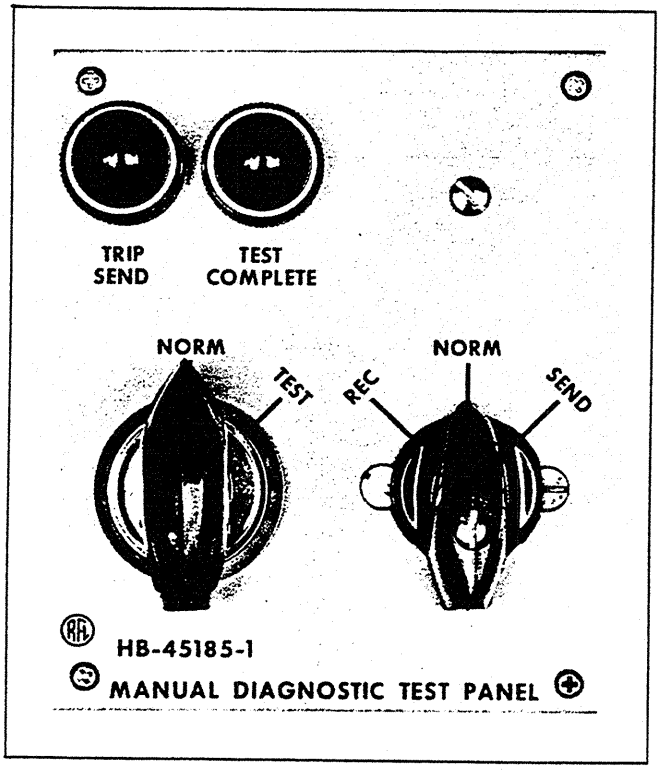
Figure 7.6 Composite schematic of wiring for Model 68 HPS (...) DC Converter HE-48107

OTHER MODULES

Supplementing the basic modules which comprise all Series 6710 Systems described in the foregoing part of this manual, is a group of modules used to perform useful auxiliary functions. When these are used in a system, data describing their operation and maintenance will be included, following this section, in the manual prepared specifically for that system. A list and brief description of modules current at the time of writing follows. Others may be added from time to time. In all cases, detailed data are available.

Manual Diagnostics (67 Man. Diag.)

This diagnostic component affords continuity testing of the Model 6745 System, namely the transmitter, communication system, and receiver (but not the trip relay). The unit mounts internally in the basic system chassis. Indicator lamps, a send-receive test switch (spring return to send), and a key-lock switch for normal-test permit the operator to check out the system without tripping the associated breakers.



Model 67 MBB Level Indicator monitors the received-signal level, using a guard or trip receiver, and indicates its relative level on an edgewise panel meter. It will also drive an external meter, and a solid-state output will operate either an internal or external alarm relay to signal an alarm condition.

Universal Interface Assembly Model 67 UNIV: Nearly every installation of the Series 6710 equipment has a requirement for one or more auxiliary circuits needed to fit it into the system with which it is to be used. To implement this need, the Model 67 UNIV has been designed as a support for accommodating a wide variety of auxiliary circuits often used to support the Series 6745.

While installations differ in detail, it has been possible to conceive several such auxiliary circuits, to standardize them, and to provide for mounting them as an integral part of the equipment by using the Model 67 UNIV. These include:

Model HB-90110 Attenuator is a 600-ohm-to-600-ohm bridged-T attenuator with adjustable attenuation to a maximum of 45 dB.

Model HB-90120 Seal-In is an SCR-controlled latch circuit which will hold a relay energized after an initiating pulse has disappeared.

Model HB-90125 Permissive Coordinating Module is designed for use with line relays and auxiliary devices used in directional-comparison permissive-overreaching transfer-trip systems.

Model HB-90130 Mercury Relay and Driver drives a relay with a single set of Form-C mercury-wetted contacts in response to either a logic one or a logic zero as the initiating signal.

Model HB-90135 Lockout Relay is an assembly in which a spring-type relay, whose contacts serve as an output signal, is controlled by a silicon-controlled rectifier which, in turn, is controlled either locally or remotely.

Model HB-90140 AND Driver used a two-input AND gate to drive an open-collector PNP output transistor capable of pulling 100 mA.

Model HB-90145 One-Shot Timer provides a buffer and driver for operating a totalizing counter with an open-collector transistor.

Model HB-90150 Mercury Relay is a relay with a single set of Form-C mercury-wetted contacts.

Model HB-90160 Relay DPDT is a relay, mounted on a plug-on card, with two sets of Form-C contacts.

Model HB-90165 Delay Timer is a Schmitt-trigger timer designed to require that the input be at a logic high for at least 100 ms before the output will go high. Provision for override is available.

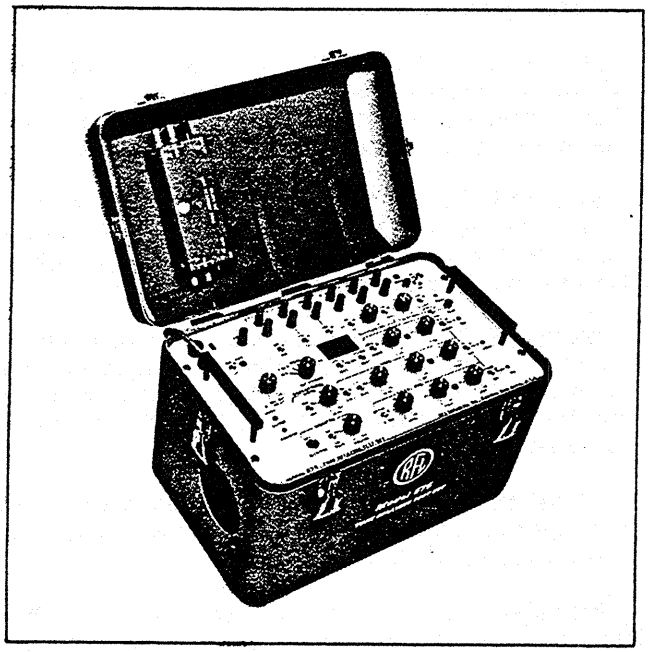
Model HB-90170 Opto-Isolator provides for electrical isolation between two circuits. It is frequently used as a keying circuit.

Model HB-90175 Hold Timer is a Schmitt-trigger which holds its output at a logic high for at least 100 ms after its input goes low. Provision for an override is available.

Model HB-90185 Trip Seal-In provides for holding a received trip signal and sustains its own trip-output signal even though the carrier for a valid trip signal may subsequently fail. Return of guard signal will reset, or clear, the circuit.

Tone-Relaying Test (Test Model 675)

The Model 675 Tone-Relaying Test is a separate unit designed specifically for guesswork-free evaluation of tone transfer trip systems. The unit may also be used to diagnose on-line system performance under adverse conditions. It simulates background noise, white noise, either band-limited or to 20 kHz, power-fault noise, interfering tones, 60-Hz arcing, and abrupt level changes. Adjustable start-stop gating circuits afford independent adjustment of tripping and noise-burst rates, as well as signal-stepping functions. An adjustable timer measures trips received with a two-digit display for testing dependability and security.



The Model 675 provides what previously has been next to impossible in difficult trip measurements . . . test repeatability.

Trip Current Booster (67 Driver/67 Dual Driver)

The trip-current booster is a solid-state current amplifier with a capability of 10 amperes continuous, or 30 amperes for 100 ms. Single or dual outputs are available. The unit is self-contained in a box designed for wall- or cabinet-mounting. Two connectors enable input wires to be brought in through electrical conduit. Two internal, four-pin terminal blocks provide points for spade-lug connections. Each device meets IEEE High-Potential Surge-Withstand Capability Specifications.